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## CMS tracker phase-2 upgrade module noise and mitigation

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The CMS tracker phase-2 upgrade modules are required to reach noise levels close to the ones expected from the analog front-end attached to an ideal pixel/strip. Module prototypes, featuring the latest and final prototype hybrids before the production, showed noise that was higher than the expected which could pose a problem in terms of achieving the hit efficiency target. Investigations that followed, lead to an unexpected failure mode which is modeled in order to guide mitigation tweaks for the production designs. Knowledge acquired from the investigations along with the noise mitigation design changes implemented on the production hybrids are presented.

### Summary (500 words)

Two module types (2S and PS) will be used in the Compact Muon Solenoid (CMS) Tracker Phase 2 Upgrade for the High Luminosity Large Hadron Collider (HL-LHC). The 2S modules contain a double strip sensor configuration with an active area of  $(10 \times 10)$  cm<sup>2</sup>, wire bonded to two front-end hybrids that are powered and controlled by a service hybrid. The PS modules contain a strip sensor and a macro-pixel sensor of  $(5 \times 10)$  cm<sup>2</sup> wire bonded to two front-end hybrids interconnected with a power hybrid on one side and with an optical readout hybrid on the opposite side.

The three front-end (FE) ASICs that are responsible for the readout of the sensors of the two types of modules all employ binary readout. The noise per channel affects directly the hit efficiency. Higher noise means a higher threshold for the discriminator of the FE ASICs and consequently a higher percentile of signals not being detected. The CMS collaboration is targeting a hit efficiency of at least 99.5% on the active sensor region which leads to a very stringent requirement for the channel noise of the final system. This requirement is reaching almost the theoretical limits of noise as expected from the analog FE attached to an ideal strip/pixel and presents a significant challenge for the hybrid circuit and module designs.

The latest prototypes of hybrids are including all the features foreseen for the final modules and are optimized compared to previous prototypes in terms of thermal, power and noise performance. After modules with these hybrids were built and noise performance data started getting gathered, it became clear that the noise was higher than what was expected. A 20-30% increase compared to simulations and simpler earlier prototypes was measured, for both modules. Even though an increase in the noise was somewhat expected since the latest modules featured big circuits, buck converters and sub-optimal high voltage filtering because of module constraints, an investigation was launched to understand the exact pathways the extra noise was injected to the analog channels.

Ground (common mode) noise generated at the hybrids handling the voltage conversions between the two FE hybrids that would otherwise have been inconsequential, combined with unintended consequences of design choices at the module and sensor level are understood to be the main contributor to the increased noise on both modules. After the investigations, all of the different hybrids underwent design changes in order to address this issue along with other minor noise sources.

In this contribution, the noise performance of the latest PS and 2S module prototypes compared to the theoretical and early experimental results will be analysed, outlining the difficulties of the final system to reach the theoretical noise performance. A model to explain the results of the noise investigations will be presented

and the hybrid design changes for the production will be shown, focusing on the ones that target the noise issue. The information presented could be extremely useful for future low noise module designs.

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