Contribution ID: **197** Type: **Poster**

Integration and Commissioning of the ATLAS Tile Demonstrator Module for Run 3

Tuesday 20 September 2022 16:40 (20 minutes)

The electronics of the ATLAS Tile Calorimeter will be replaced for the HL-LHC. The TileCal Phase-II upgrade project has undertaken an extensive R&D program. A Demonstrator module containing the upgraded on-detector readout electronics was built in 2014, evaluated during seven test beam campaigns, and inserted into the ATLAS experiment in 2019. The Demonstrator module was build with backward compatibility with the present ATLAS systems. We present the current status and test results from the demonstrator module running in ATLAS.

Summary (500 words)

The TileCal Phase-II Upgrade will accommodate the detector readout electronics to the HL-LHC conditions using a new clock and readout strategy. In this new architecture, the on-detector electronics will transfer detector data to the off-detector electronics through high-speed optical links at the bunch crossing frequency (˜25 ns). In the counting rooms, the off-detector electronics will store the digitized samples in pipelined buffers, and compute reconstructed trigger objects for the first level trigger. In addition, the off-detector electronics will be responsible for the distribution of the LHC clock towards the on-detector electronics for the sampling of the detector signals.

The Demonstrator module consists of four independent mini-drawers capable to operate up to 12 PMT blocks. A mini-drawer is composed of a mechanical aluminum structure that supports one Mainboard, one Daughterboard, one high voltage regulation board, and up to 12 PMT blocks equipped with 3-in-1 cards. The PMT signals are shaped and amplified in two gains by the 3-in-1 cards and digitized in the Mainboard by 12-bit dual ADCs. The Daughterboards transfer the digitized data to the off-detector electronics through high-speed optical links. In addition, the lower gains of the 3-in-1 cards are summed in towers and transmitted to the Level-1 Calorimeter trigger system for trigger decision.

In the off-detector electronics, the Tile PreProcessor Demonstrator operates the Demonstrator module, implementing the upgraded clock and readout architecture envisioned for the HL-LHC. The Tile PreProcessor Demonstrator also enables backward compatibility of the Demonstrator module with the present ATLAS Trigger and Data AcQuisition and the Timing, Trigger and Command systems. Several integration tests were carried out for the commissioning of the Demonstrator module at CERN. Bit Error Ratio (BER) tests were used to evaluate the signal quality of the high-speed links between the TilePreProcessor and the Demonstrator module. In addition, the latency stability between the distributed and the received clock was also studied using digital techniques based on subsampling. In addition, the performance of the upgrade electronics has been studied with Charge Injection, Laser, and Cosmic runs, showing excellent performance in terms of low noise, signal quality, and timing. This contribution describes in detail the hardware and firmware for the implementation of the data acquisition system for the Demonstrator module and discusses the results of the integration tests performed during the commissioning of the Demonstrator module for Run 3.

Primary author: FALTOVA, Jana (Charles University (CZ))

Presenter: TLOU, Humphry (University of the Witwatersrand (ZA))

Session Classification: Tuesday posters session

Track Classification: Systems, Planning, Installation, Commissioning and Running Experience