Investigations on Hardware Implementable Algorithms for Particle Detector Read-Out

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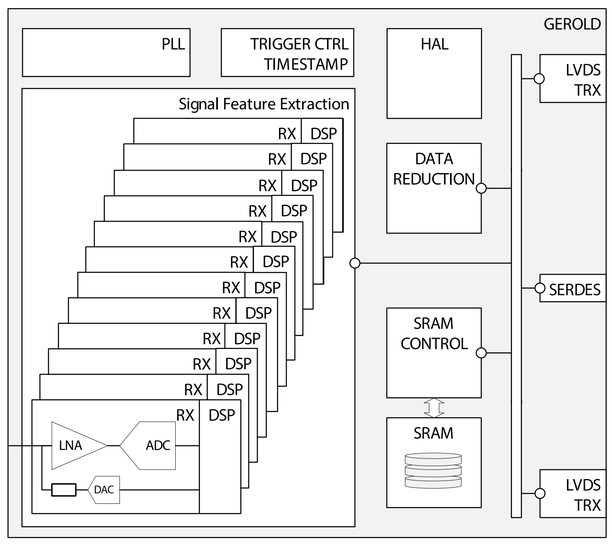
Read-Out concept

An adjustable low noise amplifier based front-end together with a flexible ADC provide the means to adapt the design to different detector implementations. The specifications fore-see a 500 MHz 8 to 12 Bit ADC.

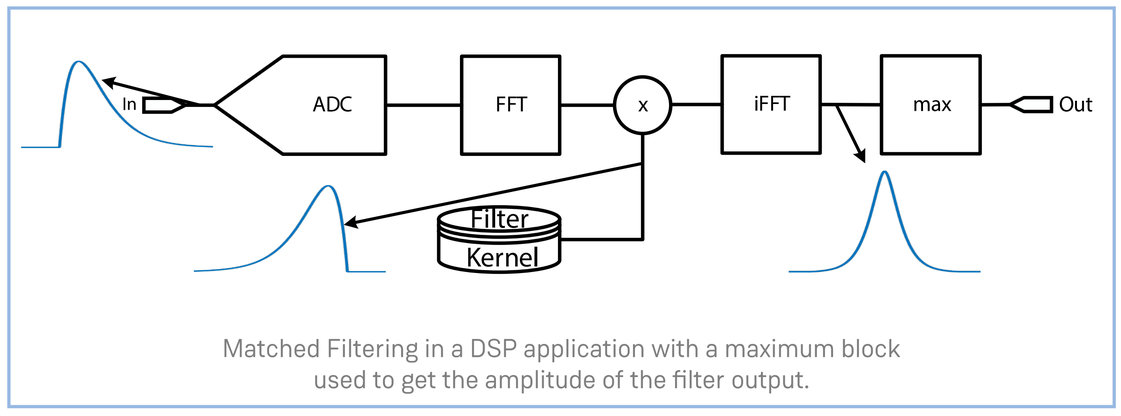
Additionally subnanosecond time resolution edge detection is under investigation.



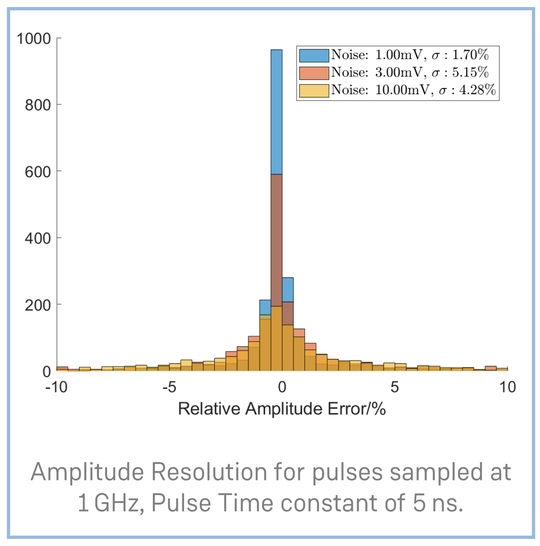
Our design uses two DSP cores. One on every single channel for processing of the waveforms. This core provides triggering, timing and charge estimation capabilities. The second core, on the cluster level combines the channel information to perform event triggering and energy estimations.

Matched Filters for Amplitude Estimation

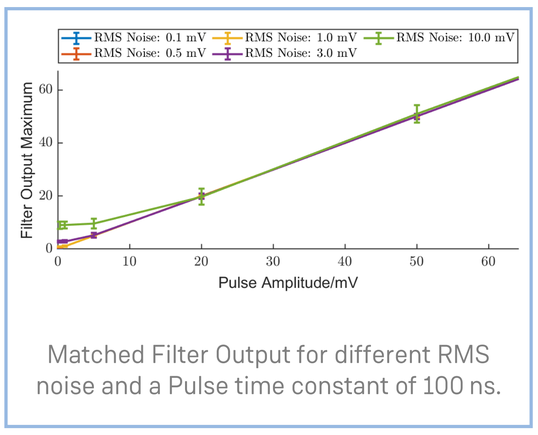
The matched filter is a communications theory based technique, that allows signal detection even in high noise environments.
By correlating the input waveform with a template of the expected signal, it achieves the best SNR. [3] An Example from our studies is the use for such a filter for improved amplitude estimation.



Matched Filtering in a DSP application with a maximum block used to get the amplitude of the filter output.

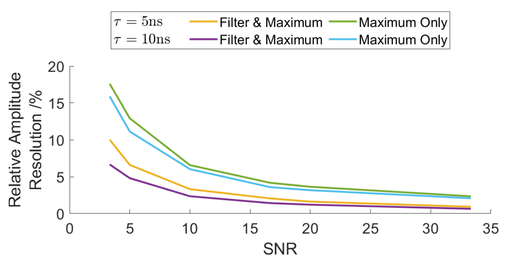


Amplitude Resolution for pulses sampled at 1 GHz, Pulse Time constant of 5 ns.



Matched Filter Output for different RMS noise and a Pulse time constant of 100 ns.

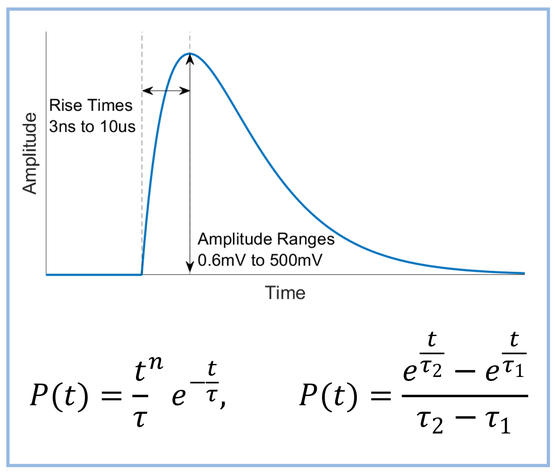
The output amplitude of a matched filter highly correlates with the amplitude of the input signal. The correlation only drops at an SNR of approximately 2. Correcting this influence could be possible.



Matched Filter Amplitude resolution compared to maximum finder without a filter. Sampling Rate is 1 GHz.

The matched filter approach achieves a factor 2 better amplitude resolution compared to a maximum finder without filtering.

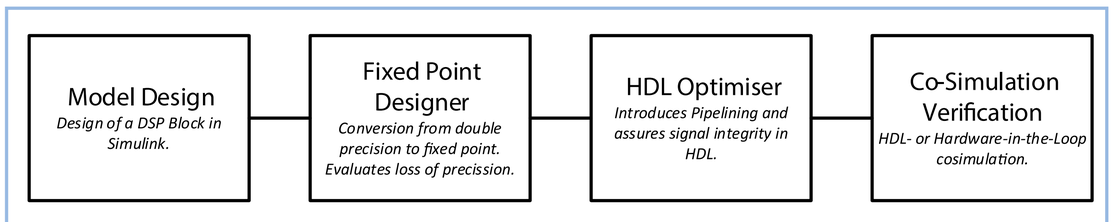
Digital Signal Processing in Simulink



$$P(t) = \frac{t^n}{\tau}\, e^{-\frac{t}{\tau}}, \qquad P(t) = \frac{e^{\frac{t}{\tau_2}} - e^{\frac{t}{\tau_1}}}{\tau_2 - \tau_1}$$

1. Use typical models for sharper output signals, as shown on the left. [1],[2]
2. Models for white and pink noise can be used in simulation
3. Parameterized Simulink models allow adjusting sampling time, bit resolution and model parameters.

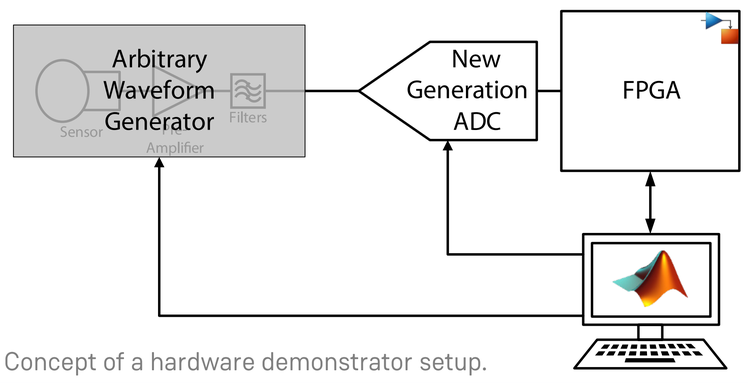
For development and verification we use Matlab and Simulink. It offers capabilities for the design of HDL convertible models with controlled testing and verification. A typical workflow from model to generated HDL is shown below.



Matlab HDL Development Workflow.

Hardware Demonstrator

A demonstrator setup is under construction using our New Generation ADC demonstrator. The ADC features an adjustable Resolution of 8 or 12 Bits and a sampling rate adjustable between 100 MHz and 1 GHz and was designed in 28nm CMOS. [4]
We already presented the ADC at last years TWEPP.



Concept of a hardware demonstrator setup.

The algorithms developed as part of this work will be deployed on an FPGA card for testing. Matlab and Simulink provide the means to run controlled simulations.

We start with using an Arbitrary Waveform Generator in order to get first hardware verifications. The design foresees the coupling to a particle detector in order to evaluate our systems in application at a later stage.

Outlook: Research Target

The overall target of this research project is the delivery of a read-out ASIC that incorporates our ADC and front-end together with a set of DSP blocks.

The tune ability of the ADC together with togglable DSP blocks allows to adjust the power demand and performance of this ASIC for the needs of different detector and sensor setups.

[1] CMOS, Angelo Rivetti, 2015
[2] Radiation Detection and Measurement, Knoll, 1979
[3] The Scientist and Engineer‘s Guide to Digital Signal Processing, S.W. Smith, 1997
[4] Towards a generic receiver chain for particle detectors, L. Krystofiak, 2022

Definitions:
SNR – Pulse Amplitude over RMS Noise

Electronic Systems (ZEA-2)
Detector Systems

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