Contribution ID: **54** Type: **Poster**

Investigations on Hardware Implementable Algorithms for Particle Detector Read Out

Tuesday 20 September 2022 16:40 (20 minutes)

In order to meet power and heat budget in large multichannel detector systems, an early data reduction by the means of signal feature extraction is necessary.
We are contributing to this topic, studying different approaches from analog and digital signal processing, investigating the influence of parameters like bandwidth and digitizer resolution. In a second step, we are looking into the influence of the signal parameterization, evaluating algorithms that are suitable for sensors of different characteristics.
We will present our methodology together with first results, showing the capability of common approaches as well as novel ideas.

Summary (500 words)

Modern detector systems often consist of several thousands of individual sensors that all need to be read out in parallel. This results in large amounts of data to be transmitted, requiring high-speed interfaces with a high power draw, and heat generation. Both are undesirable properties, as they can influence the detector performance negatively.
In order to mitigate these downsides, the data needs to be reduced early in the processing chain. How this is done best is the subject of past and ongoing research. The most popular approach being to directly extract the information of interest from the signal, limiting the amount of transmitted data to a few bytes per event. This approach requires circuitry, either analog or digital, that can
\begin{itemize}
\item[\lbrack a\rbrack] reliably detect a pulse coming from the sensor.
\item[\lbrack b\rbrack] extract the pulse features that encode the desired information.
\end{itemize}
To aid in the research process, we have developed a tool set in Matlab that allows the simulation of analog and digital behavior. We have used Matlab and Simulink, as it has many built-in functions for the development of signal processing systems. This is enriched by the HDL Coder toolbox, which enables us to rapidly deploy digital logic to an FPGA and validate our approaches in a hardware-in-the-loop setup.
However, the use of Simulink also comes with a few downsides. In order to allow simulations with a high bandwidth, the simulation time steps need to be small (in the order of \SI{1}{\pico\second}), making simulations lengthy and leading to high memory usage requiring an adapted simulation concept.

We use this framework to evaluate different approaches that could achieve the two tasks defined above, implementing different algorithms with both analog and digital components. We are interested in the behavior of different blocks in the receiver chain and their effect on the achievable precision. Hence, we are studying parameters such as the bandwidth limitation in the front end or resolution in the digitization stage. \\

As this study is part of our pursuit to build a generic receiver IC for particle detector experiments, we investigate the influence of changes in signal properties on the achieved precision and accuracy, in order to develop a set of algorithms that is suitable for the use with sensors of different characteristic. We use different signal models, resembling pulses with exponential rise and fall characteristics, emulating pulses with a total charge of \SIrange{0.1}{500}{\pico\coulomb}, a rise time ranging from \SIrange{0.5}{100}{\nano\second} at a total width of \SIrange{1}{1000}{\nano\second}.

In this contribution, we are going to discuss the challenges that arose in the implementation of our tools and present the results of our work. We will be shedding light on the capabilities of widely used approaches like single threshold triggers or constant fraction discriminators, and evaluate more advanced implementations.

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Session Classification: Tuesday posters session

Track Classification: Systems, Planning, Installation, Commissioning and Running Experience