The new readout system of the ALICE Zero Degree Calorimeters in LHC Run 3

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The ALICE Zero Degree Calorimeters (ZDC) provide information on the centrality, time of the collision, vertex position, event plane and luminosity in heavy-ion operation. The operating conditions for the ZDC in LHC Run 3 will be very challenging in heavy-ion collisions, due to the presence of a physical background from electromagnetic dissociation processes with a resulting event rate that could reach 5 MHz in the ZDCs. The ZDC readout system, that was redesigned in order to operate in continuous mode without dead time, is based on a digitizer (12 bit, DC coupled, 1 GSps) in an FPGA Mezzanine Card (FMC) format that will allow a continuous sampling of the 26 ZDC channels combined with the use of an FPGA performing data reduction with the implementation of auto trigger algorithms, pedestal estimations and luminosity measurements. A scheme of the readout system is shown in the figure 1.
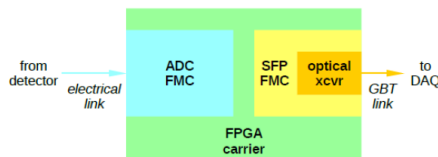

Figure 1:

The FMC is hosted on a VME carrier in order to use existing infrastructure. The digitizer is operated with digital low pass filtering followed by decimation (downsampling technique), with the advantage to reduce noise and generate data throughput at 12 sample/BC. Moreover in order to exploit the full input dynamics of the ADCs (1.0 Vpp), the analogue signals will be shifted by 500 mV. The auto trigger strategy was studied in order to be able to acquire all collisions in triggerless mode without dead time and is based on a differential algorithm in which samples at different times are compared. This trigger algorithm allows to withstand the large dynamics (from a single neutron signal to $\sim$ 60 neutron signal for Pb-Pb collisions) and an interval between consecutive interactions of $\sim$ 50 ns, which is lower than the length of the signal of $\sim$ 60 ns. The firmware architecture for a readout module is summarized in the figure 2. The rate of information for each link is shown as red text, in black the number of lanes multiplied by the bus width, and in blue the data bandwidth. The logic is working at a frequency of $\sim$ 240 MHz (6 times larger than LHC frequency). A GigaBit Transceiver (GBT) link from the Common Readout Unit (CRU) provides commands to configure electronics and data acquisition modes, start / stop commands, synchronization signals, orbit and BC counters. The recovered clock from the GBT link is used to synchronize the clock of the
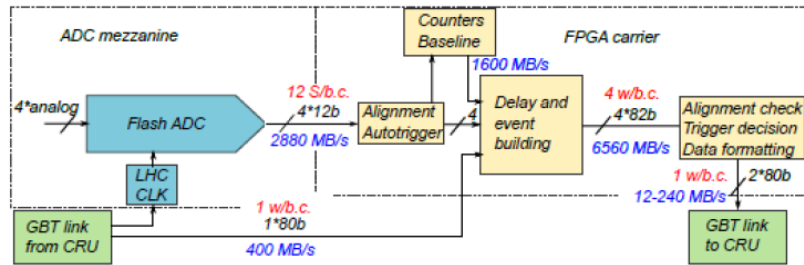
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Figure 2:

digitizer. Digitizer data are aligned with the BC and if the auto trigger algorithm is satisfied data from the corresponding BC is flagged for acquisition. A programmable delay is used to synchronize the digitizer output with trigger information. A FIFO is used to pass the data packets towards the transmission stages after the event selection. A final data processing is related to the data formatting according the protocol required by the ALICE Common Readout Unit (CRU). Finally a GBT link transmits to CRU the triggered BC and previous BC for pedestal estimation. The performance and the architecture of the new readout system will be presented.