PAUL SCHERRER INSTITUT

Development of a CompactPCI-Serial Hardware Toolbox for SLS-2.0

TWEPP 2022

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Abstract

Motivated by large project SLS upgrade and to respond to increasing performance demand (bigger data, faster processing), our electronic and control system experts got the task to evaluate alternatives to our long-lived VME technology. CompactPCI-Serial was chosen as standard platform for building our future embedded control and data acquisition system. We are currently developping two CompactPCI-Serial FPGA boards: UFC, the FMC+ carrier and CIO the communication I/O. Both use the same Zynq® UltraScale+™ MPSoC as processing building block.
These two boards in combination with COTS hardware provide our system engineers the flexibility to build system architectures for various applications with required performance and budget (high-end and/or cost-effective)

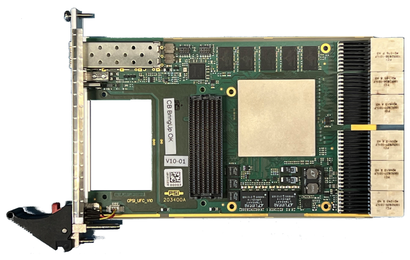
Why CompactPCI-Serial?
Technology trend is shifting from parallel bus architecture (e.g. VME,PCI) to switched serial interconnects (e.g. Ethernet, PCIe).

Very poor communication performance of the **VME** bus, which is far behind today's technology VME does not seem to have a future.

µTCA is modern and promising but has some issues. Its complex shelf management system (IPMI) makes developers and industry reluctant to join this standard. Backplanes interoperability between cards and crates is non-trivial.

CPCI-Serial offers comparable performance and functionality as uTCA but with much less complexity.
- Not need an MCH to operate. Well-established and widespread technologies, namely Ethernet and PCIe.
- Expectation that this platform keeps up with the technology advances and the user demand.
- A larger variety of industrial powerful and cheap CPU cards are available on the growing market.
- The standard allows mixing commercial components and customized hardware in the same system. For example, I/O cards communicate with central CPU via PCIe (or Ethernet) while high-end FPGA boards exchange data via gigabit links on the same backplane.
- PSI internal know-how is available.
- CPCI-Serial based data acquisition systems have been already developed and deployed (e.g. in SINQ).
- High potential for synergies at PSI

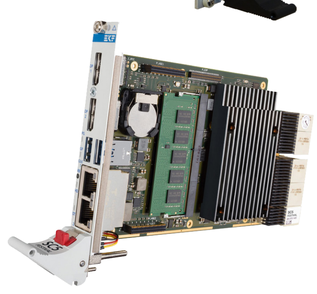
We are acquiring momentum in building our CPCI-S portfolio to cover good range of applications



Open CPSI_UFC
- FMC+ Carrier
- High performance, real-time Control & DAQ
- Application: LLRF, eBeam Instrumentation

Open CPSI_CIO
- Serial data processing and communication (10 Gbps)
- Cost-performance efficient hardware
- Applications: timing, streaming, serial I/O

RTM_DAC
- Rear Transition Module with 500 MHz DAC & digital I/O
- Application: LLRF



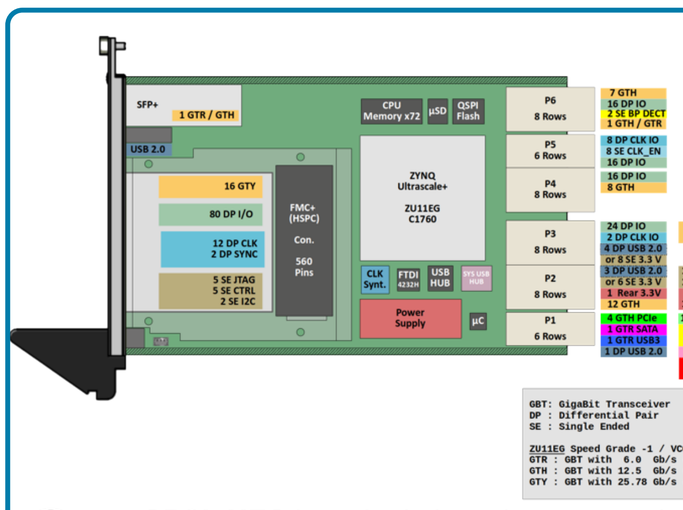
SC5-FESTIVAL (COTS)
- System CPU, Intel Xeon(R) 3.00GHz, Quad core, 16 GB RAM
- Application: General control system, computation, memory intensive applications

FMC AD3110 (COTS)
- ADC 16-bit 250 MSPS
- Application: LLRF, eBeam diagnostics

FMC217-Fast Digitizer (COTS)
- 12-bit ADC @ 6.4 GSPS,
- 16-bit 1xDAC @ 12 GSPS
- Application: Filling pattern

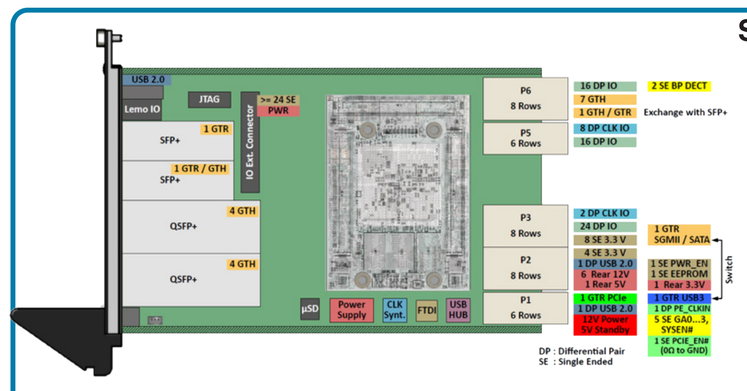
TXMC635 (COTS)
- Low-medium performance low-cost DAQ and I/O
- Applications: Beamlines, slow control, slow DAC & ADC measurements DC to few kHz.

Processing Boards
Two boards with different performance level using same family of Zynq® UltraScale+™ MPSoC with common user I/O pinout allows compatible RTM's and compatibility from a software and firmware point of view.
Multiple cards are synchronized by means of Multi Gigabit Transceivers (MGT). The link topology is fully programmable through the FPGA fabric.



Status:
- First prototypes fully tested
- 10Gb/s Backplane interconnect tested Ok.
- 26 GB/s transmission between FPGA & FMC Ok
- Second Revision in house for final testing
- Serie production end 2023

Open CPSI_UFC is a single board computer designed around the Zynq® UltraScale+™MPSoC (Multi-Processor System on Chip). This implementation enables Linux RT, high-speed applications and safety applications on one single peripheral card. The board implements a PCIe x4 Gen2 interface both as a master and slave.This board supports FMC+ mezzanine cards.The board can be used in system slot as system controller, and has GB links connected to all others slots over the backplane (full mesh).

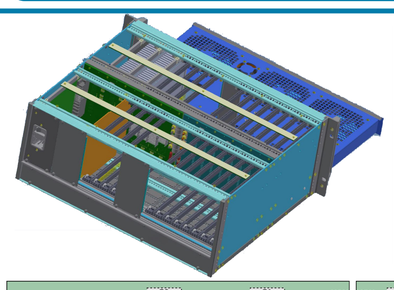


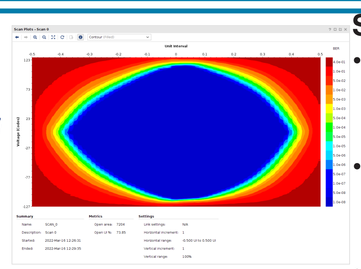
Status:
- First prototypes fully tested
- Second Revision redesign pending
- Features for Timing System, event forwarding and detection tested

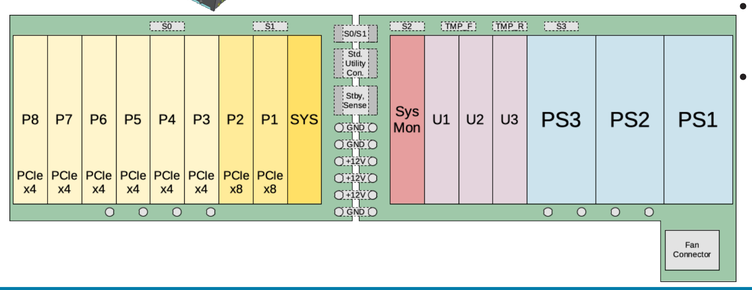
Open CPSI_CIO is a single board computer designed around the Zynq® UltraScale+™ MPSoC (Multi-Processor System on Chip).The design is implemented with an Enclustra XU1-6CG System-on-Module. This board is specially dedicated to systems interconnect and timing management, with 10 QSFP/SFP+ front connect modules and GB links connected to the backplane. This board can be used as generic data stream processing plattform.

CPSI-S Crate (COTS)/Custom
- Scalable Power Supply: up to 3 PSU
- .Optimized cooling
- Front/Rear temp monitor
- Rear lenght extension

The CPCI-standard defines communication protocols and signal levels between boards as well as the electrical and physical dimensions of the peripherals. In order to guarantee maximum compatibility of customs RTMs, we define the pinout of the free users I/O (CPSI-S). We also separated the power from the CPCI-S backplane to implement 3 user slots, a monitor card and an additional redundant power supply module.

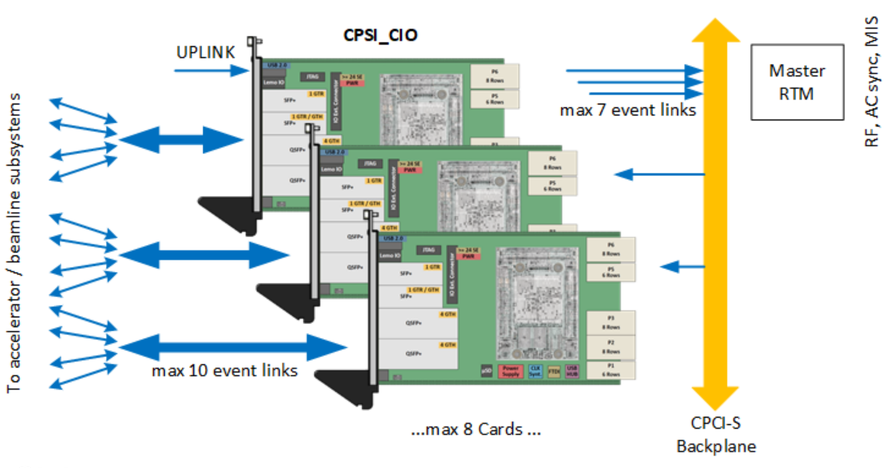




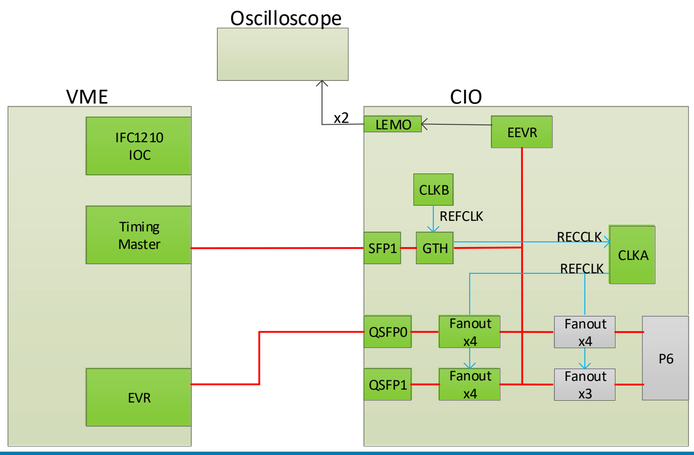


Status:
- Improved Backplane has good Signal Integrity (10 Gbps)
- Improved Power-Supply available – testing in progress
- All critical testing done June 2022
- Backplane is released for manufacturing All critical material ordered or on ELMA stock, expected late 2022

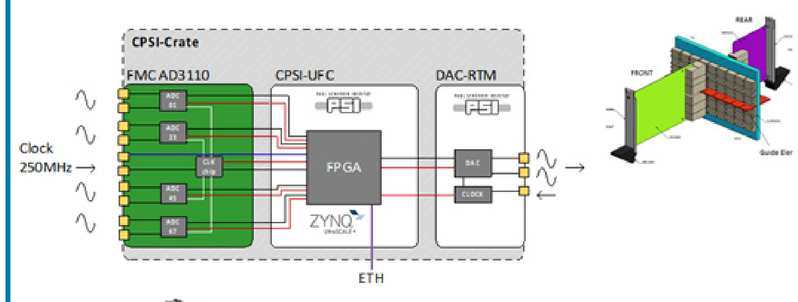
SLS2.o Timing
Master, Distribution, Receiver

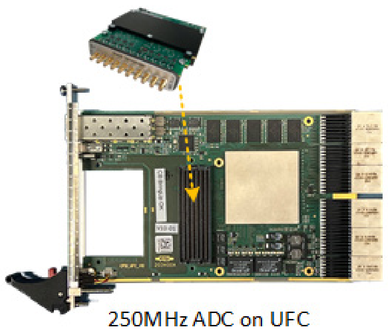


Status
- Tested Embedded EVR
- Implemented Timing Fanout with 1 uplink and 15 downlinks
- 8 dowlninks on thefront panel tested
- 7 downlinks on the backplane not tested
- Clock recovery tested
- Clock jitter cleaner tested



LLRF application with CPCI-S Tools
Low latency control loops
- IN/OUT propagation 112 ns
- LLRF control loop latency below 1uS
- ADC: 16-bits @250MHz
- DAC: 16-bits @500MHz





250MHz ADC on UFC

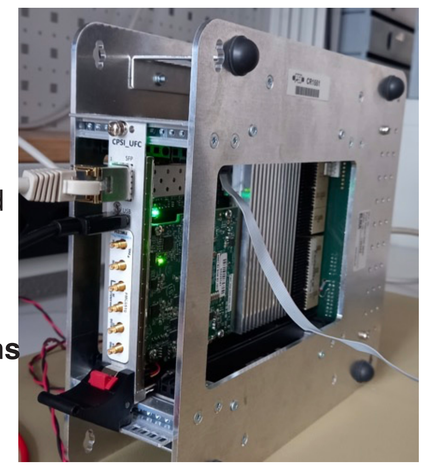
DAC 500MHz (rear transition module)

Status:
- CPCI-S hardware in action
- Characterization of ADC and DAC successfully done!
- Application firmware is being implemented

Fast Digitizer (ADC+DAC on CPSI_UFC) Vadatech FMC217

Status
- Reference project ported on the UFC-Board
- First ADC data @6.4GS/s acquired
- First DAC data @12.4GS/s generated

Planned applications
- General purpose fast scope
- Filling Pattern Monitor for SLS2



Firmware and embedded software for board support package and low level testing are operating. BSP library is growing. The use of the same Zynq® UltraScale+™MPSoC family allows reuse of code for development and test benches and reduce the engineering effort.
Epics implementation is done and operational for both processor boards. Common processing architecture and embedded Linux allows easy integration of EPICS to run locally on the plattforms.

Future HW development activities:
- Crate monitor development
  - Signal conditionning board
  - Smaller crates with reduced number of slots