The readout system for the tracker of the High-Energy Particle Detector on board the CSES-02 satellite

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(on behalf of the CSES-Limadou collaboration)

TWEPP 21/09/2022

Outline

- The Limadou Project
  - The Lithosphere–Ionosphere Coupling.
  - The China Seismo-Electromagnetic Satellite (CSES)

- The High Energy Particle Detector 02 (HEPD-02) part of CSES-02
  - Overview of the High Energy Particle Detector (HEPD-02).
  - The HEPD-02 silicon tracker and its readout system.

Limadou Project

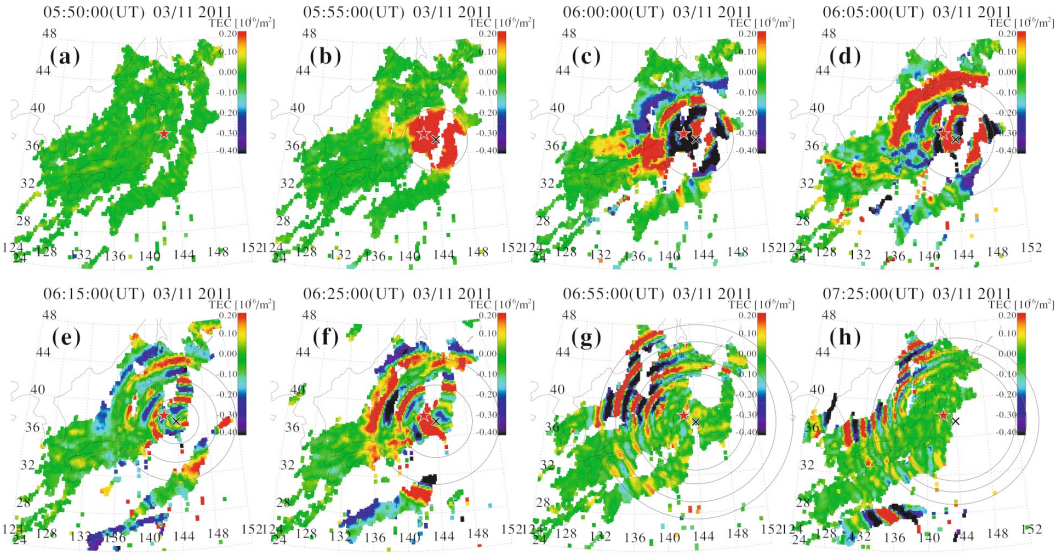
The Limadou project is a Chinese-Italian collaboration to build a constellation of satellites to monitor electromagnetic field and waves, plasma and particle perturbations in the magnetosphere.

- CSES-01: launched in 2018 and operative
- CSES-02: projected lunch date around 2023
- Further satellites under discussion

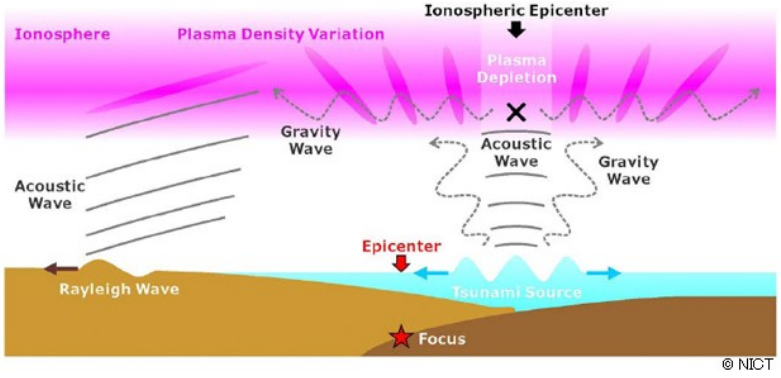
LIMADOU 利玛窦

Seismo-Electromagnetics

Seismo-Electromagnetics is the field studying the Litho/Atmo/Iono/Magnetosphere coupling.



T. Tsugawa et al. DOI: eps.2011.06.035



CSES-02

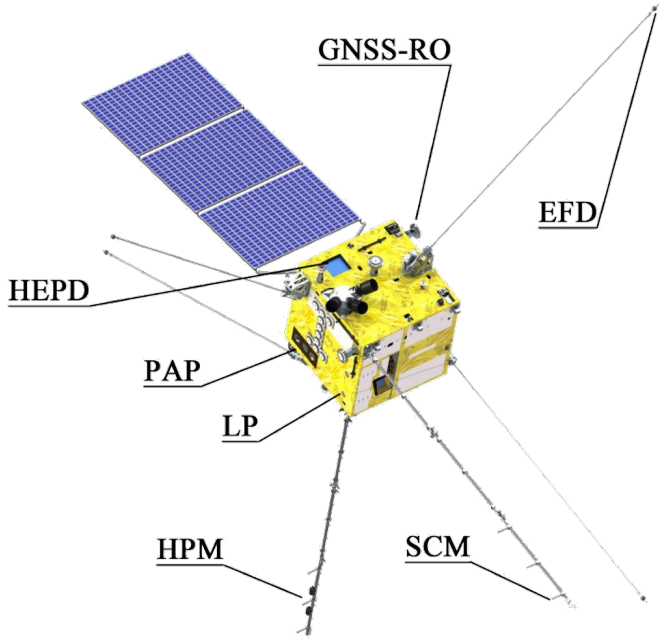
The China Seismo-Electromagnetic Satellite (CSES) is designed to perform precise correlated measurement of EM fields and particle fluxes.

Instruments:

- EM fields detectors (EFD, HPM, SCM)
- Plasma physics (LP, PAP)
- Particle detectors (HEPD, PAP)

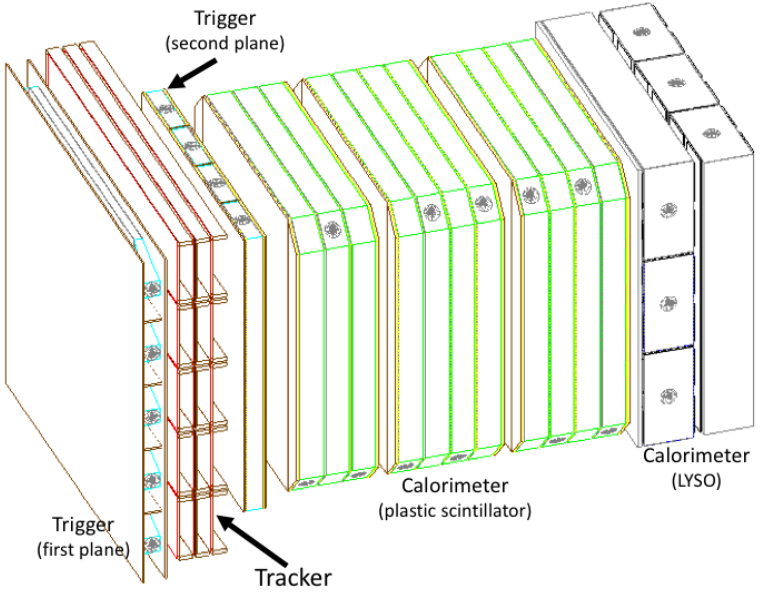
Fields of interest:

- Lithosphere-ionosphere coupling
- Solar Physics (space weather)
- Cosmic ray fluxes



HEPD-02

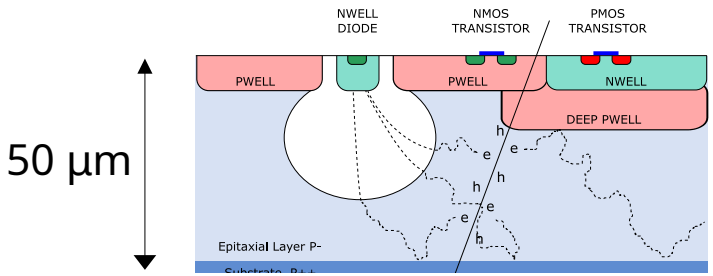
High Energy Particle Detector (HEPD-02) to measure fluxes of trapped particles in the magnetosphere in the 3-150 MeV range for electrons and 30-300 MeV for protons.

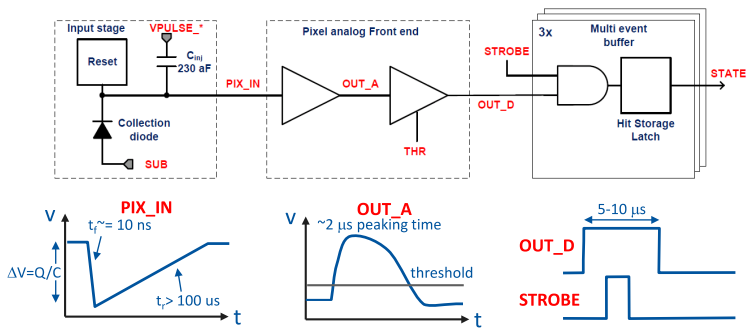


- 3-planes detector tracker based on the MAPS pixel sensors.
- Two layers of crossed trigger bars, aligned with the tracker turrets.
- 11-tiles plastic scintillator
- Two layers of LYSO scintillators.
- Structure surrounded by veto detectors.

ALTAI sensor

The ALTAI sensor is a CMOS Monolithic Active Pixel Matrix sensor (variant of the ALPIDE sensor developed by the ALICE collaboration for the LHC LS2 upgrade).





- 15×30 mm^2 sensor composed by a 1024×512 pixels matrix
- ~30 µm pixel size.
- Readout circuit implanted on the same substrate of the active area.
- Each pixel generates a binary output (hit/no-hit) after a trigger command.

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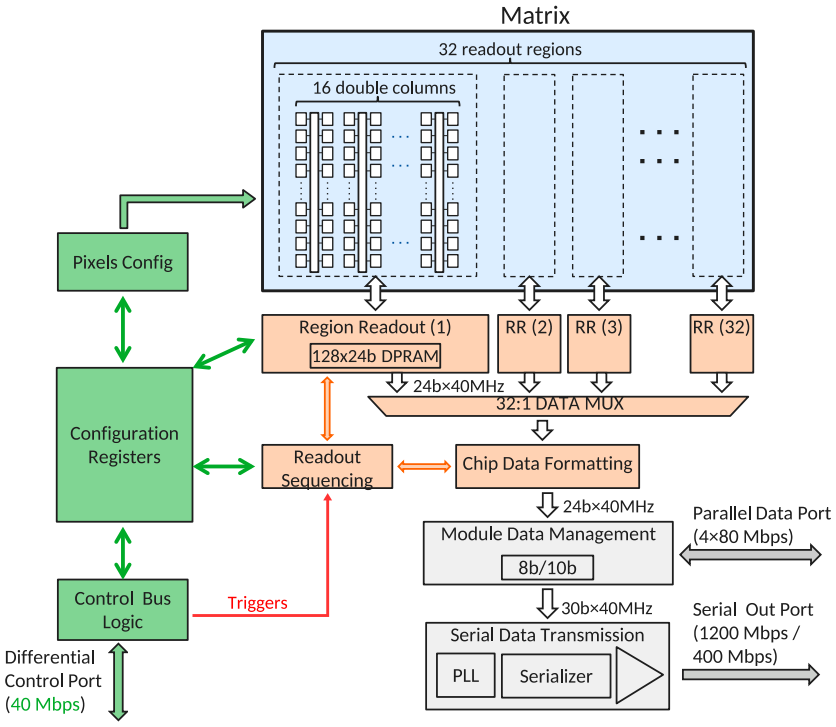
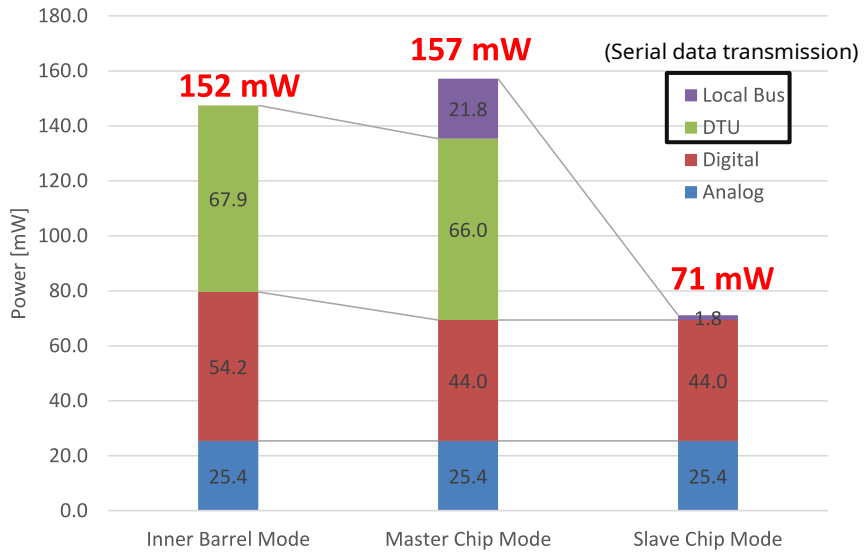


- Readout performed on groups of two columns, with zero suppression and efficient cluster coding.
- Fast readout port (up to ~1.2 Gbps) + Parallel port for local bus (daisy chain configuration 1 master + max 6 slaves).
- Control port offering a slow readout side-channel (~3-5 Mbps data rate).

Power Consumption Reduction

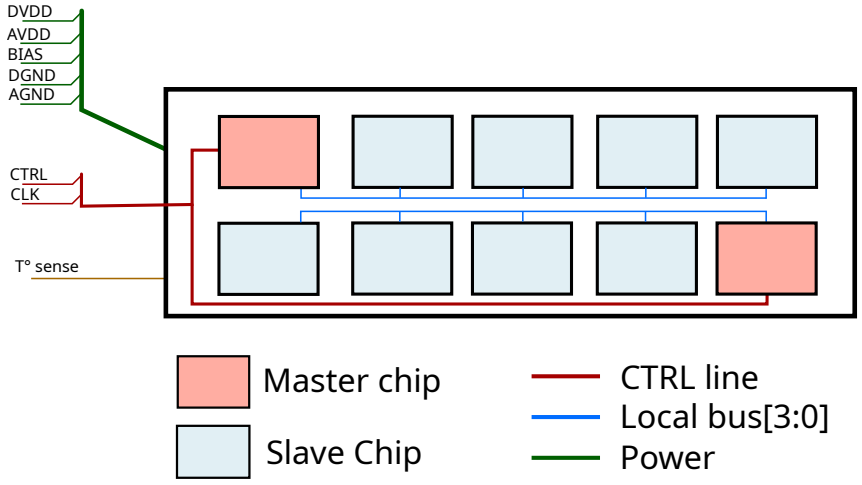
The tight power budget available requires the development of a custom tracker readout system:

- Readout is performed from the chip slow control port.
- Use of clock gating.
- Modular structure to implement a sparse readout.



Stave structure

The basic unit of the tracking detector is a stave with 10 chips (2 master with 5 slaves each)



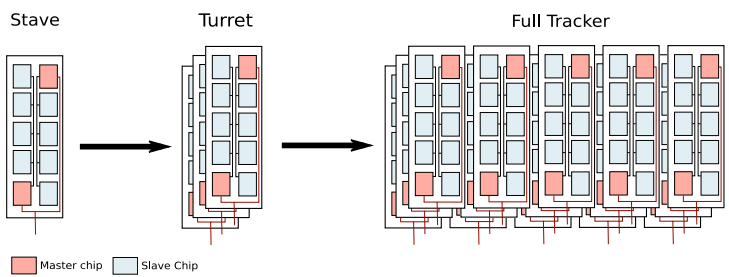
- The high speed serial line on the two master is not connected.
- The two masters share the same CTRL line, used for the readout of the entire stave.

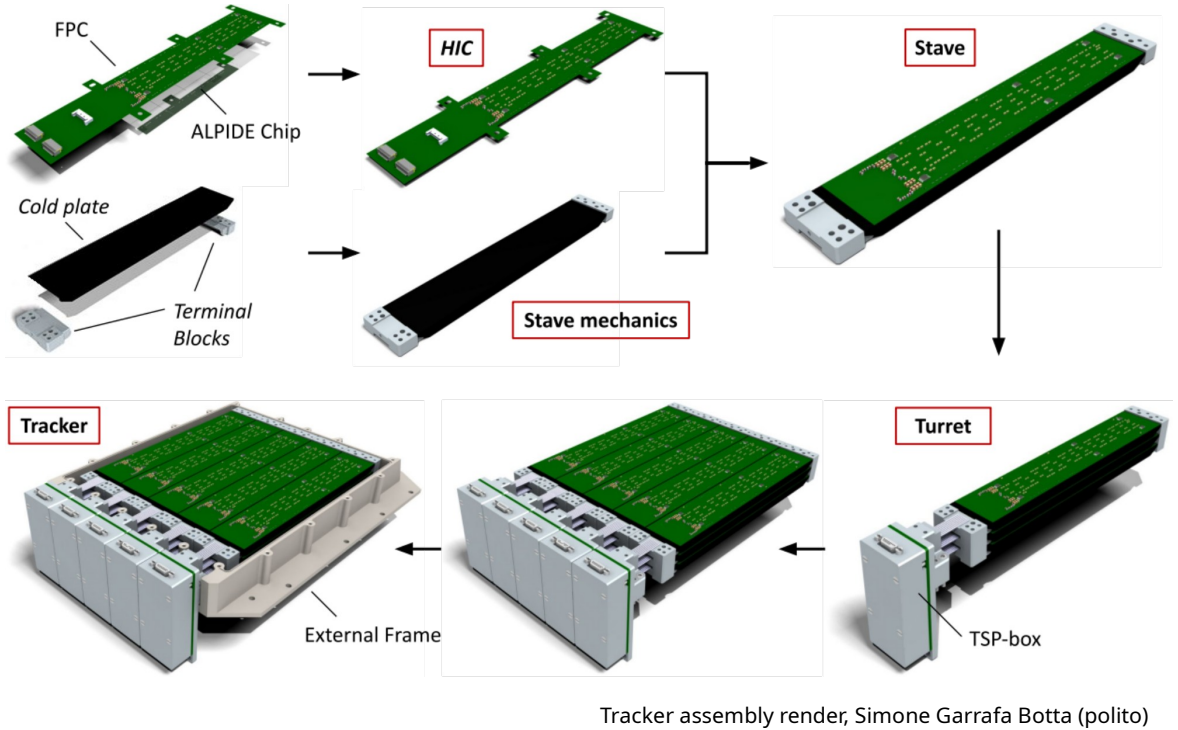
A single CTRL line shared for the entire stave is acceptable considering the expected event rate: max ~100-200 bytes @ ~400 Hz typical, ~1 KHz peak.

Tracker

The tracker is divided in 5 turrets aligned with the trigger bars.

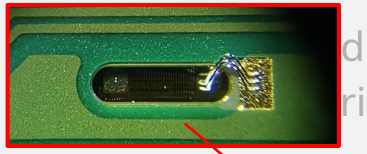
Each turret is composed by piling 3 staves.



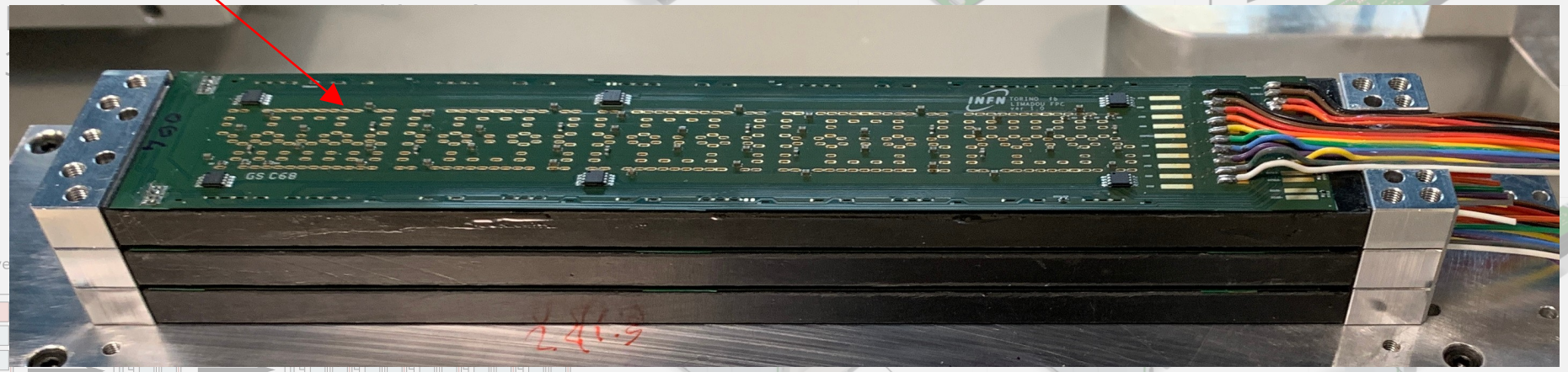


Tracker assembly render, Simone Garrafa Botta (polito)

Tracker



ded in 5 turrets
rigger bars.



Tracker assembly render, Simone Garrafa Botta (polito)

Tracker

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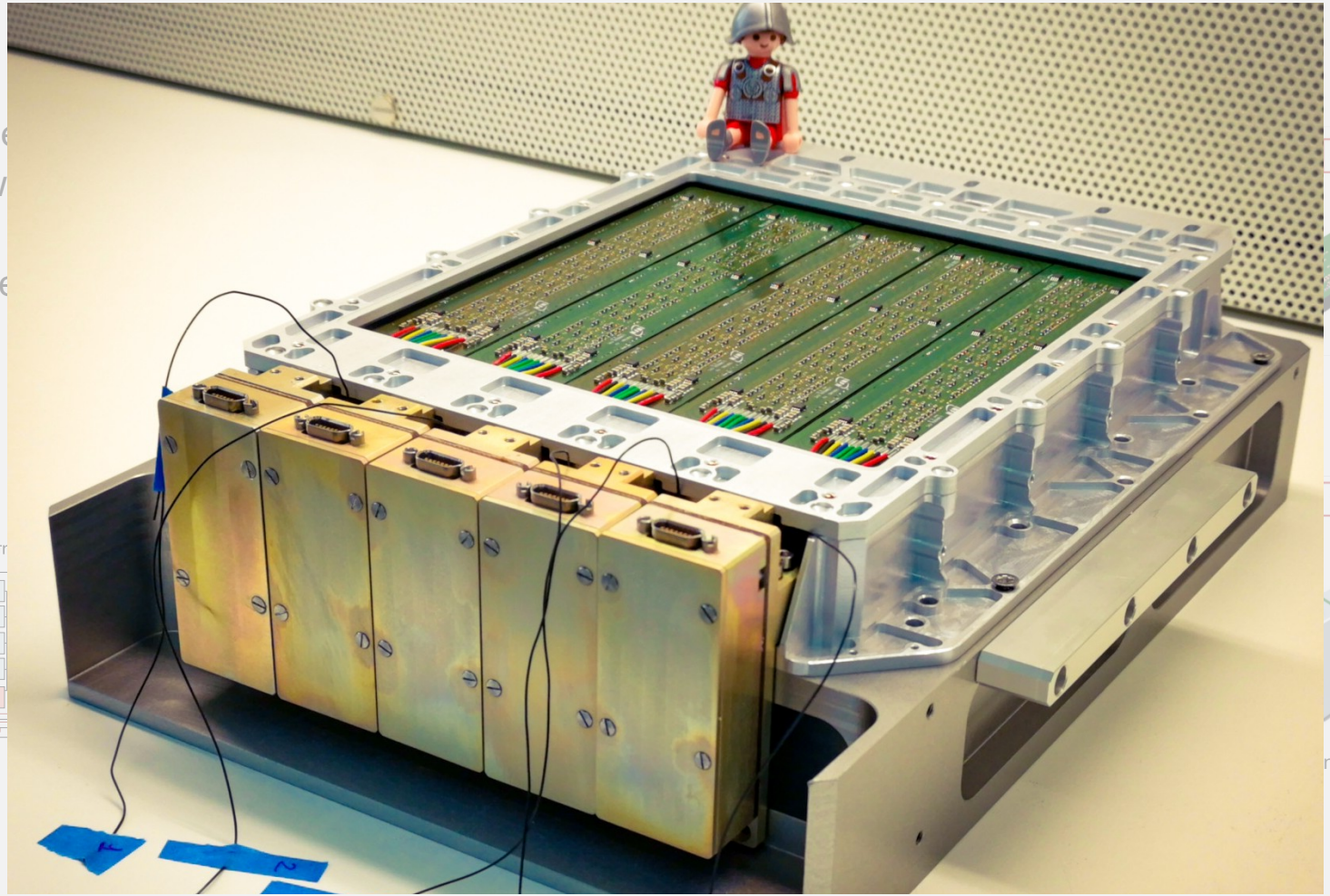
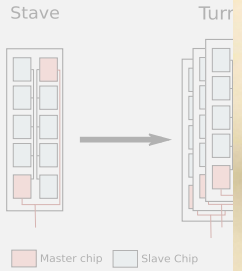
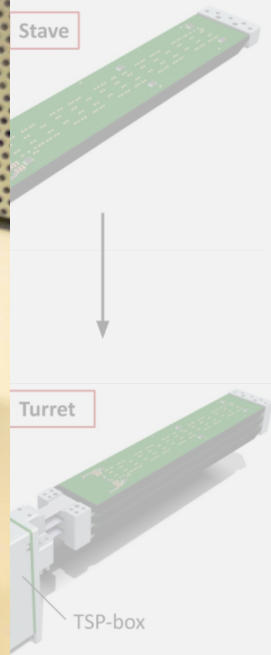
Each turre
3 staves.

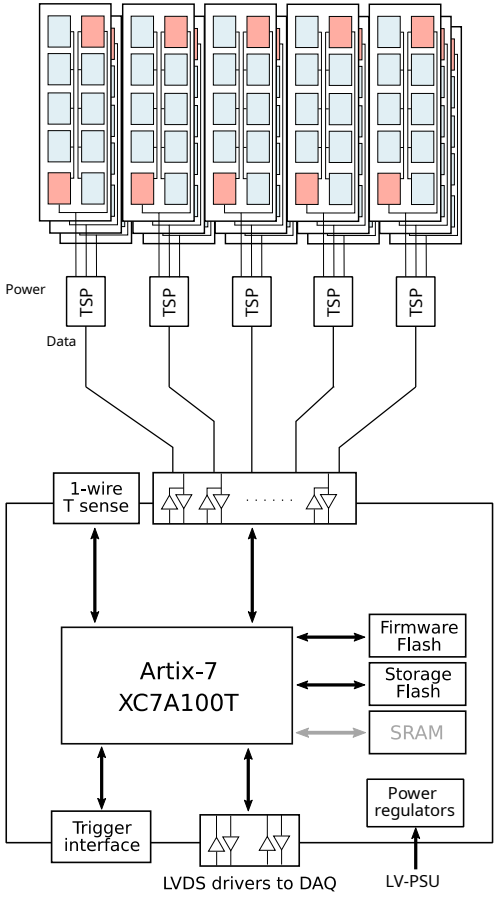






ne Garrafa Botta (polito)

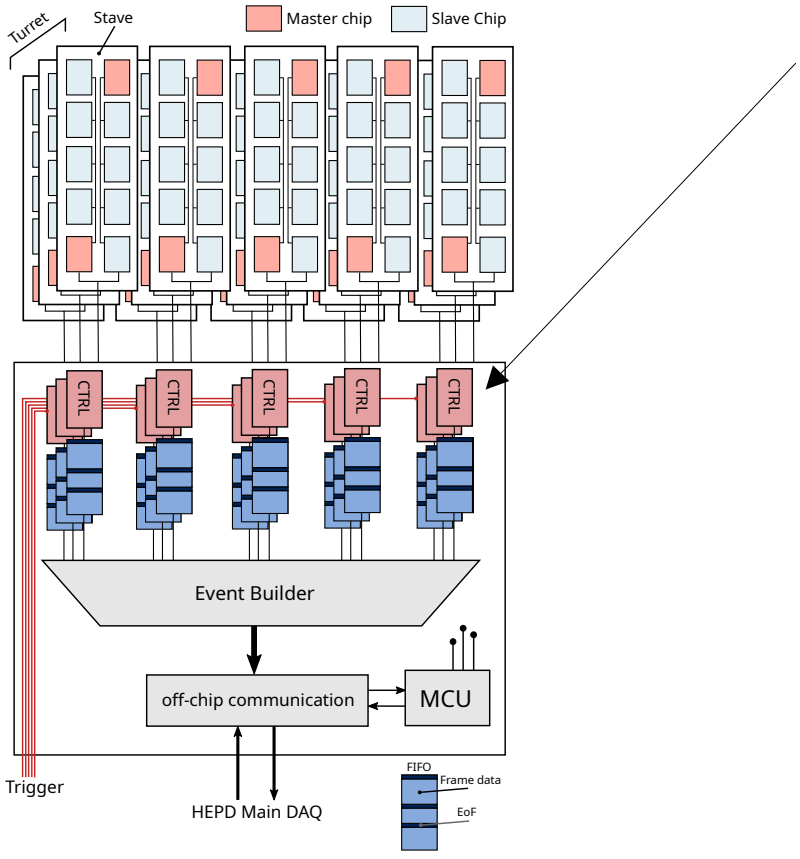
Tracker DAQ Board



The entire tracker is managed and read out by a “Tracker DAQ” board.

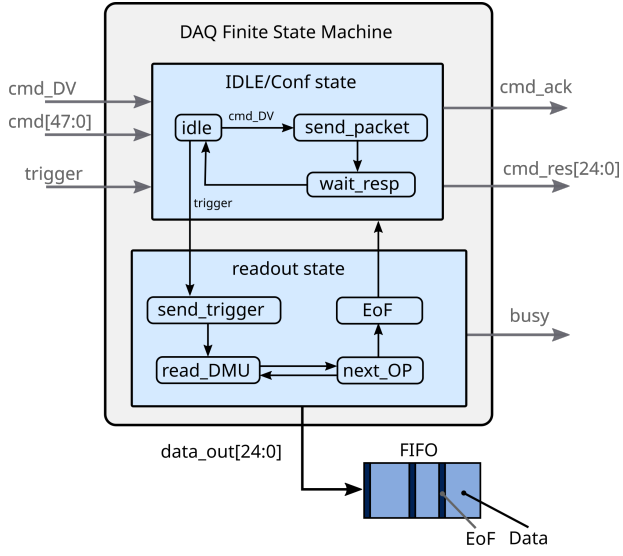
- Single low-power FPGA.
- 3x differential LVDS Control lines for each tower + 1 clock line for each turret.
- Spacewire connection with HEPD main DAQ.
- 5 trigger lines + busy output.

Firmware Implementation

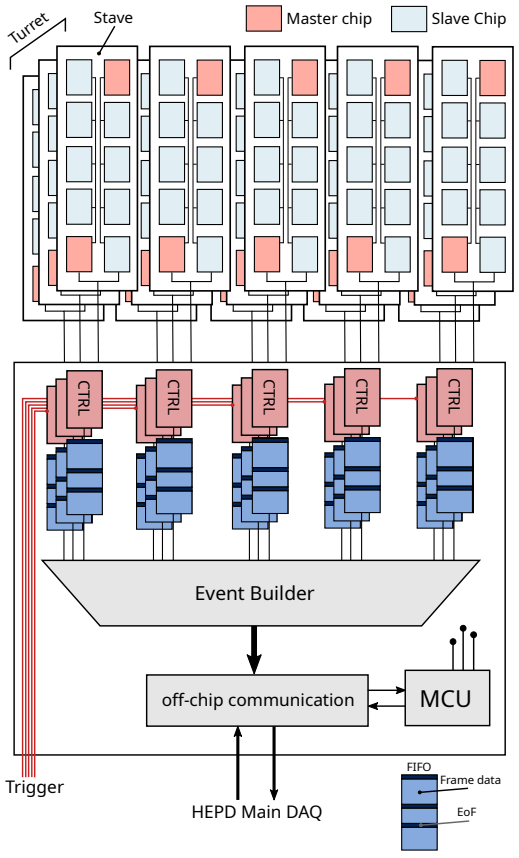


(x15) CTRL stave readout cores:

- Handle commands to the staves.
- Implements a readout FSM.
- Additional zero-suppression.

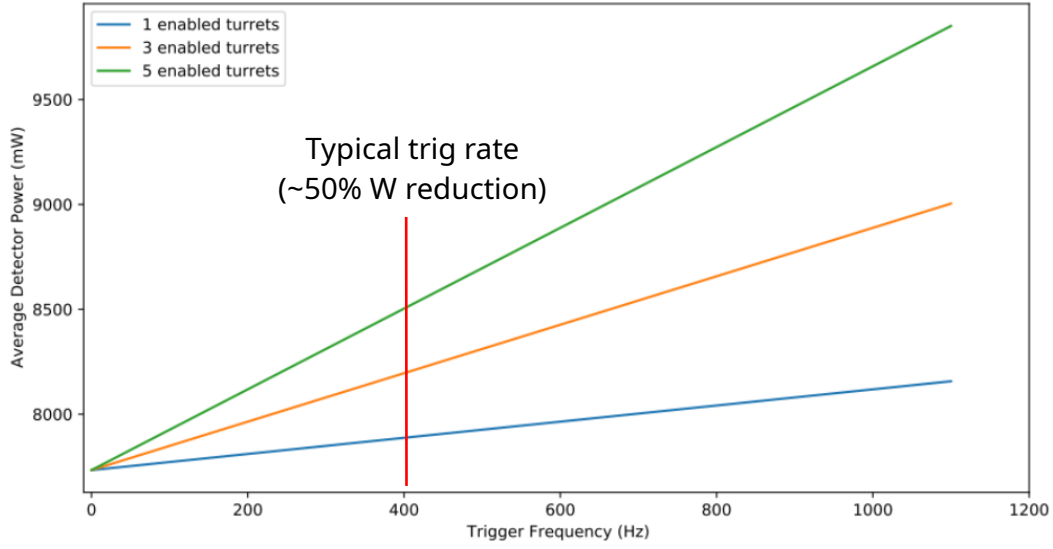


Firmware Implementation

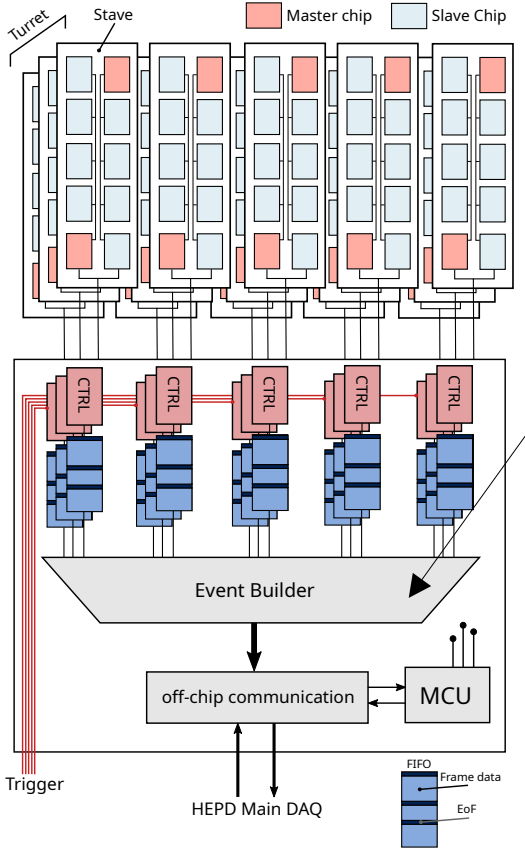


Sparse readout of the tracker and use of clock gating to save power:

- Clock signal is provided to a turret only when a trigger is received and then disabled after readout.
- Typically only 3 turrets are enable at a given time.

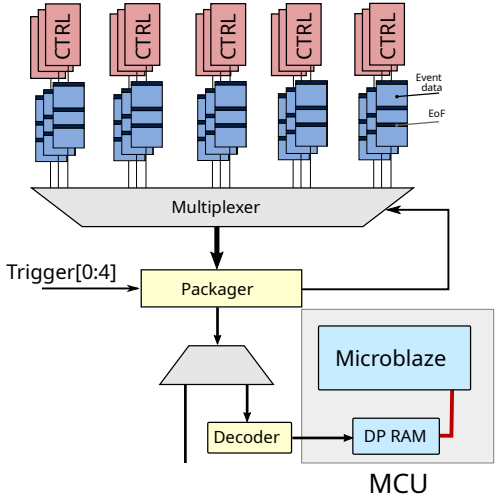


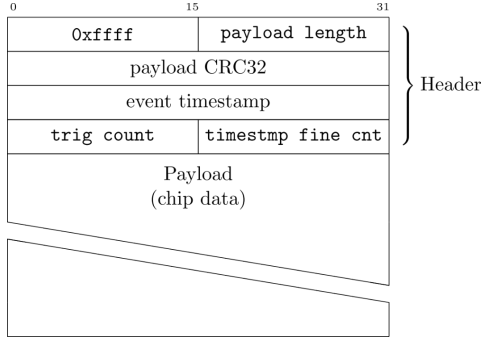
Firmware Implementation



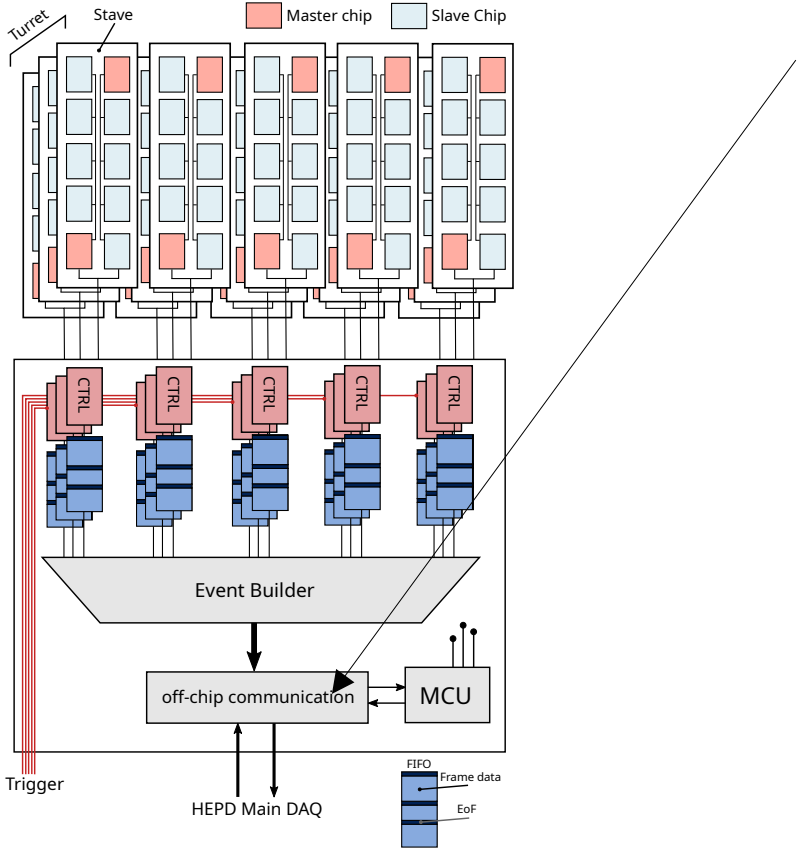
Event packaging:

- Generation of an event package.
- Data is transmitted or decoded and passed to the CPU (for calibration)



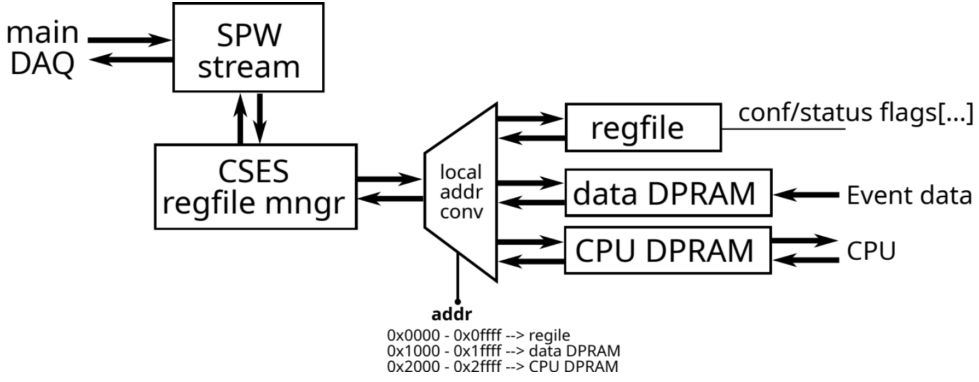


Firmware Implementation

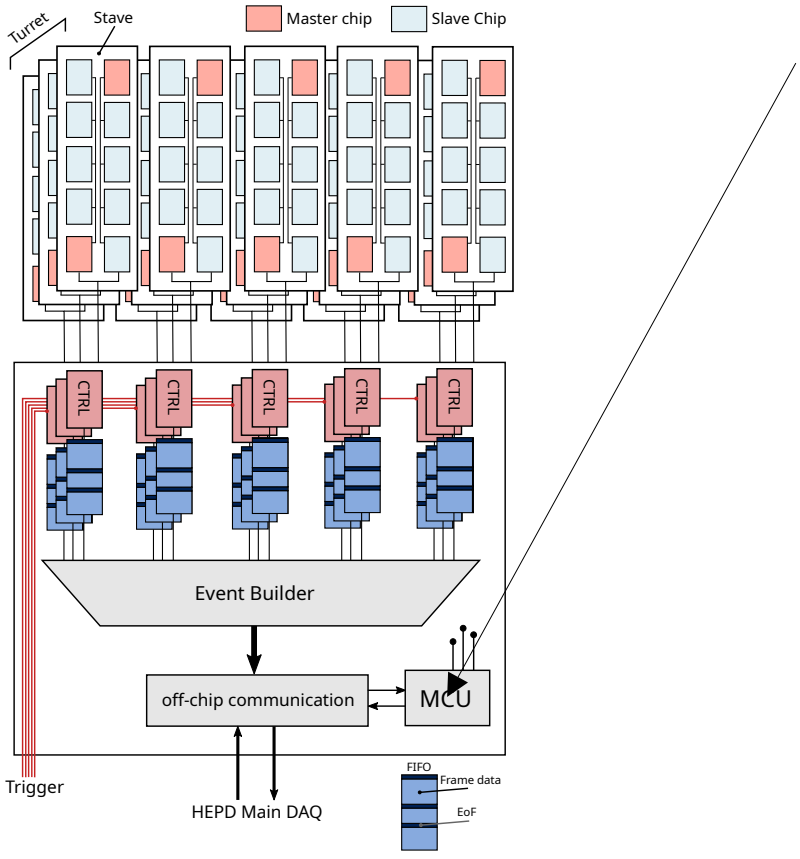


Data and commands transmission:

- Custom protocol based on a “spacewire-light” link.
- Access to shared DPRAM regulated with simple flags.

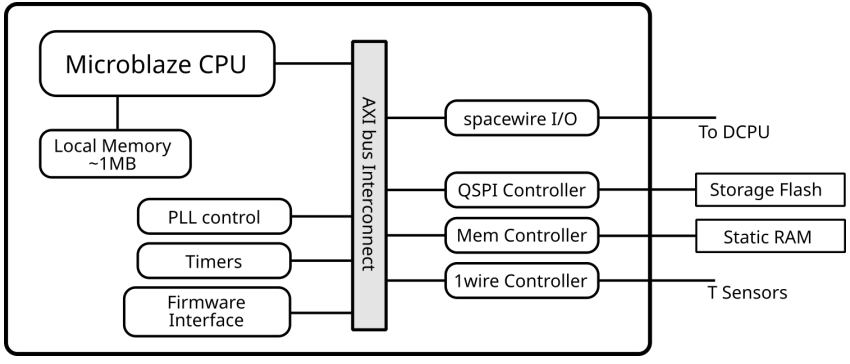


Firmware Implementation

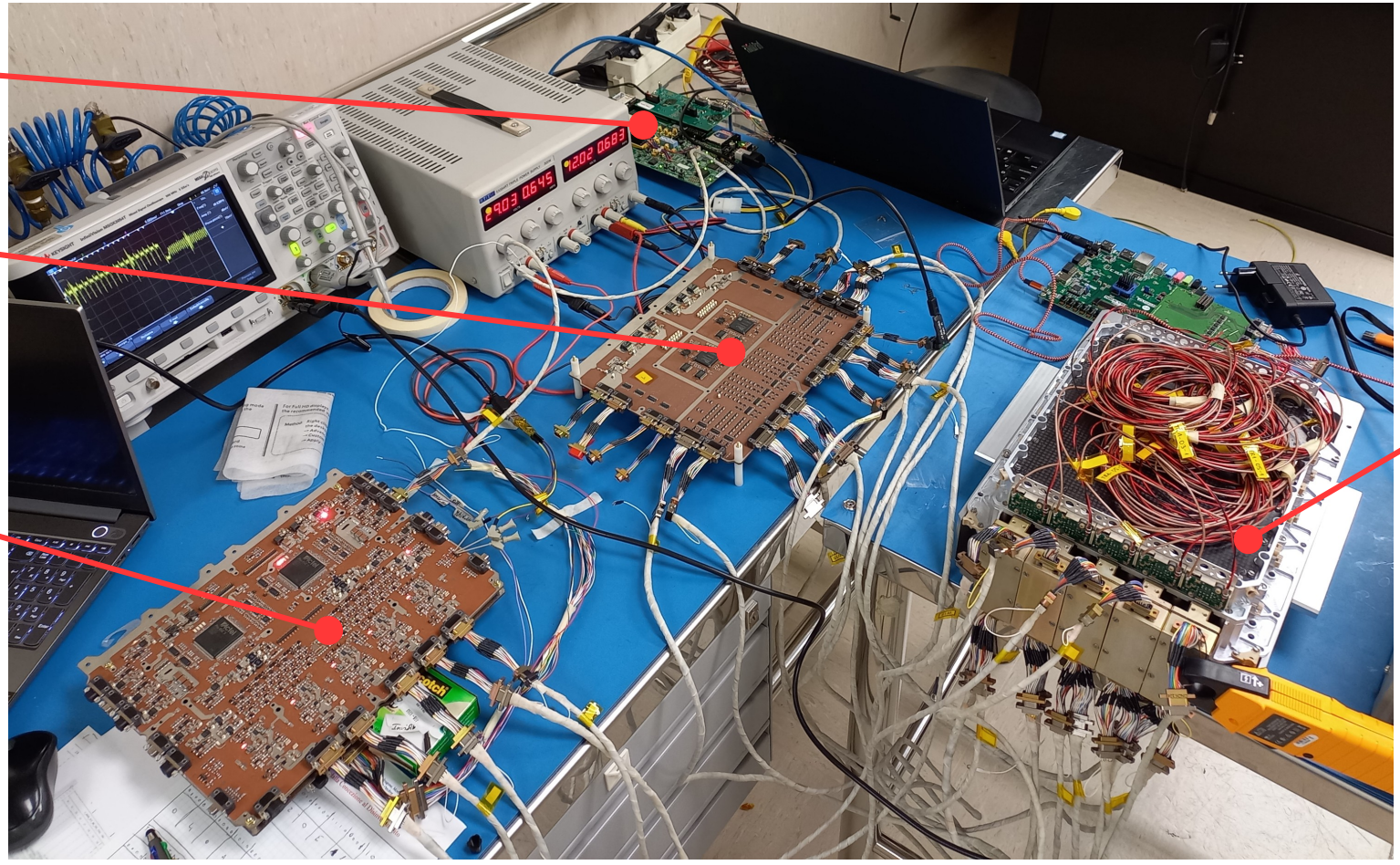


Micro-Controller Unit:

- Based on a Xilinx Microblaze soft-CPU.
- Implement routines for configuration, calibration, and gather telemetry data.



Tracker Subsystem Integration Testing



Conclusion

- Developed a readout system to fit the CSES-02 mission’s constraint.
  - Sparsified readout of the tracker.
  - Efficient test and calibration procedures.

- HEPD-02 integration in the final stages.
  - Testing and beamline characterization to begin soon.
  - Launch expected between end of 2022 and begin of 2023.


Thank you