# Commissioning and running experience with the CMS GE1/1 system

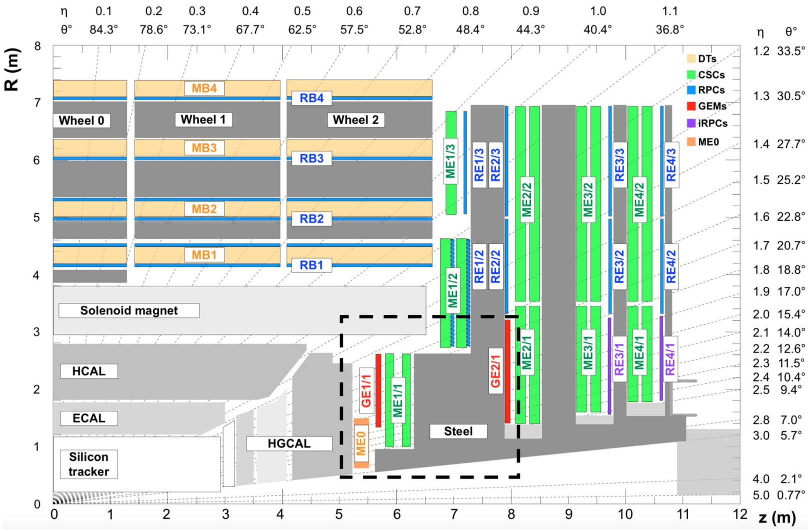
Laurent Pétré, on behalf of the CMS Muon Group

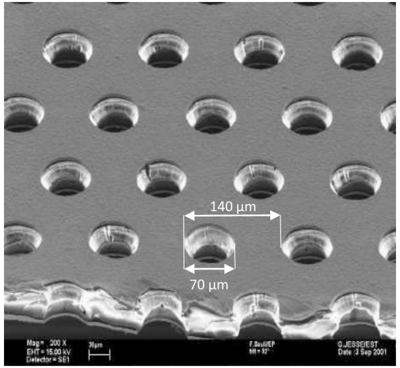
TWEPP 2022: Topical Workshop on Electronics for Particle Physics
19-23 Sept 2022 - Bergen, Norway

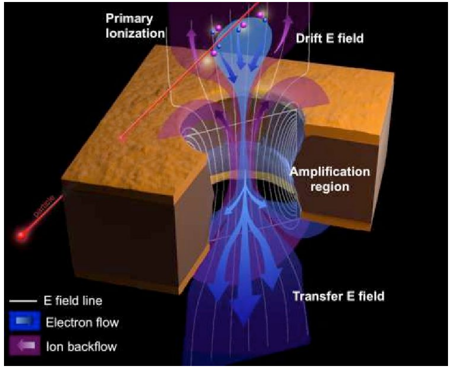
# The CMS GEM upgrade project

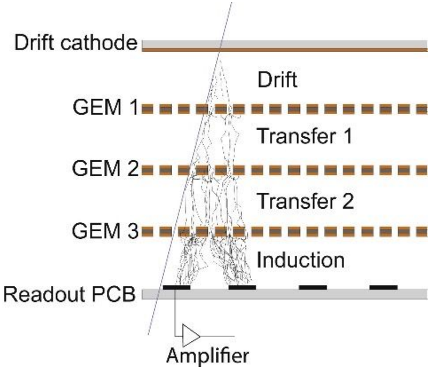
The CMS GEM project is part of the CMS upgrades preparing for the high-luminosity LHC phase. New detectors based on the Triple-GEM technology are being installed in CMS to cope with the increase in **background rates (up to 150 kHz/cm²)** and trigger requirements.

Triple-GEM detectors, gaseous micro-pattern detectors, meet the environmental and physics requirement in terms of time and spatial resolution, efficiency, and rate capability as well as robustness against aging. The CMS GEM detectors are unique due to their **large size (20-40 cm x 130 cm)**, the operation in **magnetic field (~3T)**, and the expected luminosity.




- High rate capability: **up to O(MHz/cm²)**
- Efficiency **> 97%**
- Space resolution ≈ **300 μm**
- Time resolution ≈ **8 ns**
- Gas mixture: **Ar/$CO_2$ 70/30**

# The Phase-I upgrade : GE1/1

Decade-long project whose installation finished in Sep 2020:

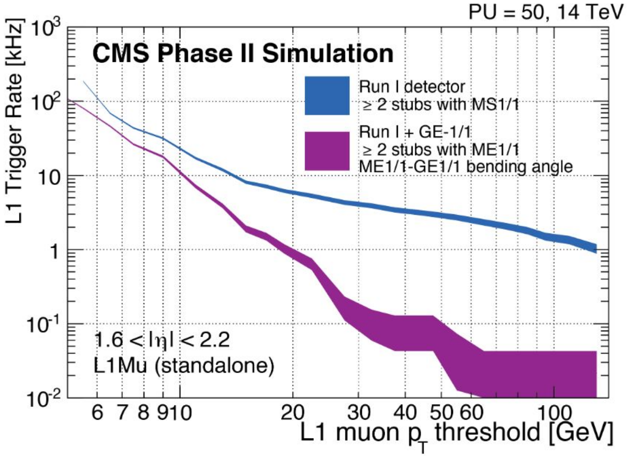
- “Slice test” installed beginning of 2017
- Mass production started in Oct 2017

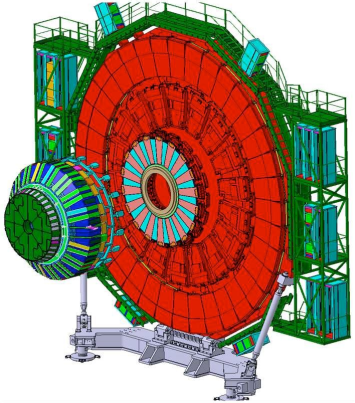
Main goal: improve the muon momentum measurement in the CMS Level-1 trigger within a single GEM+CSC station.

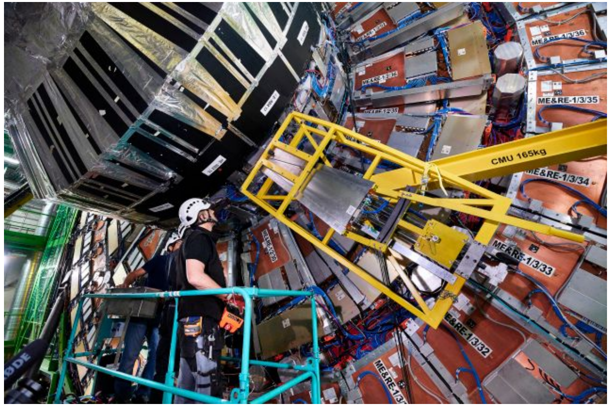
**GE1/1’s 144 chambers are now routinely used in CMS data-taking and still undergo active commissioning activities.**

A few numbers:

- Pseudorapidity |η| coverage: 1.55-2.18
- 36 super-chambers per endcap
  - 2 layers per super-chamber
- 144 chambers (72 shorts + 72 longs)
  - Chamber angular opening: ~ 10°
  - Overlap between adjacent chambers
- 442,368 readout channels

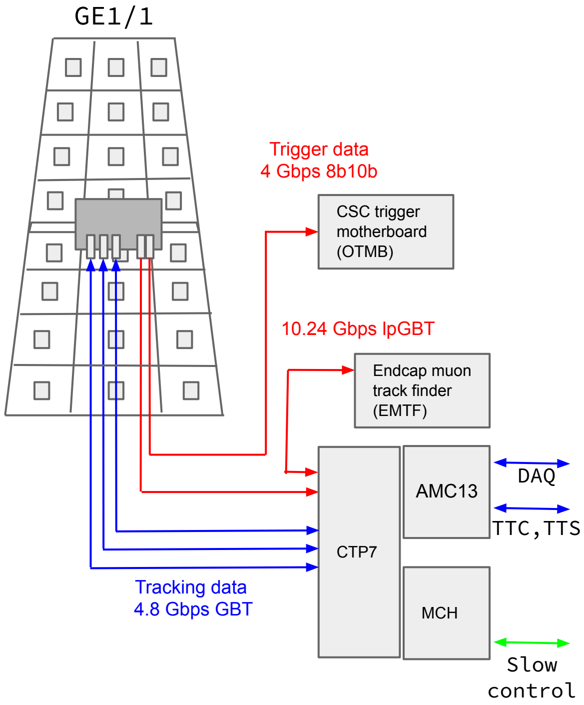


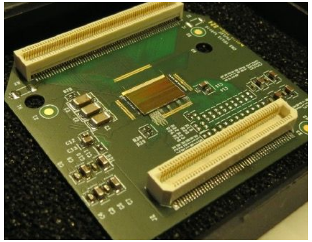






| Jul 2019 | Negative end-cap installation | Oct 2019 | Jul 2020 | Positive end-cap installation | Sep 2020 |
|---|---|---|---|---|---|

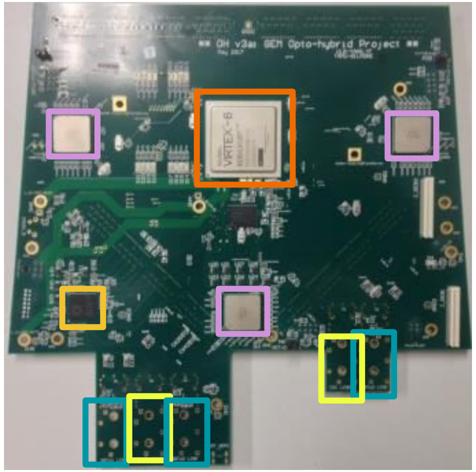
# The GE1/1 electronics



3456 **VFAT3** - Custom ASIC - 24/chamber

- 128 binary channels readout
- Preamplifier + shaper + CFD
- Synchronous trigger data
- High granularity tracking data sent upon L1A (Level-1 Accept)
- Built-in calibration circuit



144 **OptoHybrid** - Data concentrator board

- Virtex-6 for trigger data compression
- 3 GBTx + 3 VTRx for communication with the counting room
- 2 VTTx for trigger data transmission
- 1 SCA for board monitoring

12 **CTP7** - µTCA AMC module

- Virtex 7 FPGA with Zynq SoC
- Handles event building, slow controls, and fast controls (trigger/clock distribution to front-ends)
- Handle up to 12 OptoHybrid

# A noise issue

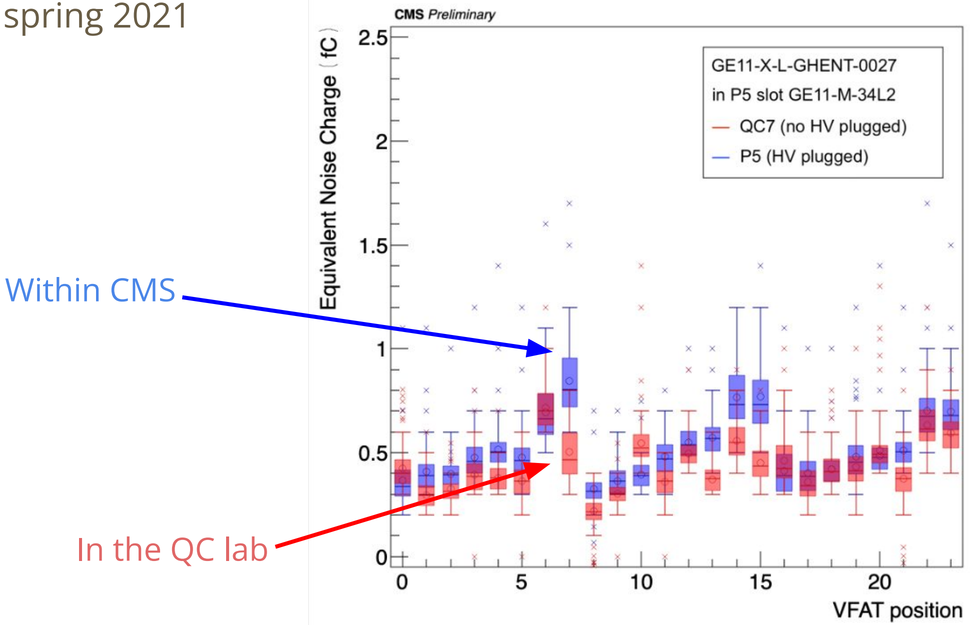
High levels of electronics noise (> 1fC) in the detector were measured in 2020 during early commissioning and confirmed at the end of the installation:

- Significantly higher than during the quality control (QC) steps in the lab
- Would have pushed up the thresholds and impacted the detection efficiency

Carried on an extensive investigation campaign in spring 2021 to reduce the noise to acceptable levels (< 1fC).

A variety of hypotheses were studied:

- Environmental factors (CSC, HCAL)
  no impact
- Impact of the high-voltage system
  no impact
- Impact of the low-voltage system
  **group effect linked to the cables**
- Interaction between GE1/1 chambers
  no evidence
- Interaction between GE1/1 super-chambers
  no evidence

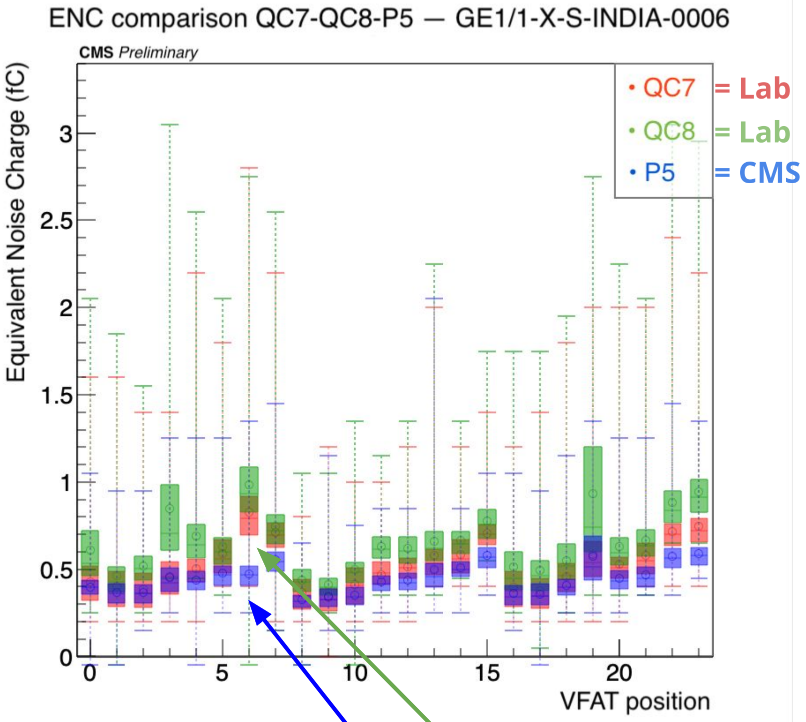


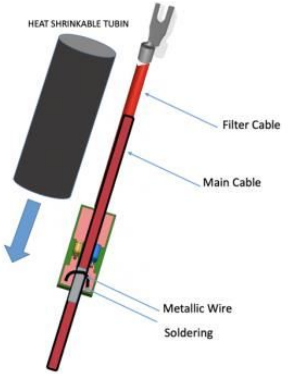
# A noise solution

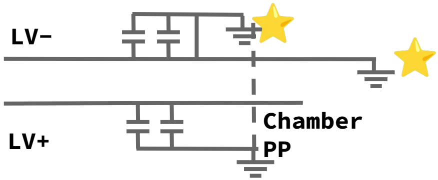
Implemented two solutions:

- Installation of LV “filters” at the chamber level
  - Improvement of the connection to ground
  - Addition of a decoupling capacitor
- Addition of a filtering capacitor in the LV power supply

At the end of the modifications in May 2020, the electronics noise level reached <1 fC on most of the chambers.



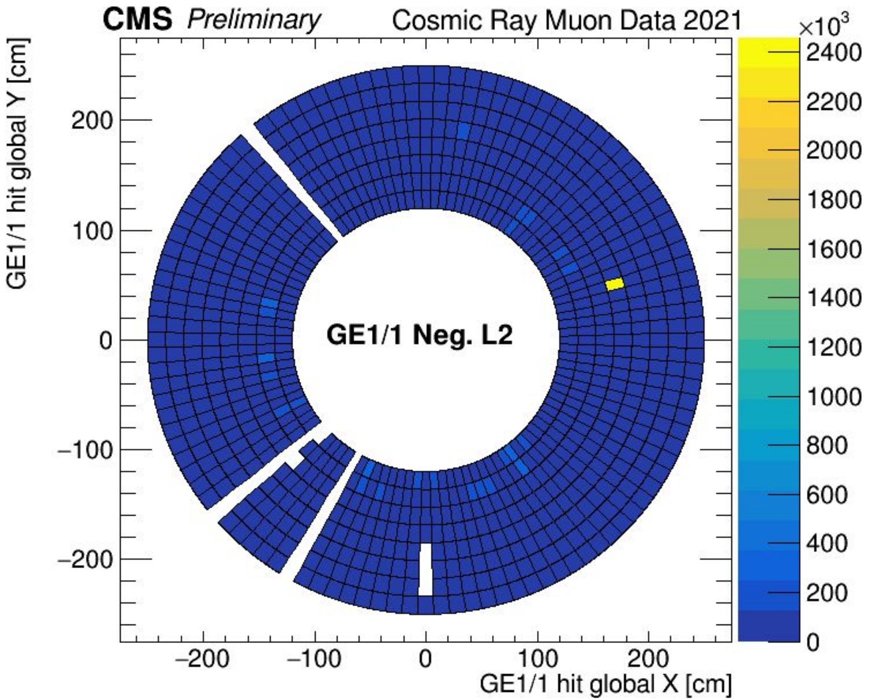



# Communication failures (I)

Soon after the installation, unexpected communication failures with the front-end electronics were observed, both during calibration scans and regular data taking. Combination of multiple effects:

- GBTx chip fetching corrupted configuration from fuses after power-up (failure rate of a few %)
  - Automatic power cycle of unlocked links implemented in 2021 through the communication between the DAQ and DCS systems
- Random communication failures with the VFAT
  - Affect a single transaction or multiple transactions
  - Affect both the DAQ & trigger data paths
  - (Re-)designed the DAQ, firmware, and online software to gracefully handle communication instabilities (reached VFAT granularity in March 2022)




Lessons:

- **Always validate the front-end data & react accordingly in case of corruption.**
- **Start the commissioning of the full system as soon as possible with enough time for long-term stability tests.**

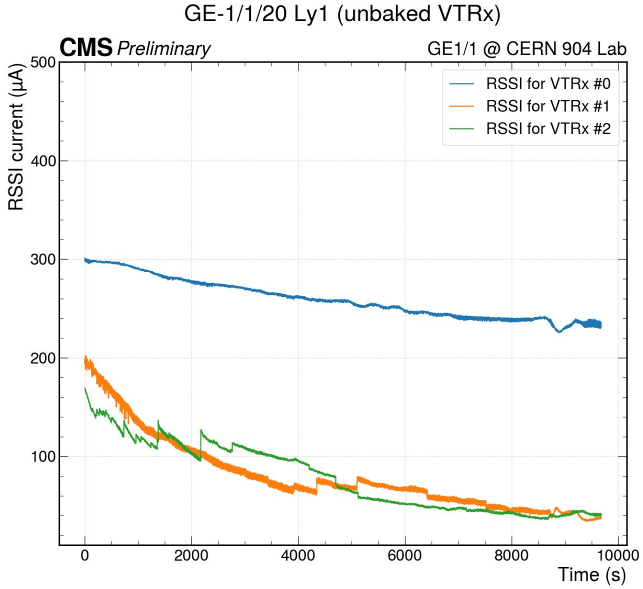
# Communication failures (II)

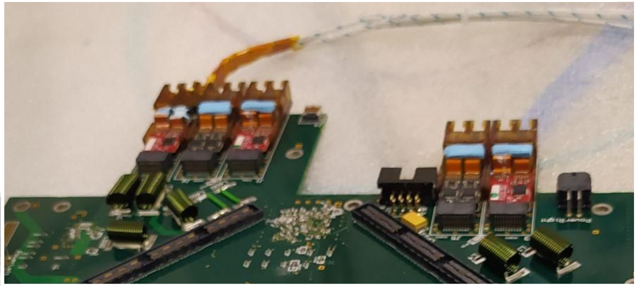
Another major source of communication failures is linked to the VTRx:

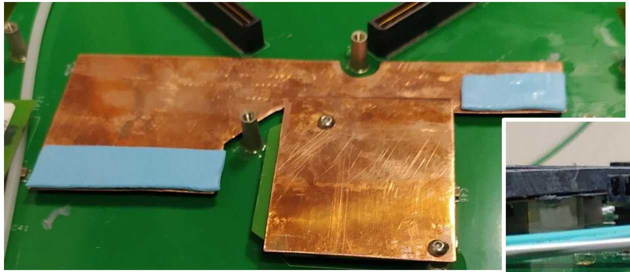
- If the temperature gradient between fiber and the VTRx ROSA (Receiver Optical Sub-Assembly) is high enough (> 10°), the VTRx assembly glues can outgas and deposit on the fiber
  -> Loss of optical power and thus connectivity

- Two most problematic super-chamber extracted from CMS
  - OptoHybrid modified to readout the Receiver Signal Strength Indicator (RSSI) from the VTRx
  - Refurbished with baked VTRx and now monitored
- **Improved cooling on VTRx/VTTx will be installed in LS3**

Issue fully workaround by the DAQ developments previously mentioned.





# High-multiplicity events

October 2021 was the first time GE1/1 was fully read out at high trigger rates (~50 kHz):

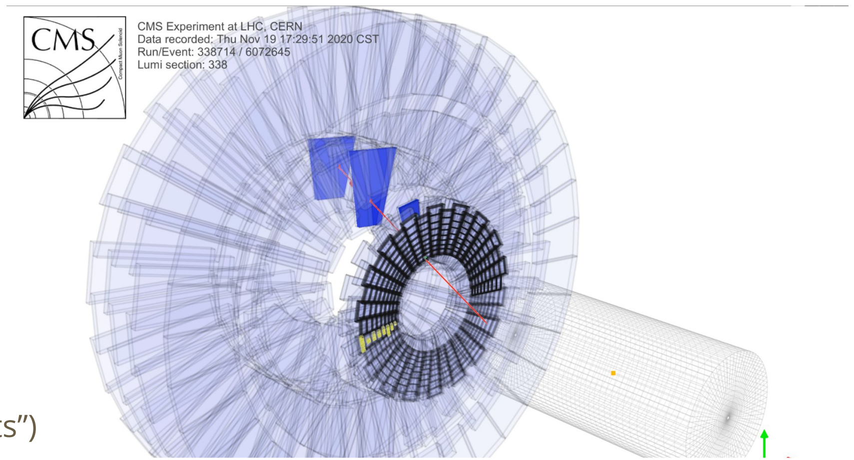
- Implemented Zero Suppression (ZS) read-out mode, reducing the event size and avoiding bandwidth saturation
- Witnessed high-multiplicity activity events (a.k.a. “flower events”)
  - **Event with a large number of GEM clusters O($10^3$)**

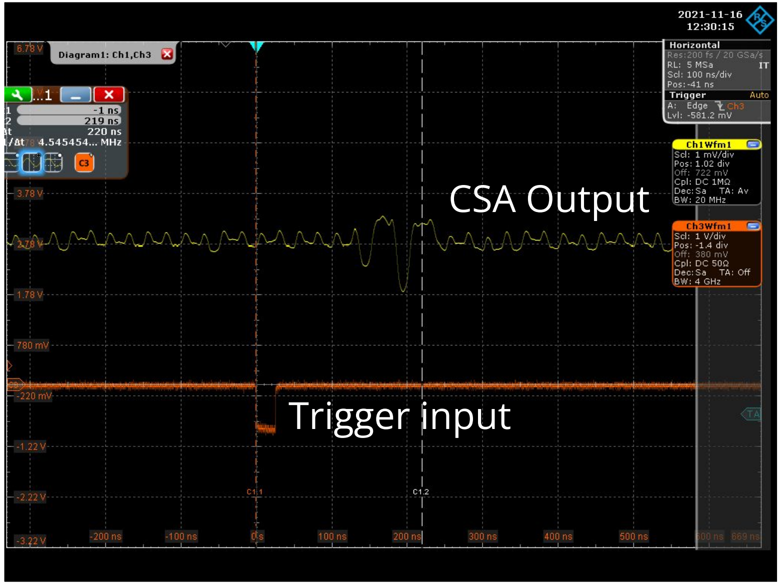
Problem understood and coming from the VFAT ASIC:

- Upon L1A, the instantaneous current drawn in the digital power domain induces a signal/noise in the analog power domain

Investigating the best strategy in terms of effective efficiency:

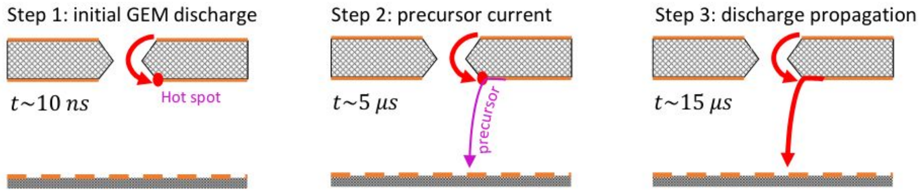
1. Increase the thresholds to cut the induced noise
2. Mask the clusters in the reconstruction, either timing- or pattern-based
3. Mask the clusters in the trigger path, either timing- or pattern-based
4. Implement a trigger-less readout
5. Implement regional triggers



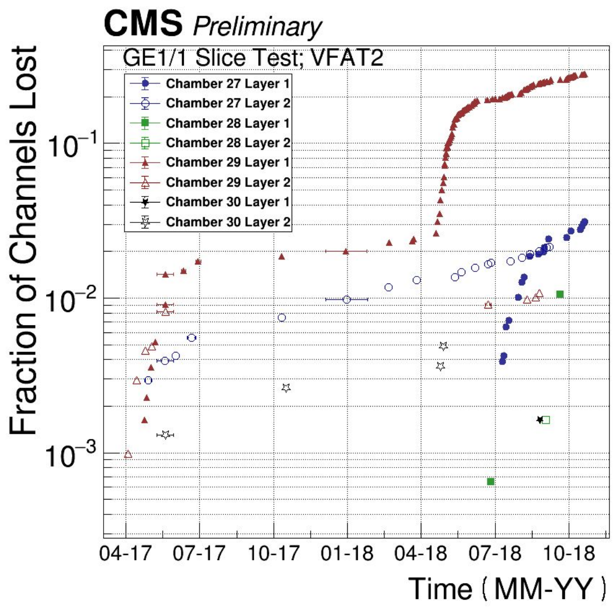

Courtesy of F. Licciulli

# Discharges & channel loss




Front-end channel loss was experienced during the GE1/1 slice test:

- The process was understood and attributed to discharges propagating to the anode and front-end ASIC
- The GEM technology is known to experience internal discharges; discharges propagating to the anode were unexpected
  - **No particular protection circuit was present on the the ASIC inputs**



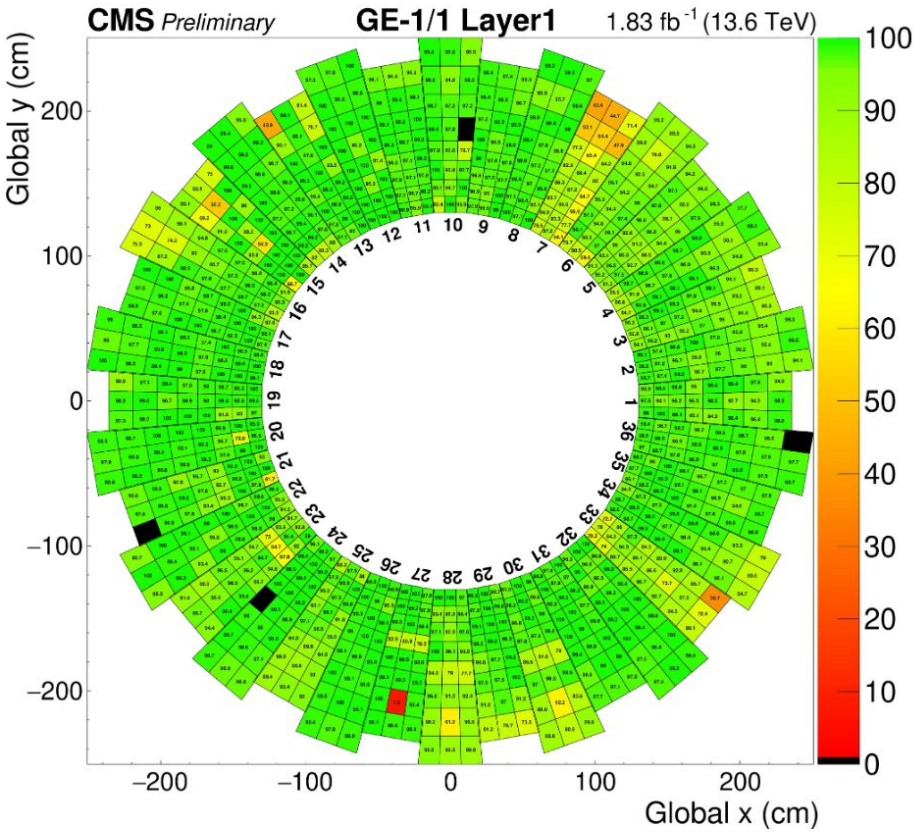

Two mitigations measures were implemented in GE1/1:

- Improvement of the electronics input protection through resistors (lowers the damage probability)
- Increase of the HV filter resistance (lowers the propagation probability)

Monitoring the number of active channels, and loss over time, is critical to best adjust the HV operations. In particular, any period with increased discharge rate must be carefully monitored.

**channel loss rate =**
**background rate (~3.15x10$^3$/VFAT) * discharge prob. (~1.24x10$^{-9}$) * propagation prob. (~50%) * damage prob. (~3%)**

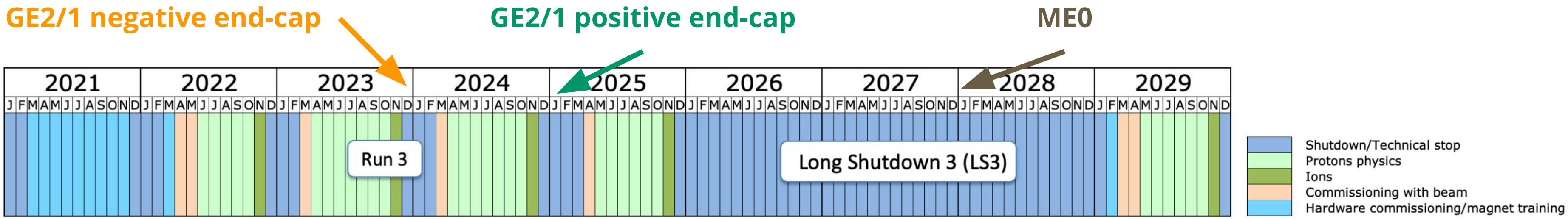
# Today : the GE1/1 upgrade

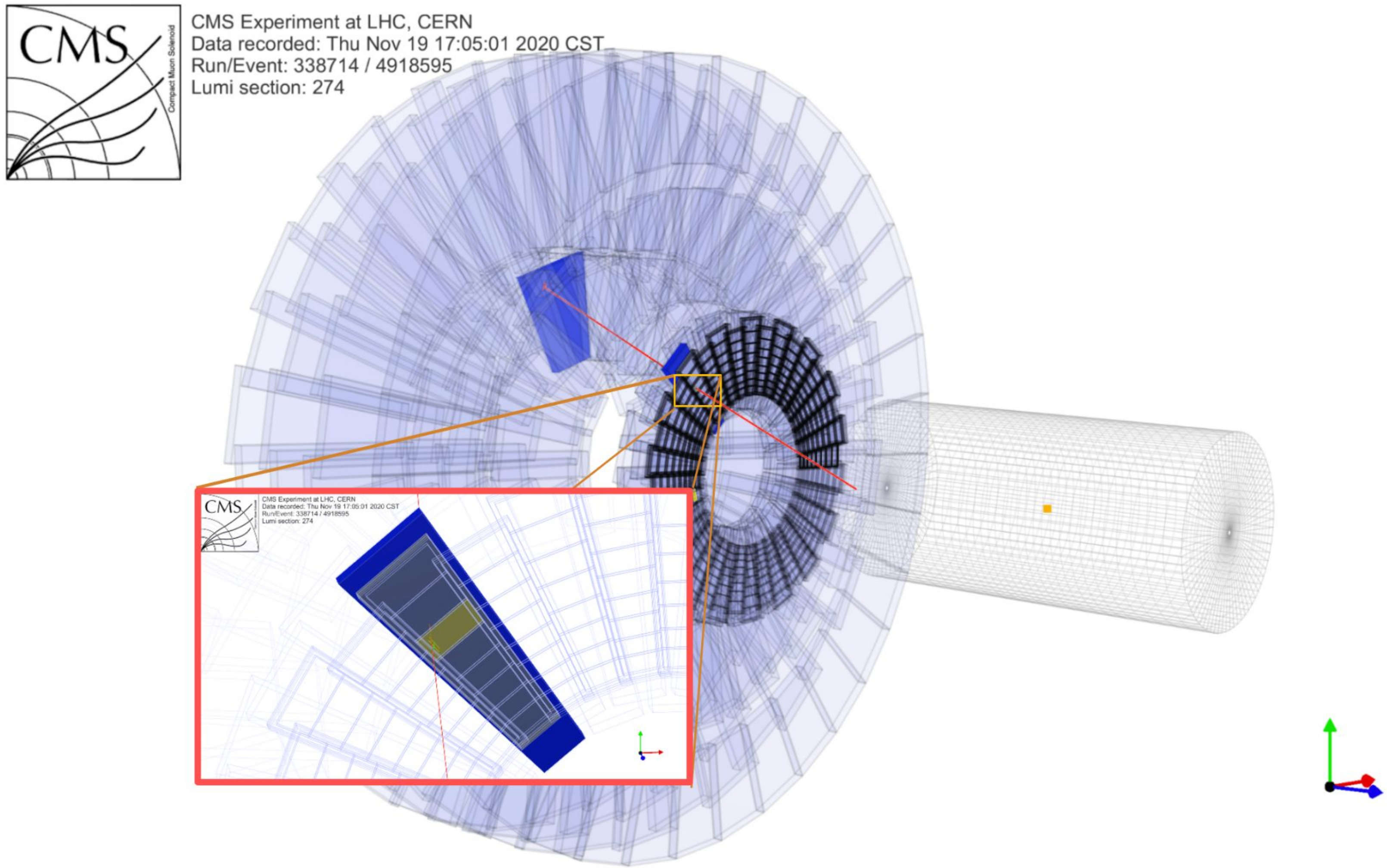



- The GE1/1 station is the first Triple-GEM detector installed as part of the CMS upgrades for high-luminosity LHC
- New detector means new problems
  - Are addressed one after the other
  - So far, so good
- Data taking in the new routine
  - Continuously assess the health of the detector, efficiency, timing,...
- Fine-tuning is starting
  - Refine the high-voltage working point
  - Optimize the front-end parameters (e.g. gain, shaping time,...)

# Tomorrow : the CMS GEM Phase-II upgrades

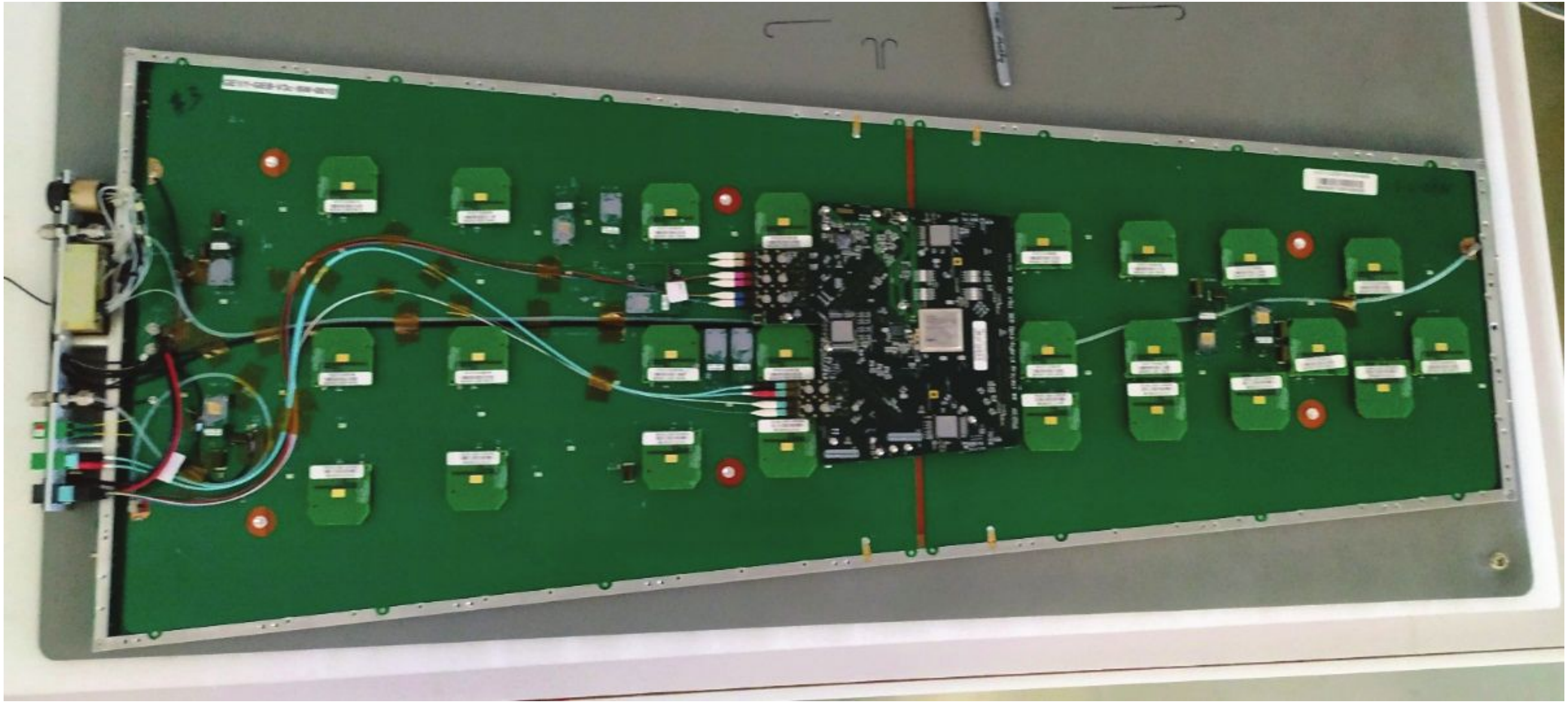
- Building on the knowledge and experience acquired with GE1/1
  - Noise, channel loss, timing, commissioning,... are all considered
- The GE2/1 station is starting mass production
  - VFAT3 front-end ASIC, OptoHybrid boards, GEM foils, and modules
  - Final quality control and integration steps at CERN are being reviewed and implemented
  - First end-cap (144 modules) to be installed end of 2023; second end-cap to be installed end of 2024
- The ME0 is mostly under the developing stage
  - Prototypes designed and under test for all components
  - Integration of a complete detector planned in the upcoming weeks and months
  - Chamber installation scheduled for the end of 2027 during the Long Shutdown 3




CMS
CMS Experiment at LHC, CERN
Data recorded: Thu Nov 19 17:05:01 2020 CST
Run/Event: 338714 / 4918595
Lumi section: 274

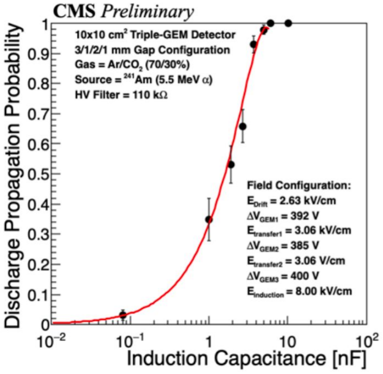
# Backup

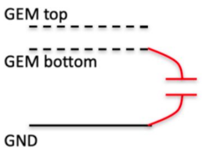
# GE1/1 Chamber

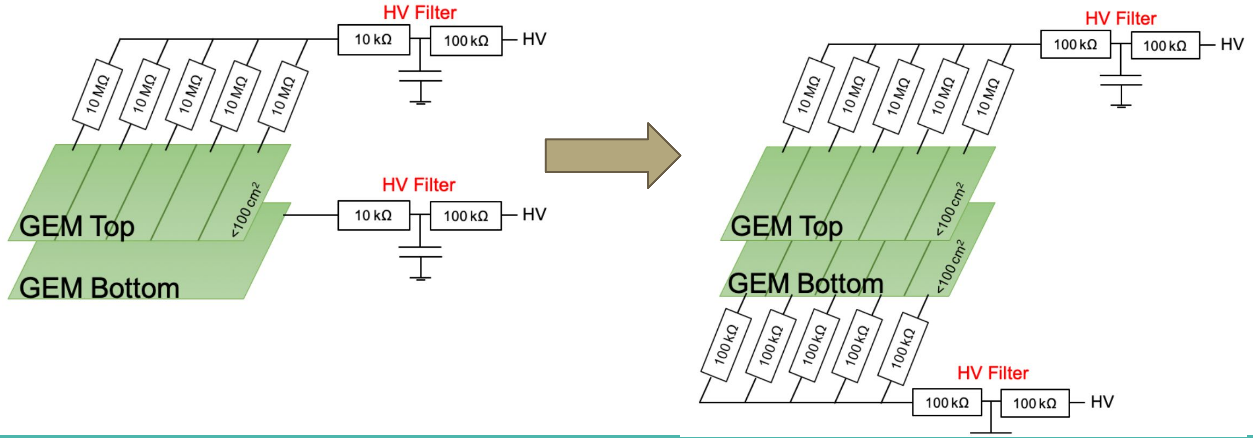


# Double-segmented GEM foils

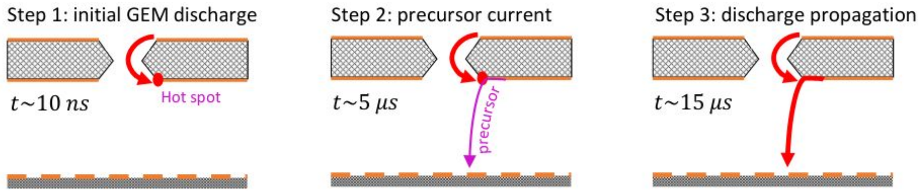
- In GE1/1, single-segmented (top segmented) foils used
  - Protect the detector in case of discharges
  - Allow to operate the chamber in case of shorts
  - Large “induction” capacitance
    - Enough energy to trigger a propagating discharge
    - Enough energy to damage the readout electronics
- In GE2/1, double-segmented foils (top and bottom segmented) have been designed
  - Limited energy to trigger discharges and damage the electronics



# Discharges mitigation




Front-end channel loss was experienced during the GE1/1 slice test (demonstrator chambers installed in 2017 up to the end of the LHC Run-2)

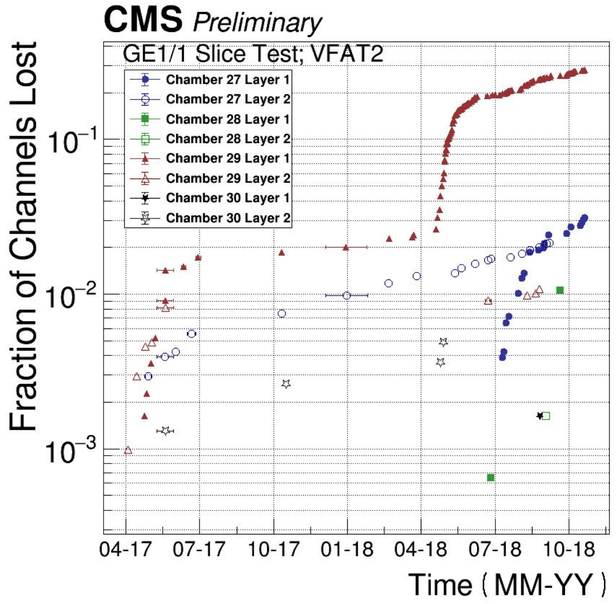
- The process was understood and attributed to discharges propagating to the anode and front-end ASIC

The process of discharge propagation is mainly driven by the large capacitance of the foils. Possible mitigations strategies are

- Usage of drain resistors GE2/1
- Reduction of the foil capacitance GE2/1
- Increase of the HV filter resistance GE1/1 GE2/1

The process of damage is mainly due to the re-ignitions of the propagating discahrge. Possible mitigations strategies are

- Improvement of the electronics input protection GE1/1 GE2/1
- Increase of the de-coupling with the HV filter capacitance GE2/1

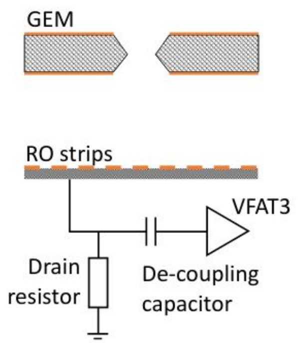


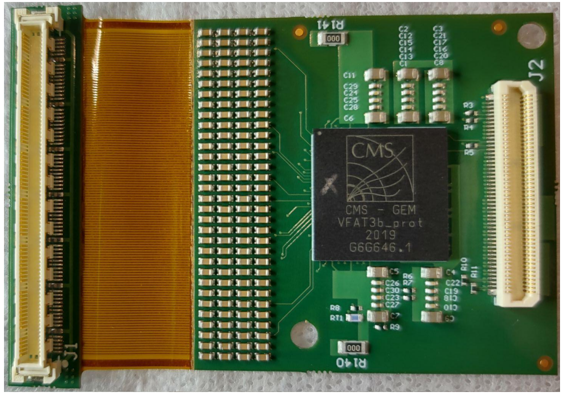

**channel loss rate = background rate * discharge prob. * propagation prob. * damage prob.**

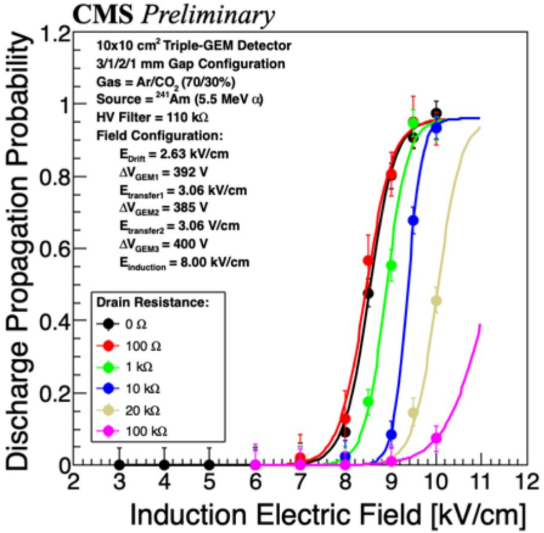
# Electronics input protection

GE2/1 allowed the re-design of the front-end electronics PCB with the implementation of a protection circuit targeting two purposes

1. Reducing the damage probability via a decoupling capacitor
   - Avoid the ASIC input channel to absorb the full energy of the discharge
2. Reducing the discharge propagation to the anode via a drain resistor
   - Quenches the precursor current by increasing the readout strip potential and suppressing the induction field

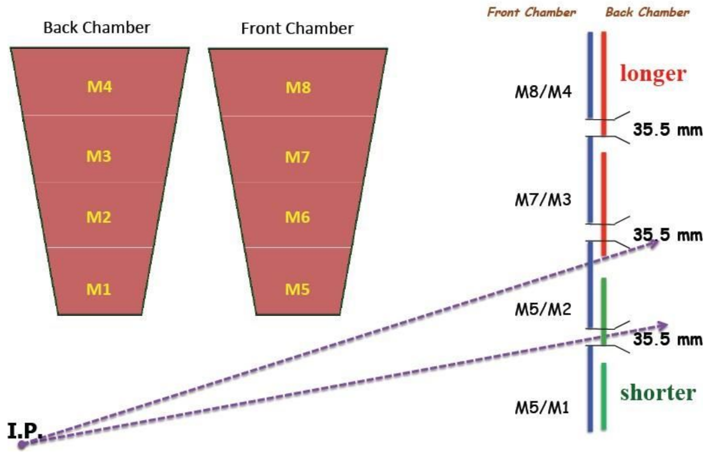


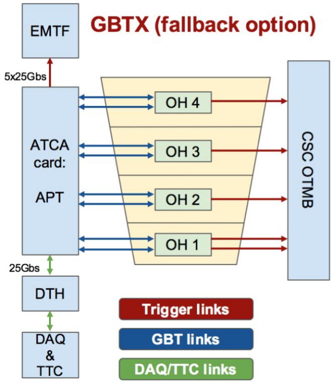



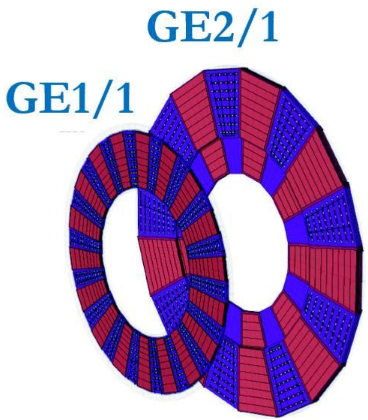



# The GE2/1 station

- Same Triple-GEM technology as GE1/1
  - Pseudorapidity |η| coverage: 1.62-2.43
- 18 super-chambers per endcap
  - 2 layers of different types to avoid overlapping dead areas
  - 4 modules per chamber
    - M1, M2, M3, M4 or M5, M6, M7, M8
- 288 modules (300 with spares)
  - Module angular opening: 20°
  - Size similar to GE1/1
- 442,368 readout channels
- Similar readout electronics as GE1/1
  - Each module equipped with one OptoHybrid (OH) board
    - 2 GBT links per OH
    - One embedded FPGA for triggering purposes
  - Front-end trigger and readout ASIC (VFAT3)



# Production challenges

Large PCBs such as the ones used for the GE2/1 Triple-GEM drift and readout boards tend to bend when subject to stretching forces.

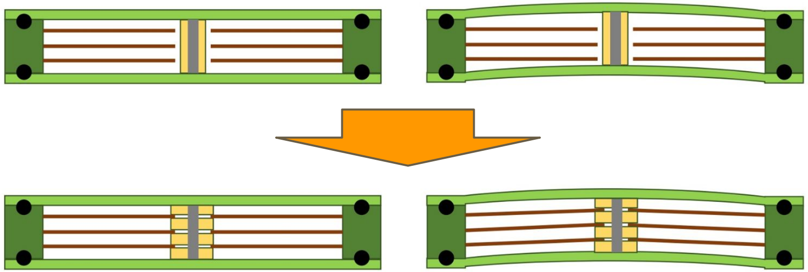
- Causes of a variation of gain across the detector

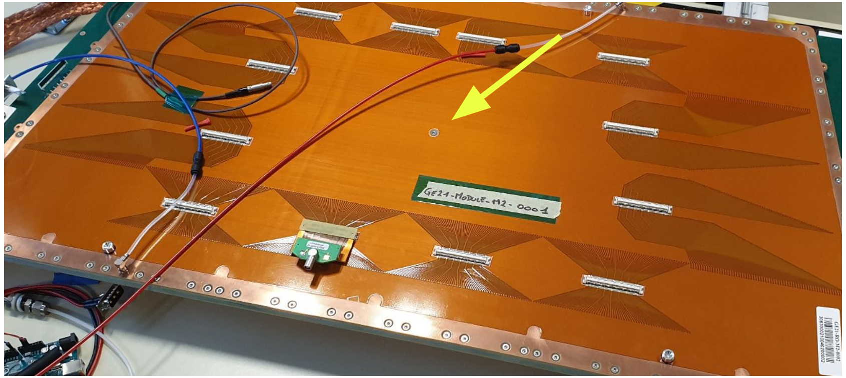
➔ A set of pillars were introduced in the GE2/1 design as an enhancement with respect to GE1/1

- Help to keep constant the gap between drift and readout PCB
- Increase minorly in the dead area
- Work well only if the PCBs are produced flat

➔ Replace the pillars to maintain the distance not only between the drift and readout PCBs but between all electrodes

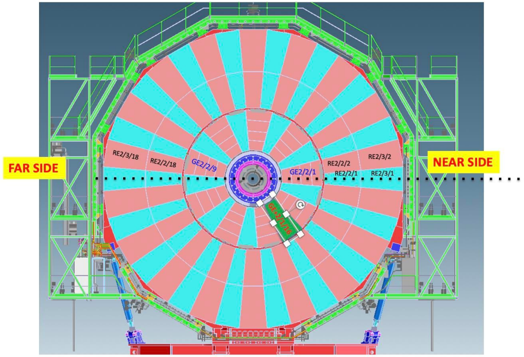
- Maintain the gap distances even for significant bending of the PCB

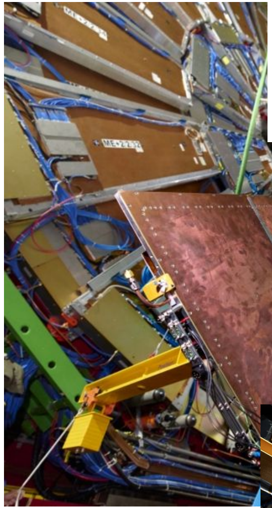


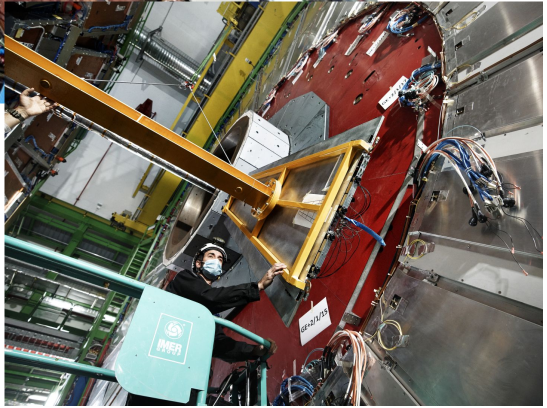


# GE2/1 demonstrator

- The GE2/1 demonstrator is a complete GE2/1 prototype layer 2 chamber that was installed in CMS (sector 16, layer 2, positive end-cap) in November 2022 as preparation for the installation and operation of the full GE2/1 system
- Exercise the installation steps
  - Mechanical installation tools
  - Services (gas, low-voltage, high-voltage) connection
- Gain operational experience
  - Test the readout electronics
  - Develop and test the DAQ system
  - Develop and test the DCS system
- Perform various confirmatory measurements:
  - Test the updated foil design and the discharges protection schemes in a real environment
  - Evaluate the channel loss rate
  - Assess the noise levels and ensure the effectiveness of grounding solutions
  - Estimate the noise rates and the cross-talk in a realistic environment



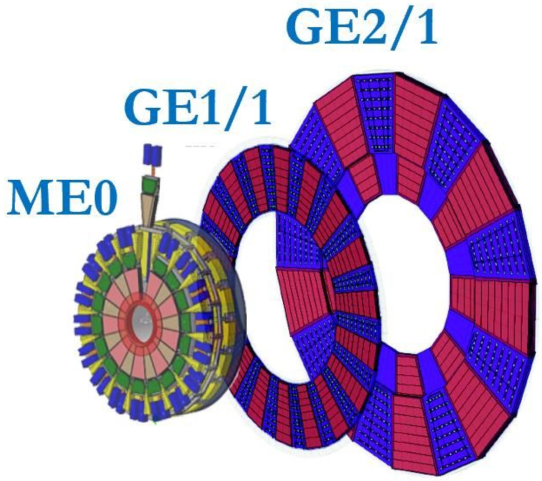


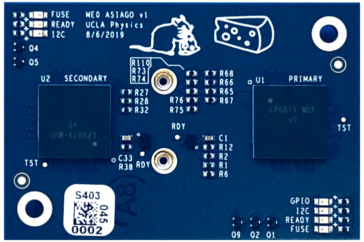
# The ME0 station

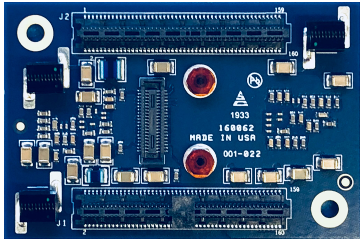
- Last part of the Triple-GEM upgrade of CMS
  - Pseudorapidity |η| coverage: 2.03–2.8
  - Closer to the beamline, closer to the interaction point
    - Higher background rate (up to 150 kHz/cm$^2$)

- 18 stacks per endcap
- 6 modules per stack
- 216 modules
  - Module angular opening: 20°
  - Module active area: 0.296 m 2
- 331,776 readout channels

- New readout electronics design with respect to GE1/1 and GE2/1
  - GBTx links -> lpGBT (4.8 Gbps -> 10.24 Gbps)
  - No embedded FPGA
  - Stub building for the L1 trigger
  - Same readout ASIC (VFAT3)



# References


- A. Colaleo, A. Safonov, A. Sharma, M. Tytgat, *CMS Technical Design Report for the Muon Endcap GEM Upgrade* - June 2015 (CERN-LHCC-2015-012, CMS-TDR-013) https://cds.cern.ch/record/2021453
- F. M. Simone, *The new GEM station GE1/1 of the CMS muon detector: status, commissioning and early performance studies* - iWoRID2021, 28 June 2021 https://indico.cern.ch/event/820476/contributions/4372964/attachments/2271940/3858641/fsimone_GE11_iWoRID2021_finaldraft_v3.pdf
- B. Regnery, M. S. Abbott, G. Mocellin, *Demonstrating the capabilities of a new GEM* - CMS News, November 2021 https://cms.cern/news/demonstrating-capabilities-new-gem
- J. A. Merlin, *GEM stack optimization for GE21 and ME0 (cross-talk studies, discharge mitigation)* - RD51 Collaboration Meeting, 24 June 2020 https://indico.cern.ch/event/911950/contributions/3879507/attachments/2062838/3460906/JMerlin_Xtalk_18052020_V2.pdf
- J. A. Merlin, *Discharge Protection, Cross-talk and Rate Capability* - RD51 Collaboration Meeting, 8 October 2020 https://indico.cern.ch/event/889369/contributions/4040763/attachments/2118822/3565435/JMerlin_SparkProtection_08102020_V2.pdf
- S. Kim, *CMS GE2/1 Status* - CMS Muon Workshop, 31 January 2022 https://indico.cern.ch/event/1121600/contributions/4708900/attachments/2381829/4070145/SKim_GE21Status_310122.pdf