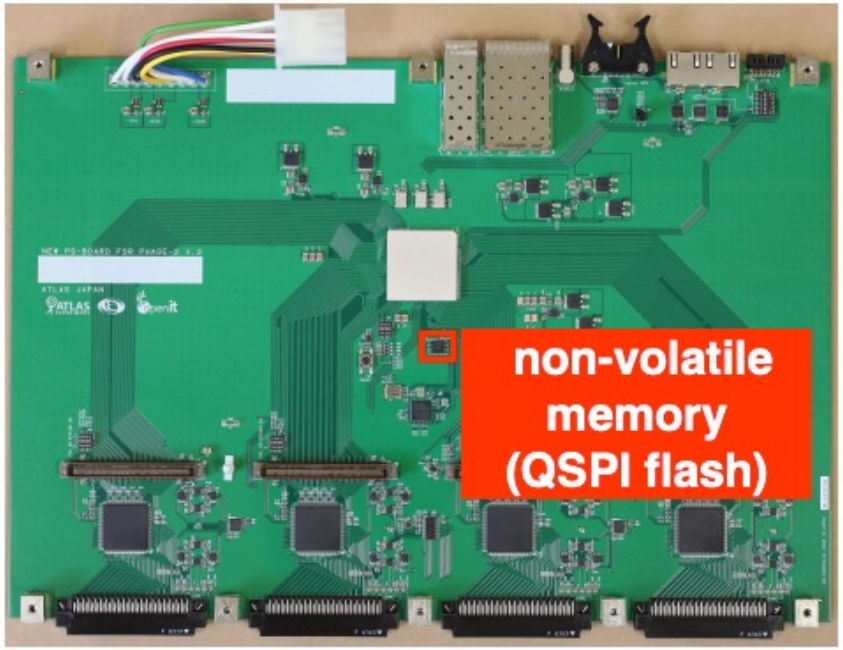
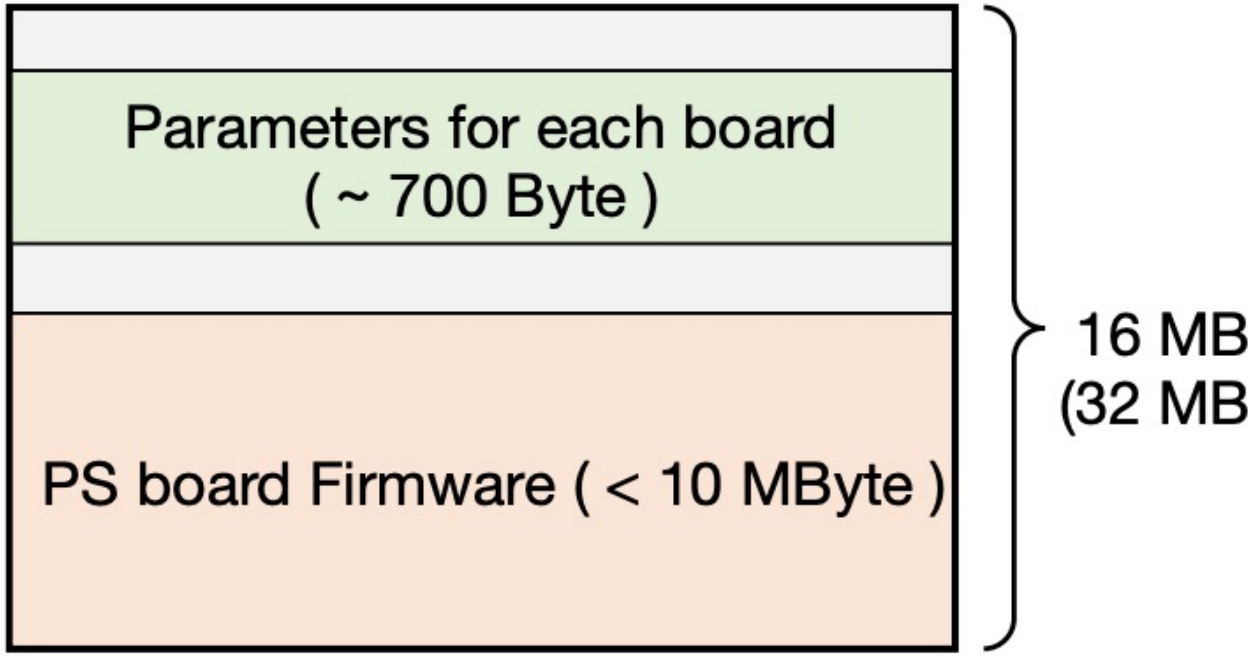
Figure 1



(a) PS board with QSPPI flash device,



(b) “user space” available in QSPI device.

FPGA-based electronics systems with the associated QSPI flash memory often spare extra memory space in the flash memory device in addition to the firmware bitstream file. We can exploit the extra space to store the operation parameters, which might have board-by-board variation. The FPGA logic can make the complete configurations without communication with remote control. Figures 1 show the usage of QSPI flash memory in this fully-automated and self-driven configuration system. For the ATLAS Phase-II TGC frontend case (PS board), at least ~6 M Byte will be available as "user space", and it is possible to store all the information needed for the self-driven configuration in the space.

Figure 2

Figure 2 shows the logic diagram implemented in the ATLAS Phase-II TGC frontend system. The logic retrieves operation parameters from external QSPI flash, stores them in triplicate memory for redundancy for single event upsets, and then components on the PS boards are configured accordingly. An FPGA logic to supervise the self-driven configuration procedure is also implemented. It monitors the board's status so that it can recognise the situation in a self-driven manner and launch the needed control procedure for the event (such as power cycle, optical link resynchronisation, and recovery from a soft error event).

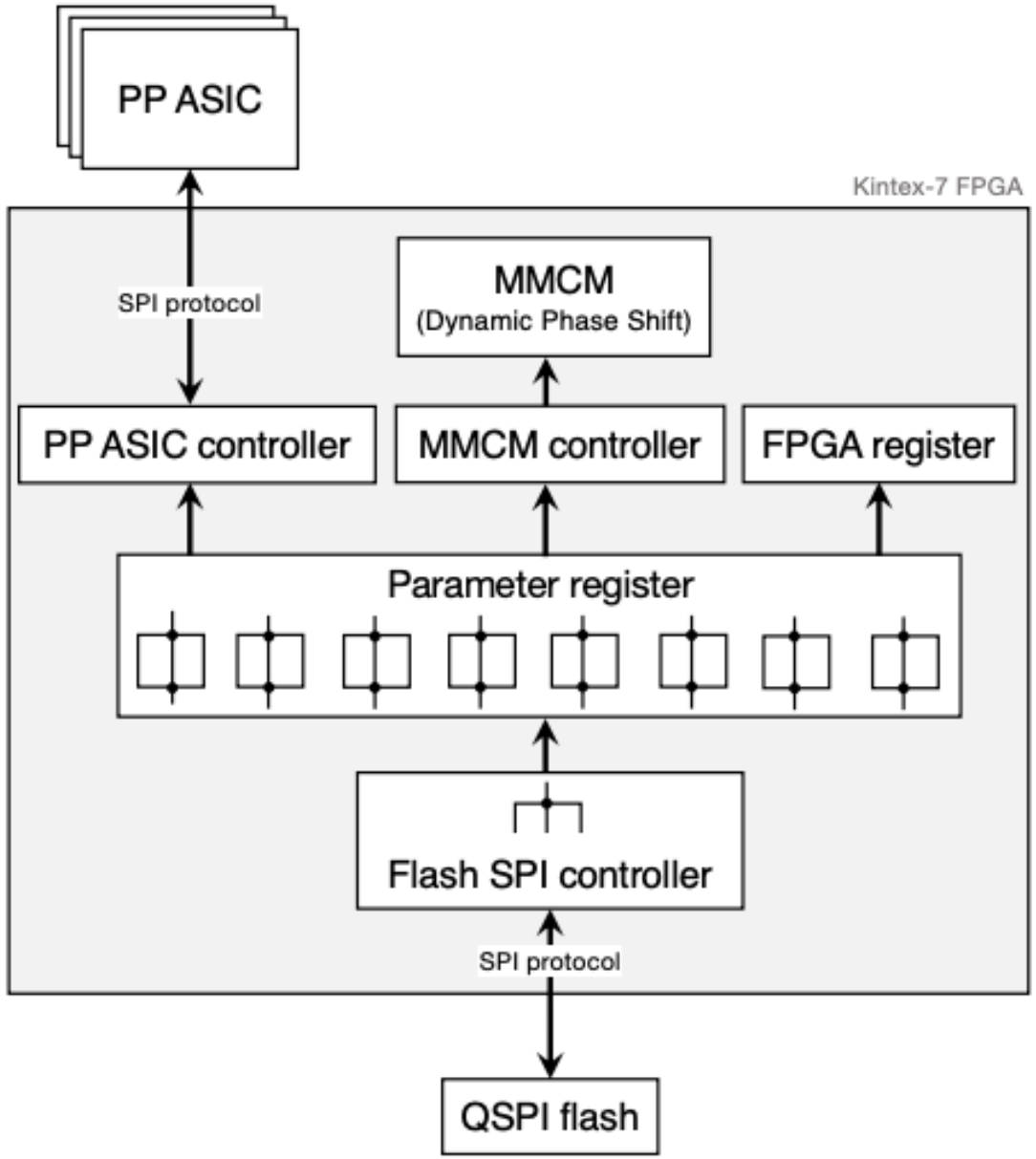
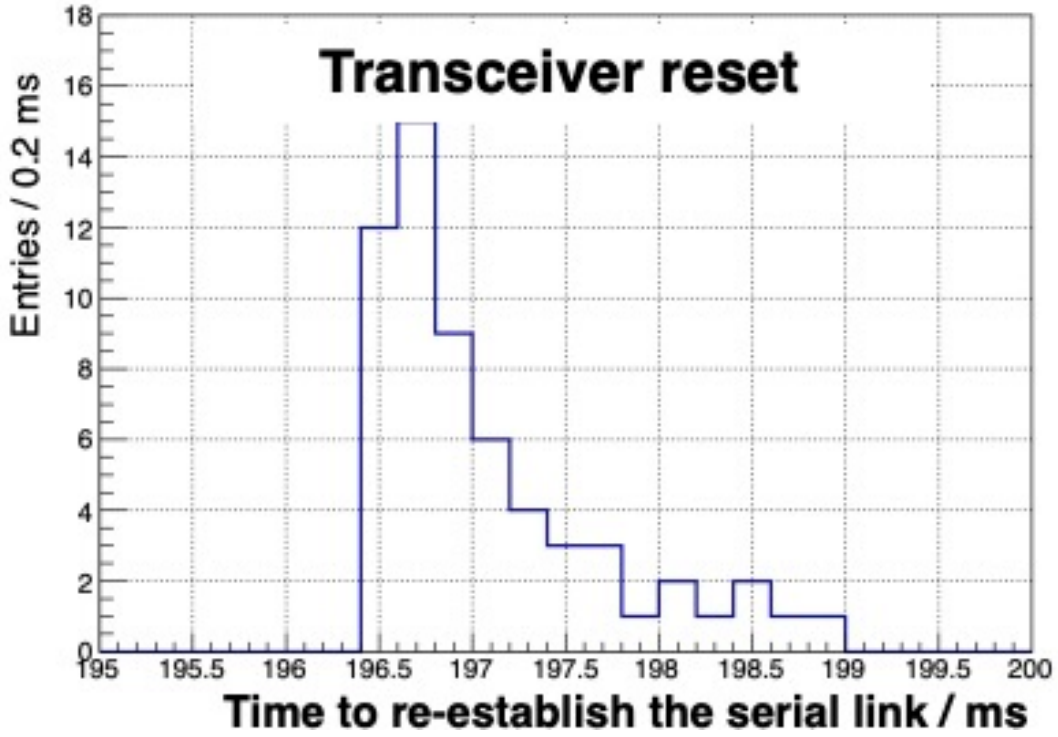
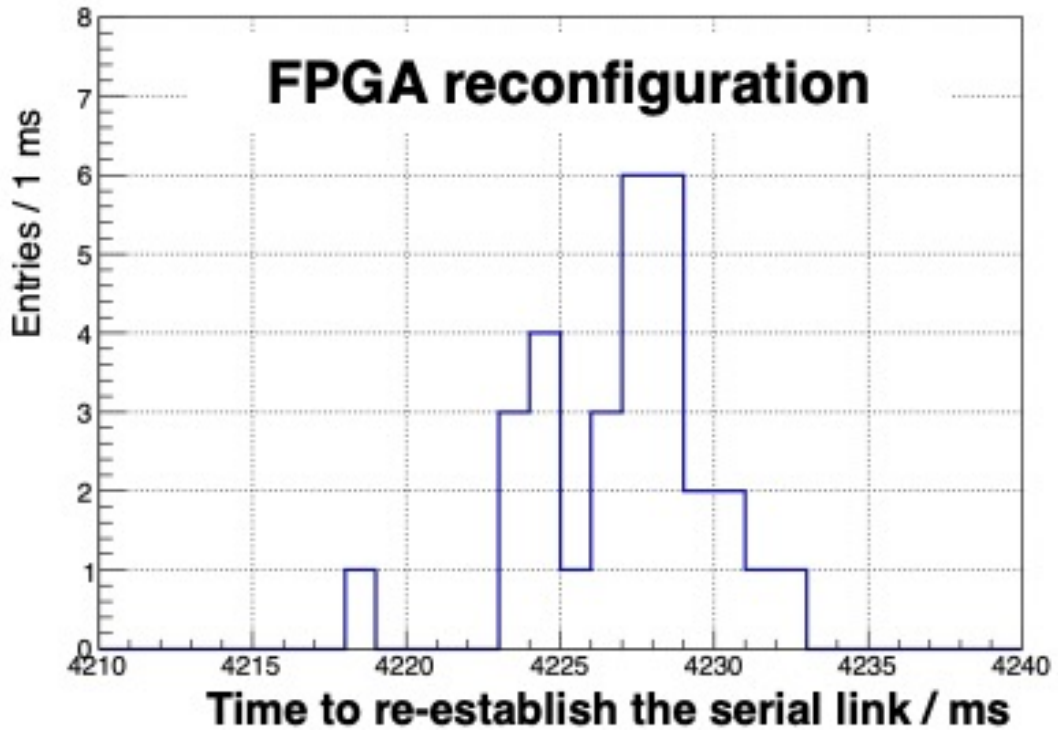


Figure 3



(a) Duration for link resynchonisation.



(b) Duration for Complete reprogramming for power cycle

Figure 3 shows the results of timing measurements in the ATLAS Phase-II TGC frontend system equipped with Xilinx Kintex-7 FPGAs: (a) Duration for transceiver reset for the case of serial link resynchronisation (200ms), and (b) duration for complete reprogramming for the case of a power cycle, including the FPGA configuration (~4s).