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Complete design of maximally-automated self-driven control mechanism for a large scale electronics system and its implementation to the ATLAS Phase-II TGC system

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Establishing a reliable and efficient method to control electronics system consisting of many boards is critical in the system design. Among unique requirements for the control in high energy physics experiments, we propose a maximally-automated and self-driven scheme for a system that exploits FPGAs, SPI flash memory devices, and high-speed fixed-latency optical links. We have implemented our ideas in the demonstration system of Phase-II ATLAS Thin Gap Chamber (TGC) system as the prototype for this new automated scheme. The method is widely applicable, and the knowledge and experience can be shared with other FPGA-based electronics systems.

Summary (500 words)

The FPGA-based design is one of the common choices in large scale electronics systems of high energy physics experiments, including front-end and back-end. Establishing a reliable and efficient method to control, configure, and monitor the electronics consisting of many boards is critical in the system design.
In collider experiments with large detector systems, fully tuned operational parameters of front-end electronics maximise the physics performance. For instance, we must maintain a variety of individual signal delay parameters for signal timing alignment for cable length and time of flight difference. Fixed latency operation of high-speed transceivers for serial links between modules in a system without phase ambiguity is a unique requirement in collider experiments for the clock distributions and pipeline trigger systems, which requires extra steps. Furthermore, it is crucial to take a minimally- required configuration sequence to keep the configuration duration as short as possible according to the situation, such as initialisation, resynchronisation of optical links, power cycle, or reprogramming FPGA to recover the soft error status. Among these demands, we propose an intelligent scheme of the configuration for the system consisting of FPGAs and associated flash memory devices, which are commonly available in various FPGA- based boards as firmware storage (Figure 1).
Our scheme will run the control and configuration in a fully standalone manner as follows with FPGA logic and SPI flash memory:
1. FPGA logic will automatically recognise the system's situation by monitoring the status of the FPGA device itself and external components to decide a minimally-required configuration procedure without communication with central service.
2. FPGA firmware will run the configuration sequence by itself, including the transceiver initialization in a fixed latency manner.
3. FPGA will retrieve all the individual parameters stored in external non-volatile memory devices.
Although traditional systems control the electronics from servers located in a remote place and often sequentially configure individual modules to handle the variation of operation parameters and sequential processes in a correct order, this new mechanism naturally parallelises all the electronics control without any communication with the

central system. It also maximises the efficiency of the operation. The FPGA will recognize error by itself and perform the recovery automatically without signals from the central system, and the new scheme allows us to minimise the possible downtime during the data taking.
We have implemented our ideas in the Phase-II ATLAS Thin Gap Chamber (TGC) system (Figure 2). The demonstration confirmed the mechanism works fine and indeed efficient and convenient in the testing, commissioning and system operation. We measured critical timings in the configuration (Figure 3), which confirmed that the new scheme allows us to complete the configuration of entire frontend system within four seconds including FPGA programming, which will be 60 times faster than the configuration timing for the existing system. The scheme can be applied to similar electronics systems with FPGAs and SPI flash memory. We can share the knowledge, experience, and technicality of the implementation for the design of other high energy physics experiments.

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