Development of a high-rate Scalable Readout System for gaseous detectors

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CERN, University of Bonn

Topical Workshop on Electronics for Particle Physics
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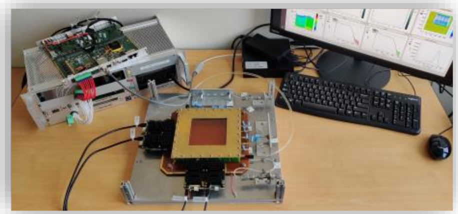
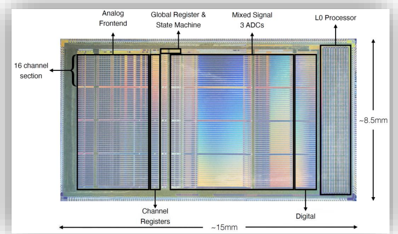
Outline

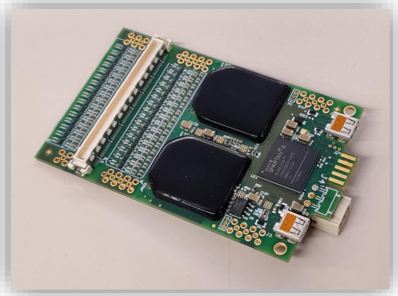
Background information



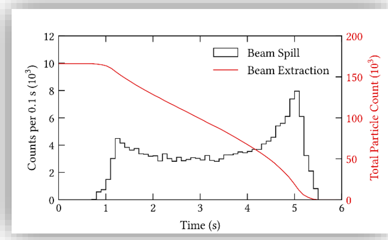
Front-end ASIC



Read-out system

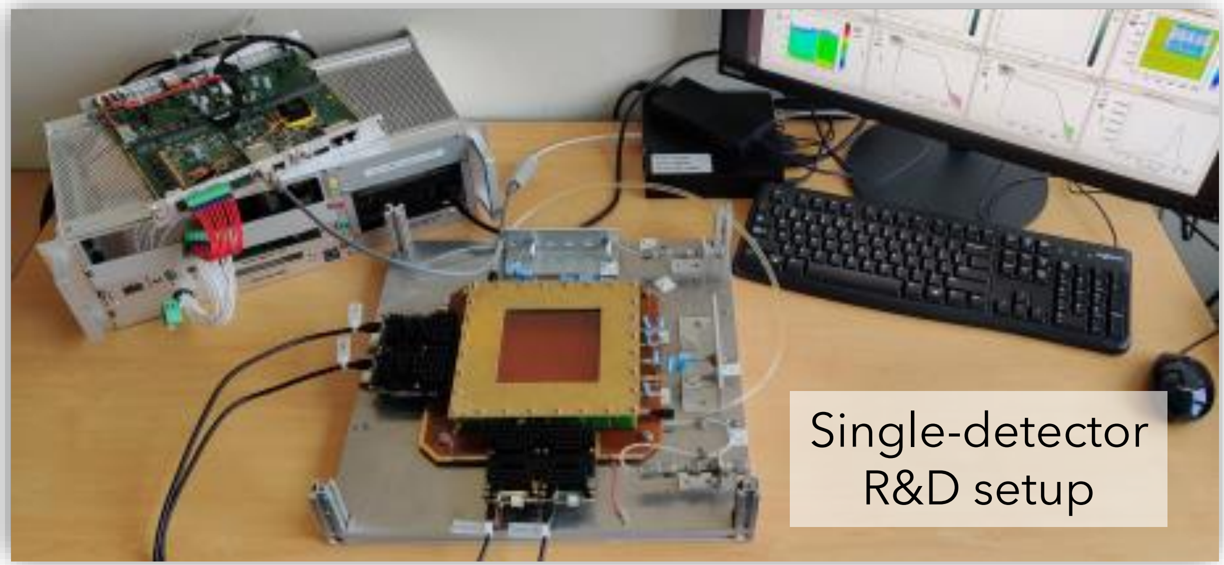


System capabilities



Micro-pattern gaseous detectors and RD51

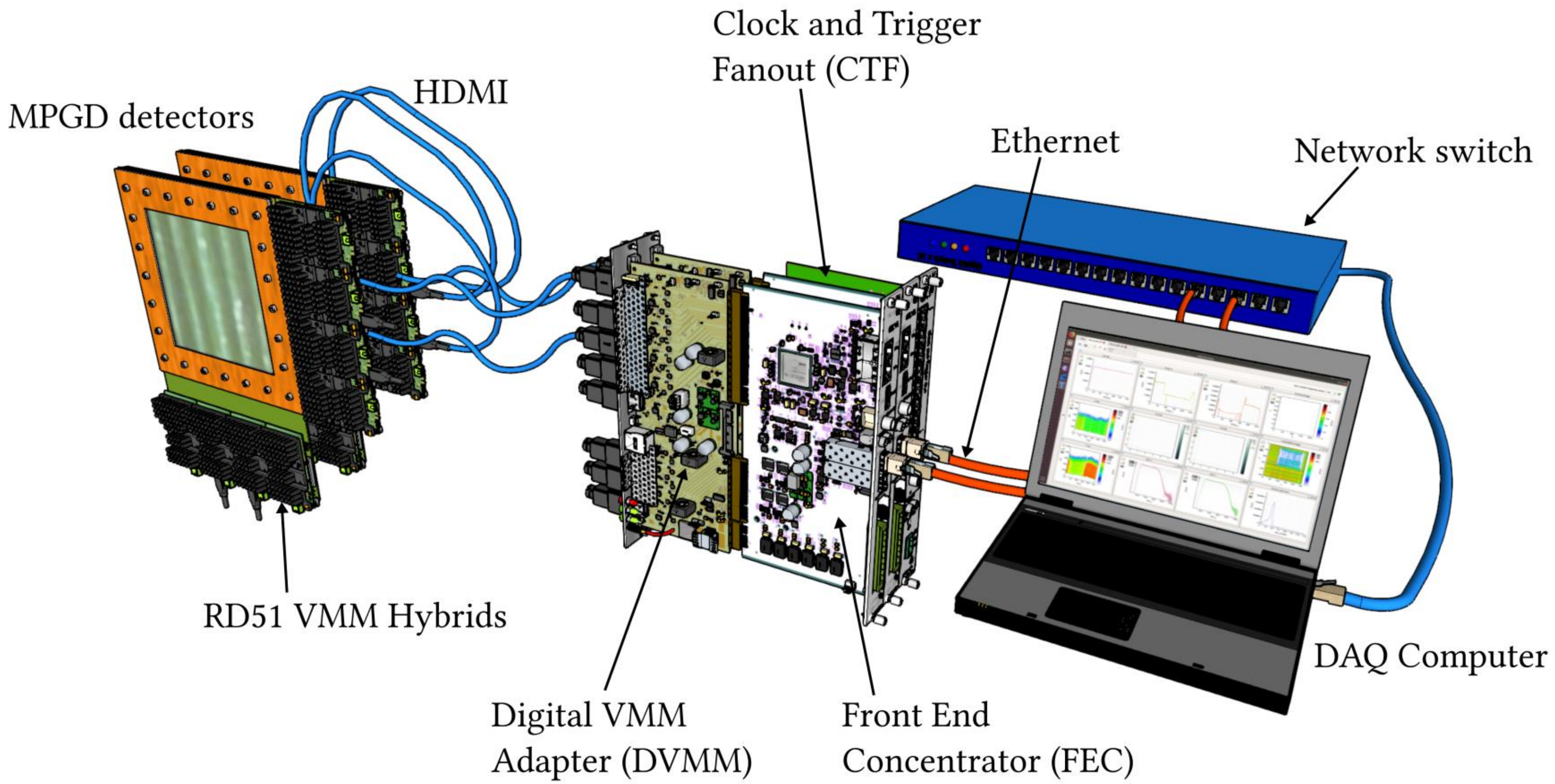
- **RD51**: CERN-based R&D collaboration on the development of **Micro-Pattern Gaseous Detectors** (MPGDs)
  - ~75 institutes
  - ~450 members
- Joint activities in the collaboration to profit from synergies
  - Test beam campaigns @ CERN SPS
  - **Common electronic readout system** (not only) **for MPGDs**
  - **RD51 Scalable Readout System (SRS)**
  - …
- SRS introduced in 2009
- Original SRS @ TWEPP 2012



Single-detector R&D setup

RD51 Scalable Readout System

- Read out small R&D setups (10 x 10 cm²) up to mid-sized experiments (several m²)
- Integrates various front-end ASIC (e.g. APV25, Timepix/Timepix3, VMM3a)



Courtesy of Hans Muller

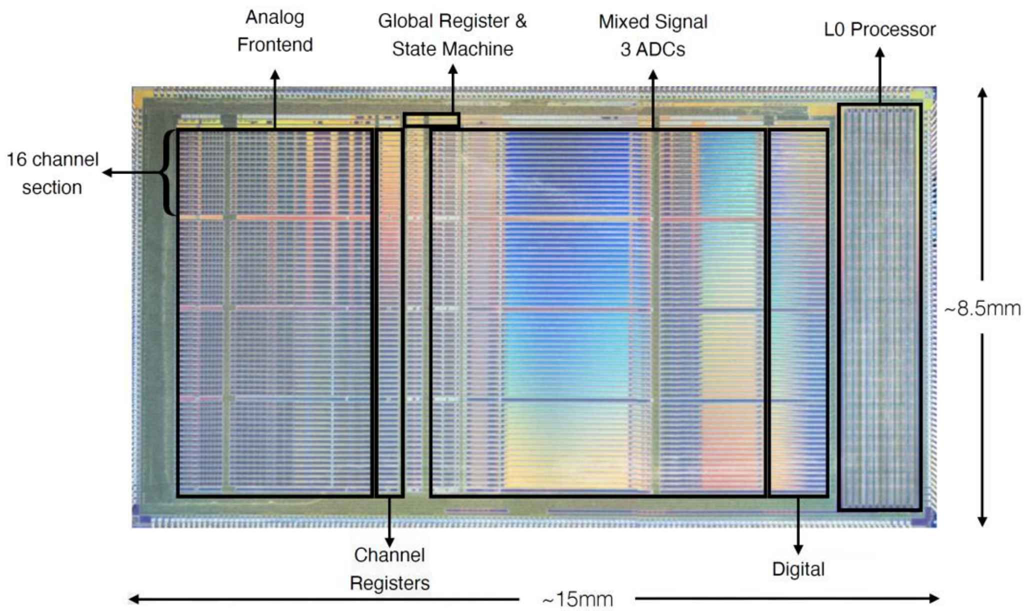
Requirements for MPGDs

- New requirements for MPGD from particle physics experiments
- ATLAS New Small Wheel (NSW), CMS GEM upgrade, ALICE TPC GEM upgrade
  - Spatial resolution **< 100 µm**
  - Time resolution in the **(sub-)nanosecond** regime
  - **MHz** rate-capability
  - Modules with m^2 size (active area of full detector up to 1000 m^2)
- Defines the requirements for electronics
- In the case of the ATLAS NSW: development of the **ATLAS/BNL VMM3a front-end ASIC**

Handle these requirements also for R&D setups and mid-sized experiments
=> Integration of the VMM3a into the RD51 SRS

ATLAS/BNL VMM3a front-end ASIC

- 64 readout channels
- **Self-triggered continuous readout in SRS implementation**
- 4 Mhits/s per channel, but max. **9 Mhits/s per VMM in SRS implementation**
- Integrated zero-suppression
- 10-bit **charge ADC**
- 12+8-bit **timing with O(ns) time resolution**
- **Adjustable peaking times** (25, 50, 100, 200 ns)
- **Adjustable electronics gains** (0.5, 1.0, 3.0, 4.5, 6.0, 9.0, 12.0, 16.0 mV/fC)
- Neighbouring-logic
- Subhysteresis discrimination
- **Input capacitances (< 200 pF up to 2 nF)**
- …

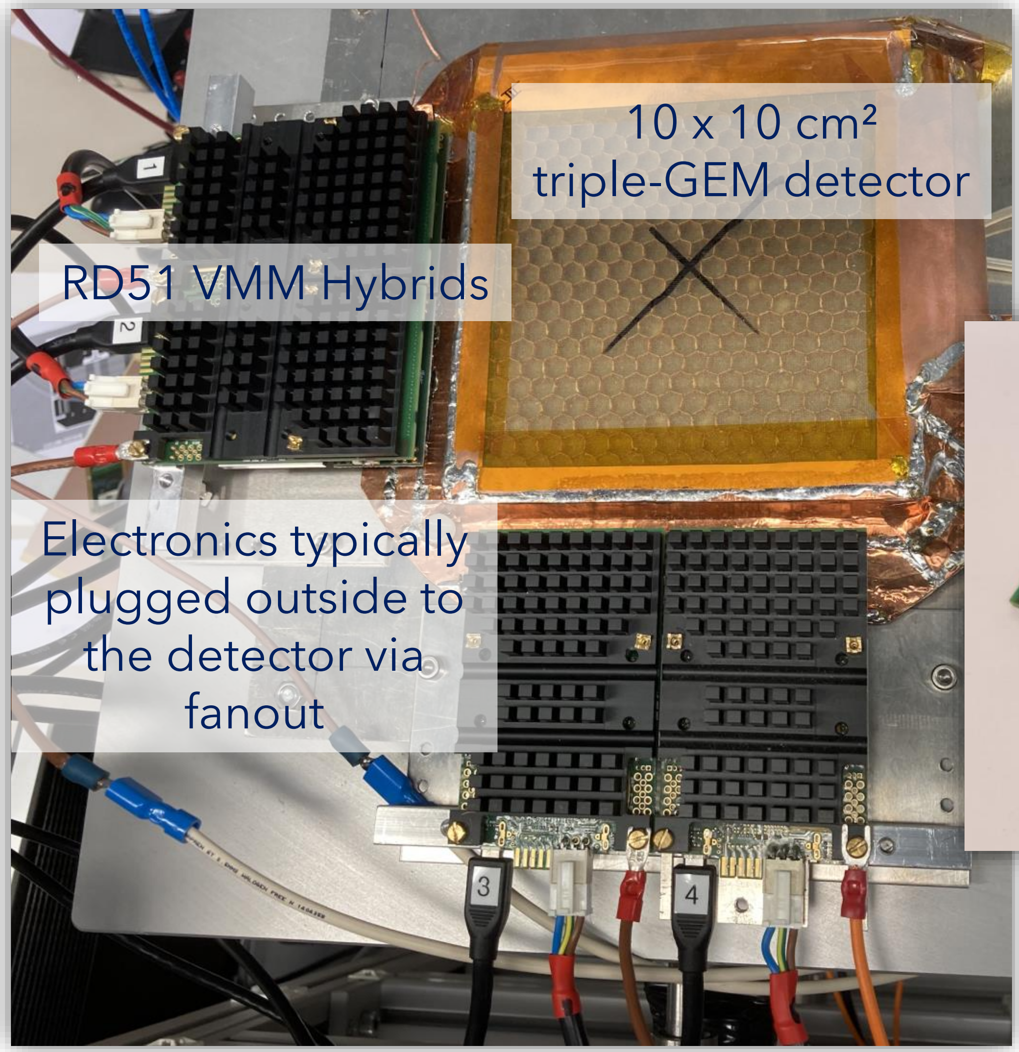


https://indico.cern.ch/event/1040996/contributions/4402617/

Configurability, i.e. peaking times and electronic gain, good for the SRS

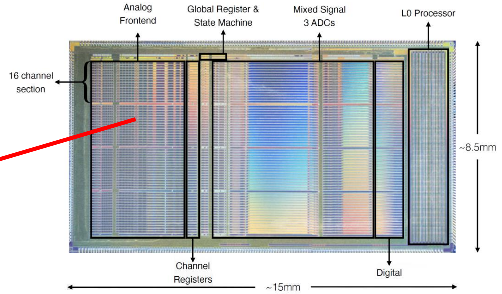
=> Cope with different detector technologies at once

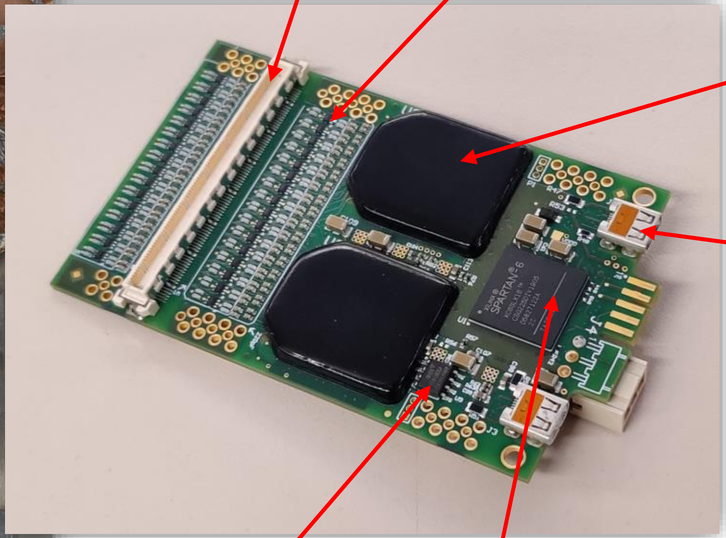
VMM3a front-end of the SRS



Hirose FX10A-140P connector
=> **128 readout channel per connector**

Discharge protection circuit for each channel





HDMI for clock, data and control signals

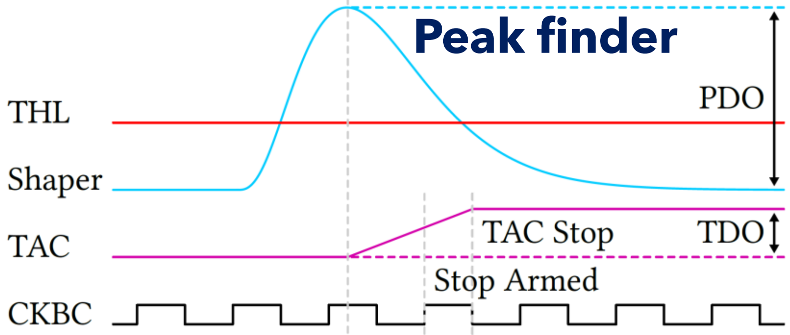
EPROM

Spartan-6 FPGA for signals

+ external ADC for VMM analogue monitoring output
+ LDOs for power regulation
+ Power/ground connector
+ ID chip

VMM3a front-end of the SRS

Each VMM channel signal = 40-bit in SRS implementation



Clockless ADC (10-bit), **only peak amplitude**

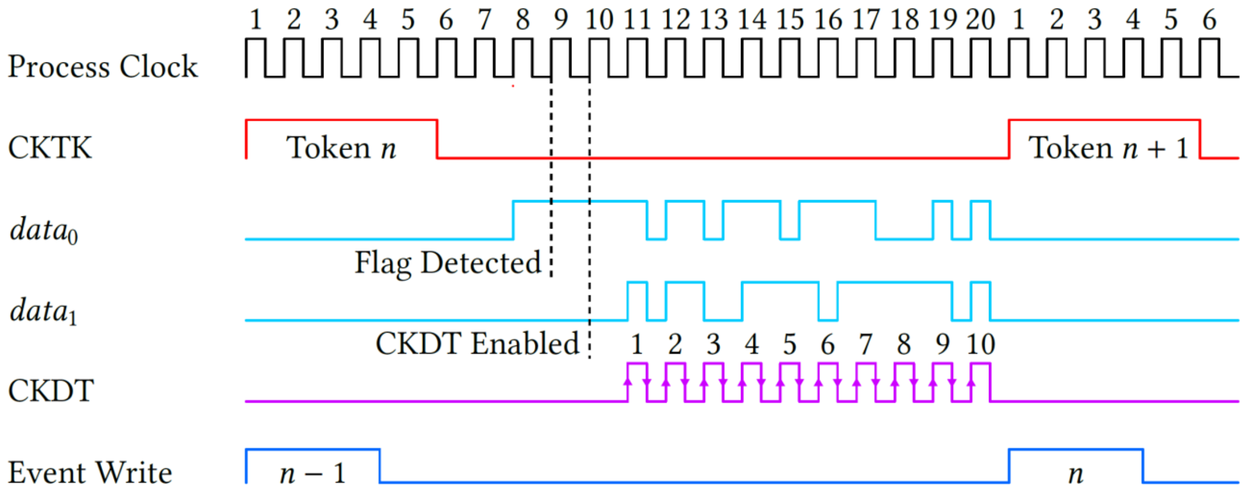
Over-threshold flag (1-bit)

TDC (8-bit **fine timestamp**)

Reference clock (12-bit **coarse counter**)

+ data-flag (1-bit)
+ channel number (6-bit)
+ extra bits for 8b/10b encoding (2-bit)

Token passing scheme to read the data from the channel for continuous readout

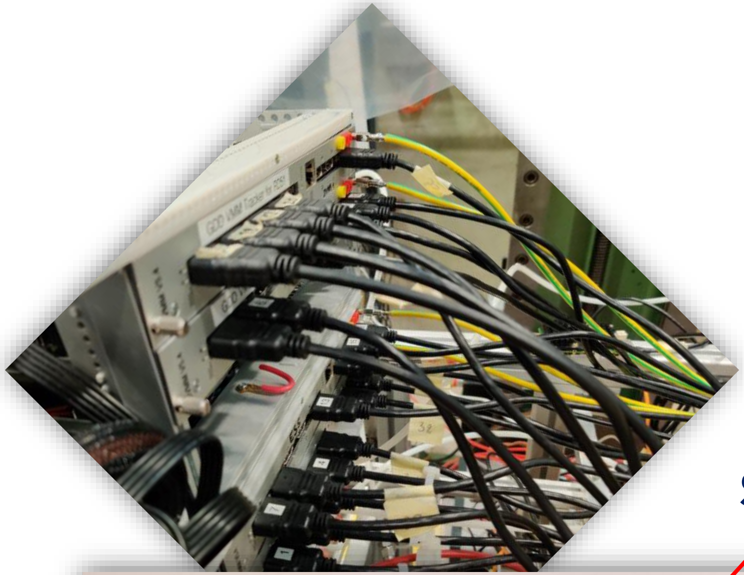


1. Token is sent
2. Data flag is detected
3. Data transmission is started
4. Event is written to buffer for 8b/10b encoding
5. Data are sent via SERDES on LVDS lines to adapter card

Maximally 9 Mhits/s per VMM

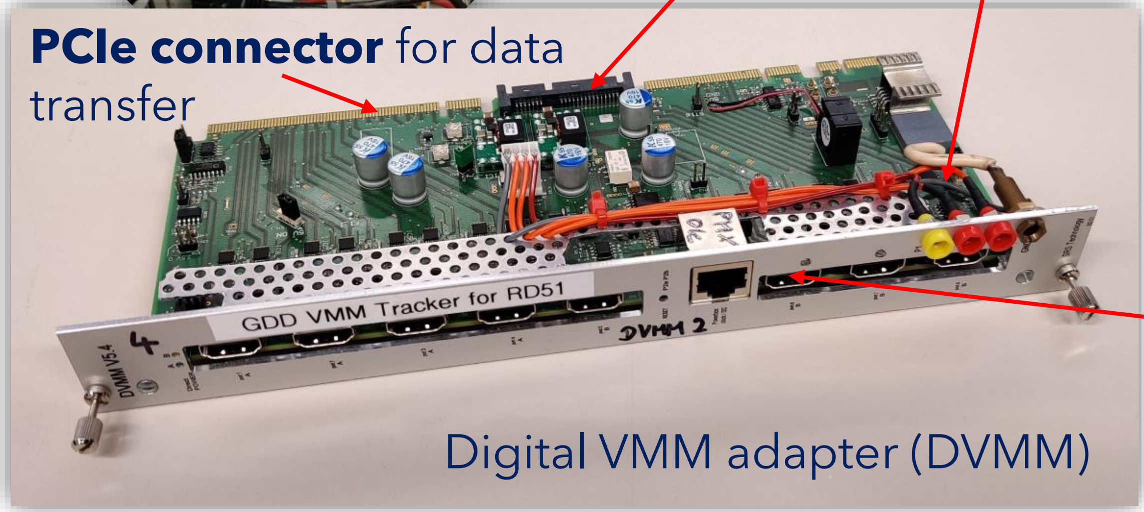
Scalable Readout System (SRS) – DVMM

Detector
↓
SRS front-end *"hybrid PCB"*
↓
ASIC-specific adapter card
↓
Common Front-End Concentrator (FEC) card
↓
DAQ PC



SATA power

Power over HDMI (2m) or PMX for longer cables



HDMI for clock, data and config

Scalable Readout System (SRS) – FEC

Detector

↓

SRS front-end *"hybrid PCB"*

↓

ASIC-specific adapter card

↓

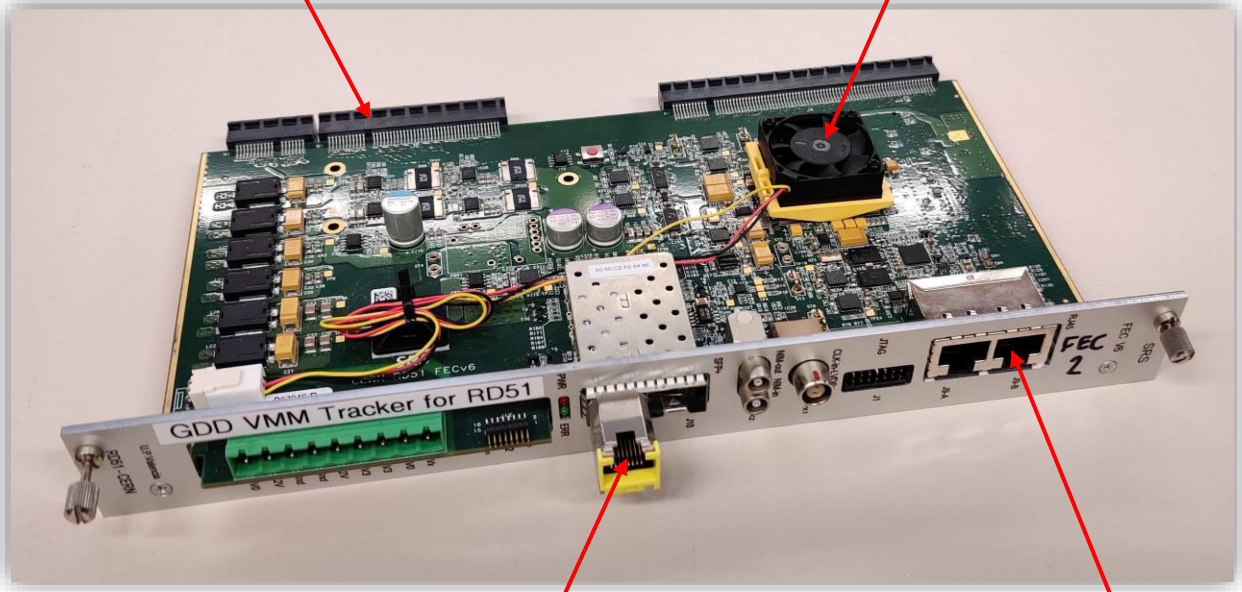
Common Front-End Concentrator (FEC) card

↓

DAQ PC

PCIe connector for data from adapter card

Virtex 6 FPGA



Gigabit Ethernet transceiver for data output

Ethernet for clock synchronisation in the case of larger multi-FEC system

Addition of chip ID to each hit

Coarse CKBC overflow counter added to each hit

Continuous data stream send

Maximally 21 Mhits/s (Gbps Ethernet)

Multi-FEC systems

Detector

↓

SRS front-end *"hybrid PCB"*

↓

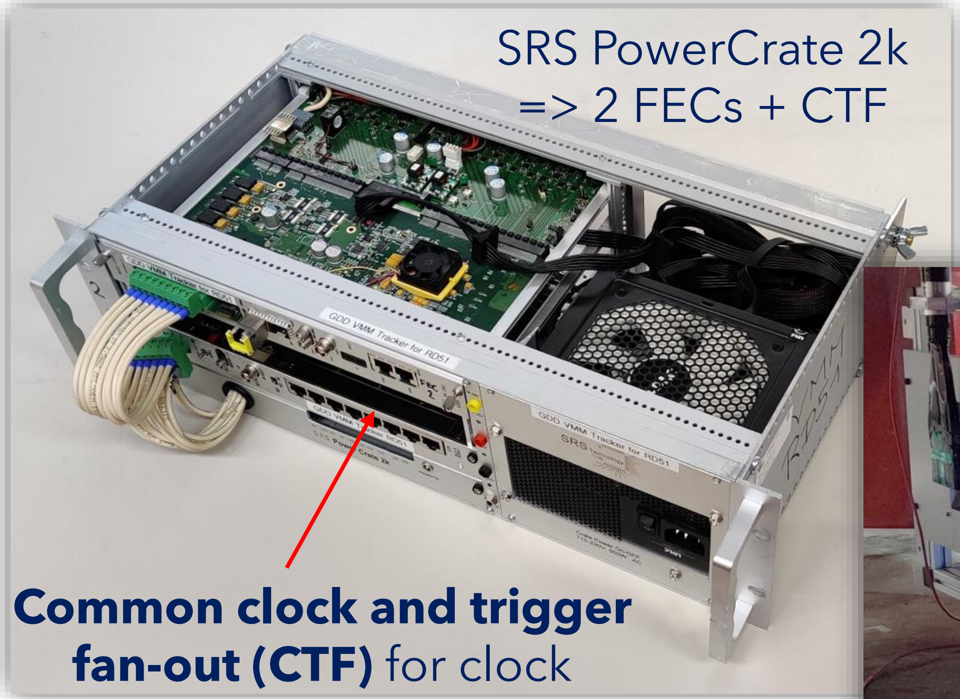
ASIC-specific adapter card

↓

Common Front-End Concentrator (FEC) card

↓

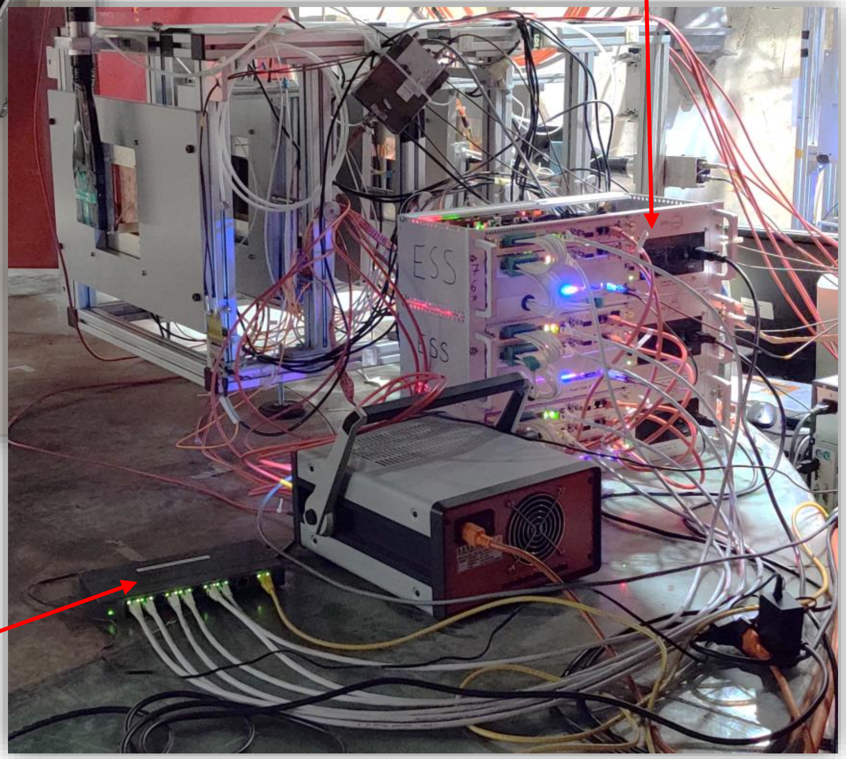
DAQ PC



SRS PowerCrate 2k
=> 2 FECs + CTF

Common clock and trigger fan-out (CTF) for clock synchronisation between front-end concentrators

Multiple crates together



Switch for data from multiple FECs

Data processing software

FEC → Switch → DAQ PC → tcpdump → Cluster reco. → Track reco.

FEC

FEC

⋮

Custom control software

https://gitlab.cern.ch/rd51-slow-control/vmmsc

DAQ PC

Offline analysis

https://github.com/ess-dmsc/vmm-sdat (Cluster reco.)

https://gitlab.physik.uni-muenchen.de/Jonathan.Bortfeldt/anamicom (Track reco.)

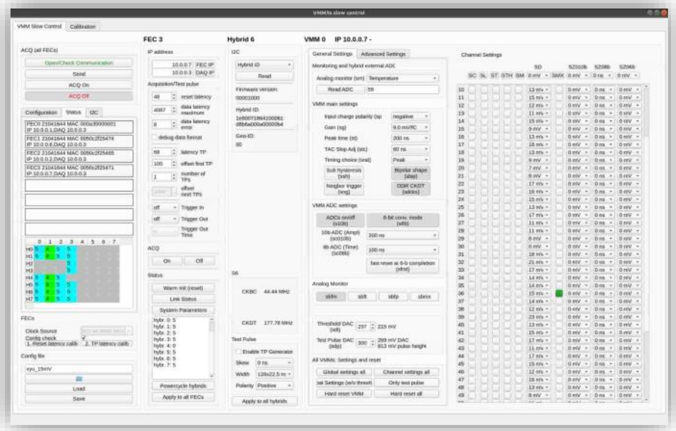
DAQ PC ↓ EFU

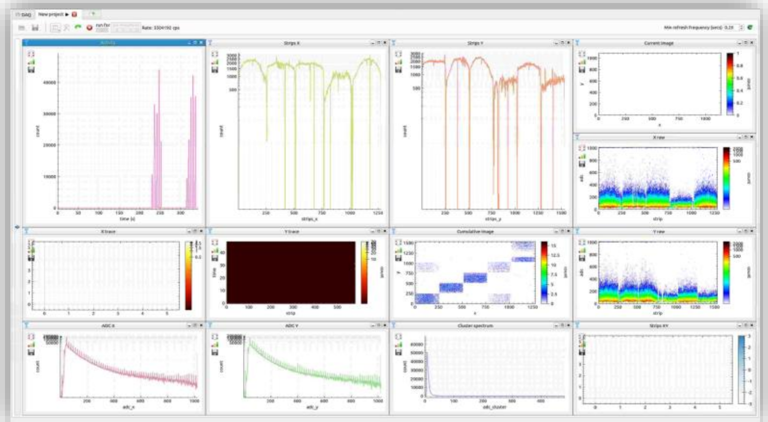
Online monitoring of clusters

EFU → kafka → Online monitor.

https://github.com/ess-dmsc/event-formation-unit (EFU)

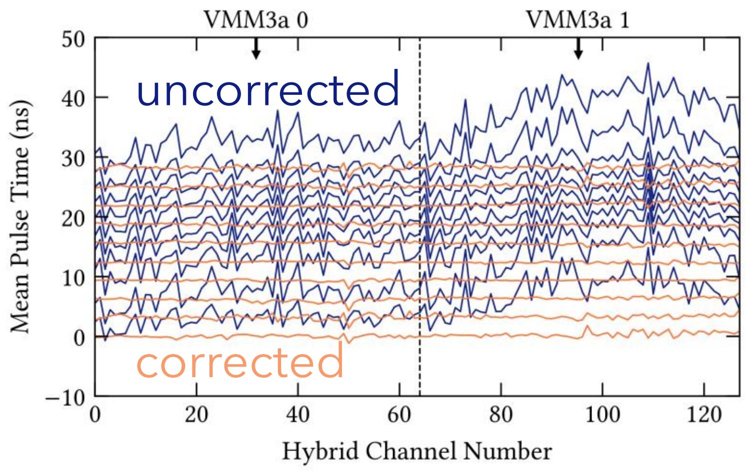
https://github.com/ess-dmsc/daquiri (Online monitor.)



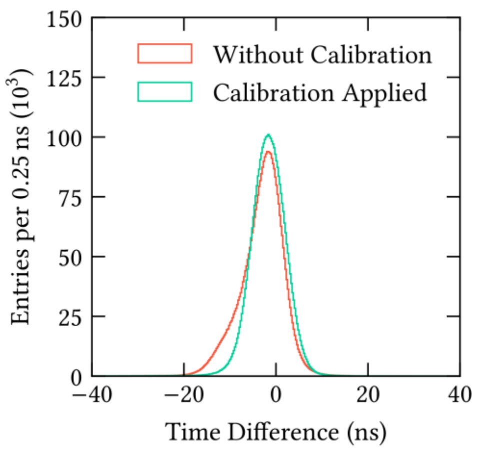


Characterisation with test pulses (timing)

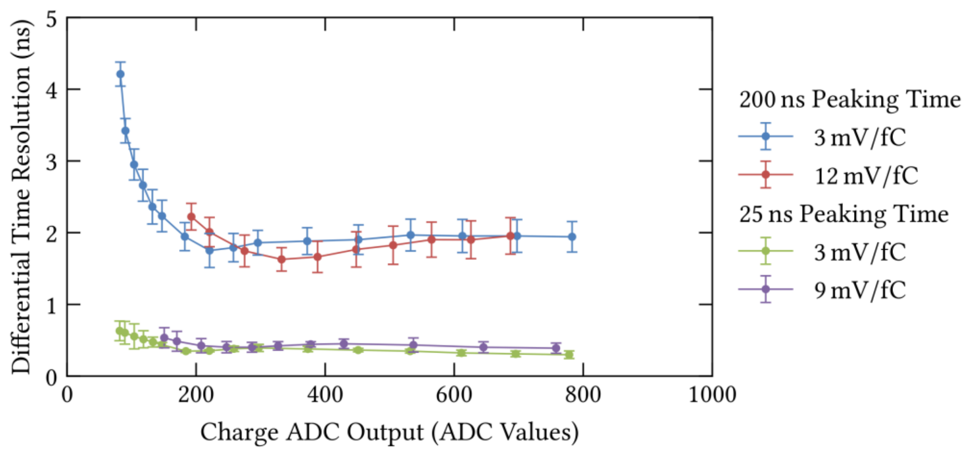
- 8-bit TDC with 60 ns TAC slope => theoretically 240 ps time resolution
- Requires **correction procedure**



Shift test pulse and measure arrival time per channel



Time difference between readout planes

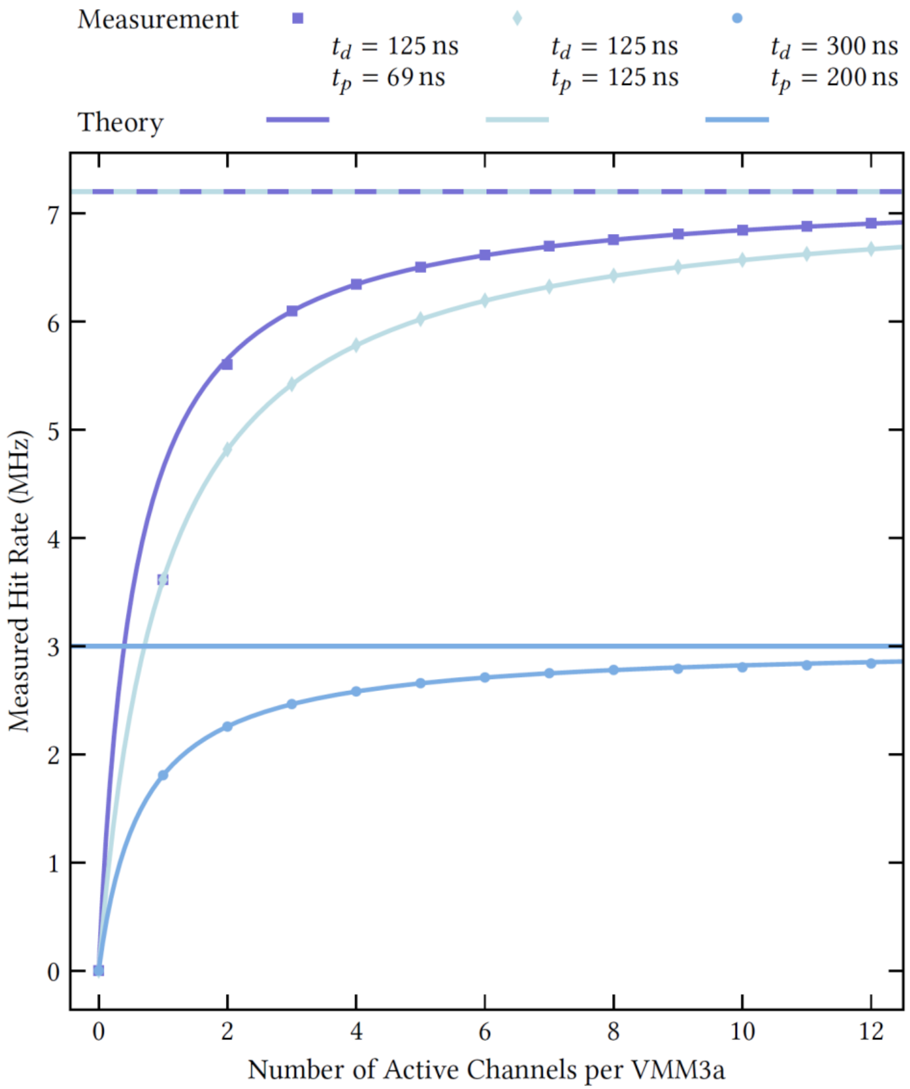


Differential time resolution for different peaking times and electronic gains, depending on the signal amplitude

Characterisation with test pulses (rate)

- Rate-measurements with test pulses
- For details see
  - https://doi.org/10.1016/j.nima.2022.166548
  - https://www.lhc-ilc.physik.uni-bonn.de/ergebnisse/dateien/t00000127.pdf
- Observation 1:

  Strong dependence of rate capability on token clock (CKTK) frequency $f = 1/t_d$, but also token loop reset time t_p



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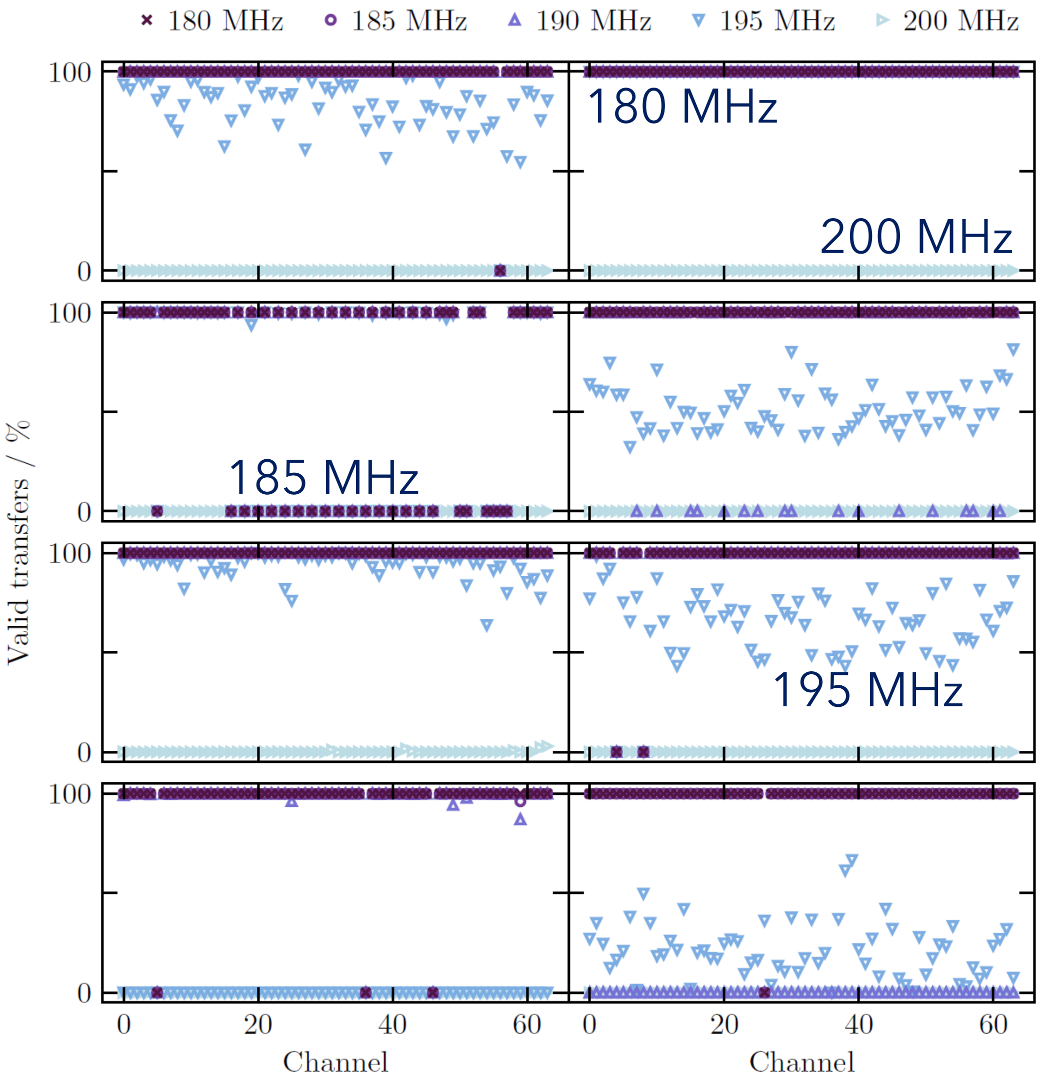
- Observation 1:

  Strong dependence of rate capability on token clock (CKTK) frequency $f = 1/t_d$, but also token loop reset time t_p
- Observation 2:

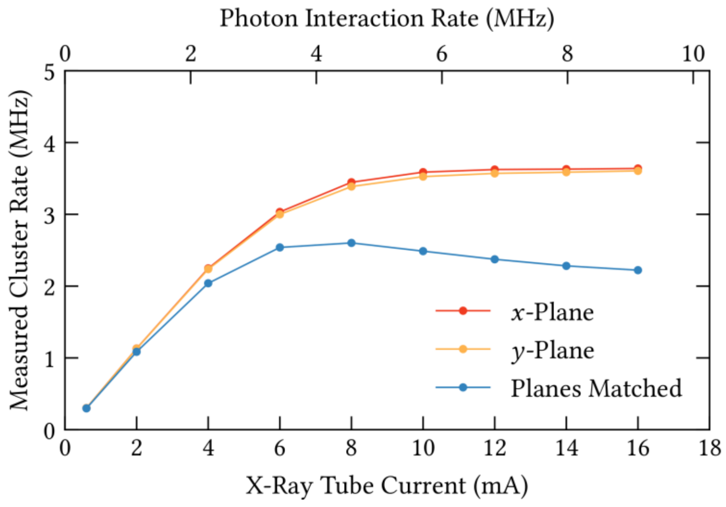
  Data transmission clock has a maximum, which is around 180 MHz in dual edge transmission



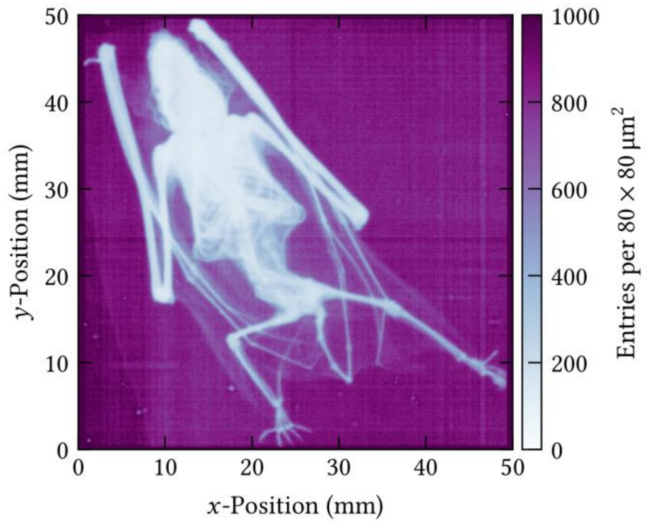
High-rate measurements (X-ray)

See also here: https://doi.org/10.1016/j.nima.2022.166548

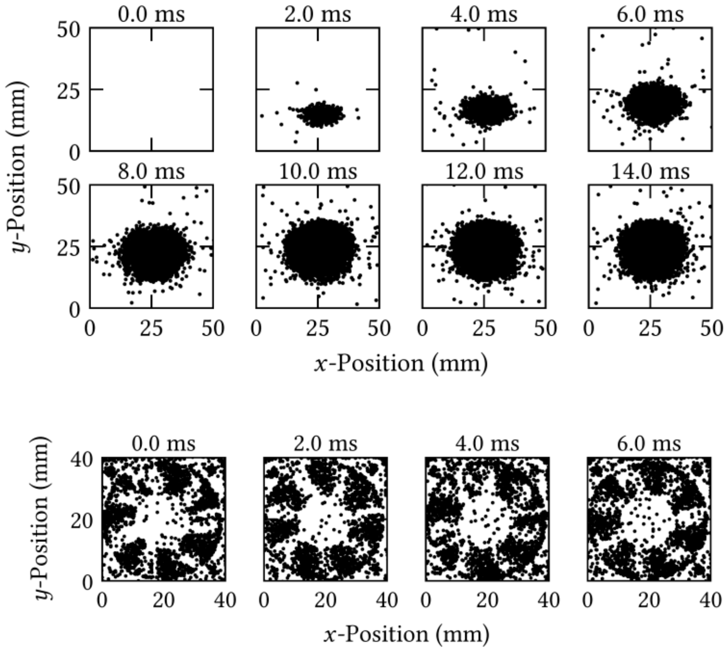
- Measurements with copper target X-ray tube
- Rate-optimised setup: 1 hybrid per FEC (18 Mhits/s per hybrid), 2 FECs
- Triple-GEM detector, x-y-strip readout



Saturation of recorded interaction rate
Cluster contains ~5 strips per plane



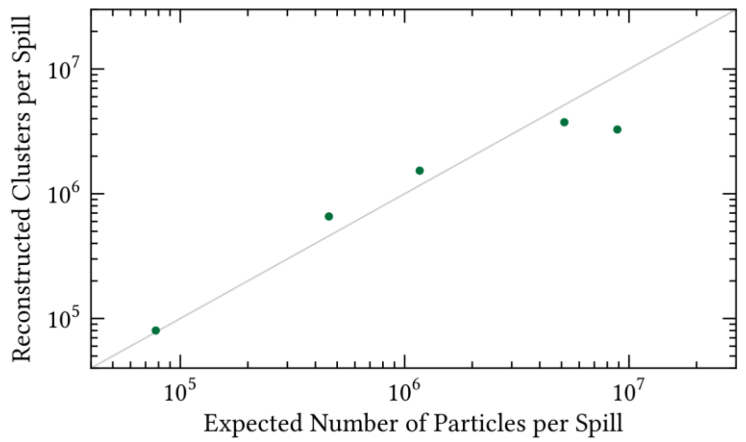
High-rate X-ray imaging
(280×10^6 recorded photons in 3 minutes)
Access to energy, position and time of photon

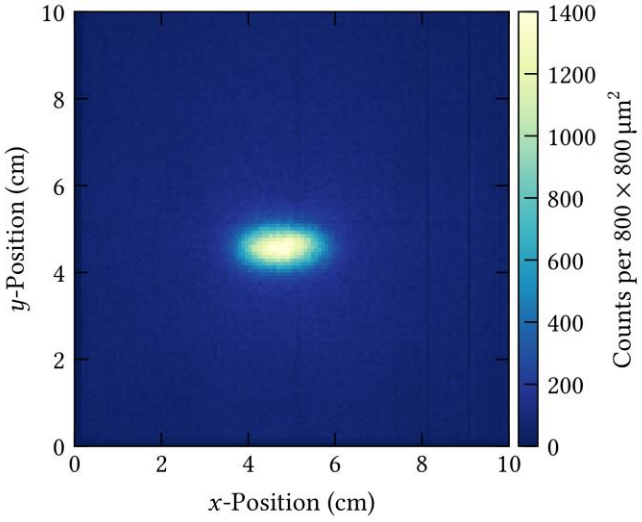


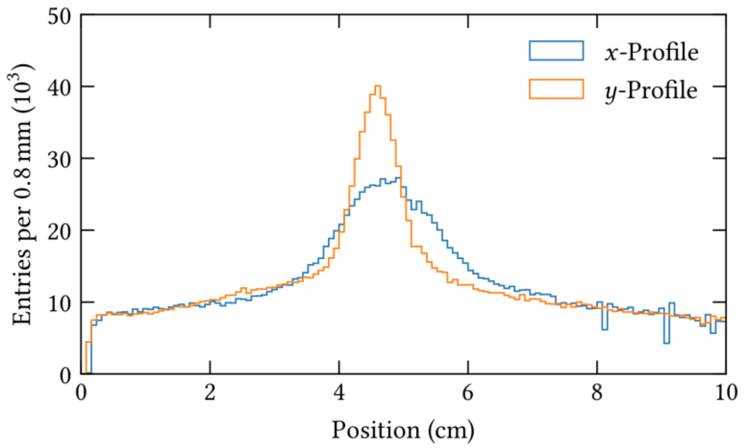
Record moving processes
(4000 photons per 2 ms frame)

High-rate measurements (MIPs)

- 80 GeV/c pion beam @ H4 line of CERN SPS
- Increase the particle flux from ~7 x 10^4 particles per spill (~5 s) to 10^7 particles per spill







- Until ~1.5 x 10^6 particles per spill everything can be recorded
- With ~5 x 10^6 particles per spill and more => saturation effect of VMM readout scheme

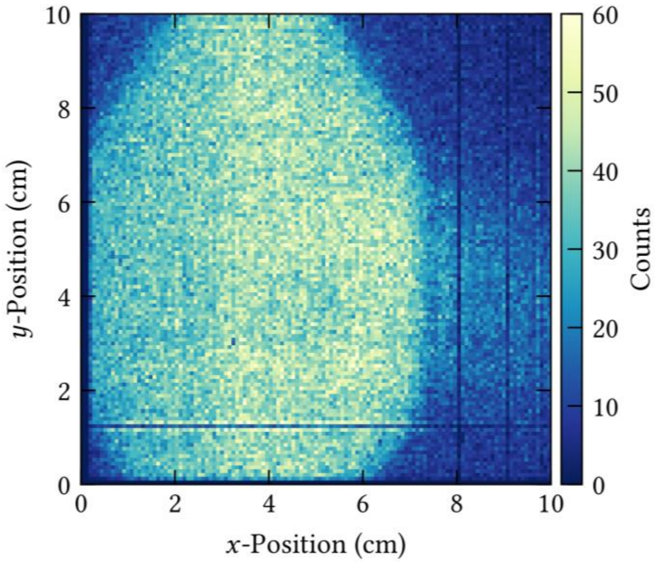
Live beam monitoring

- Due to rate-capability and continuous readout

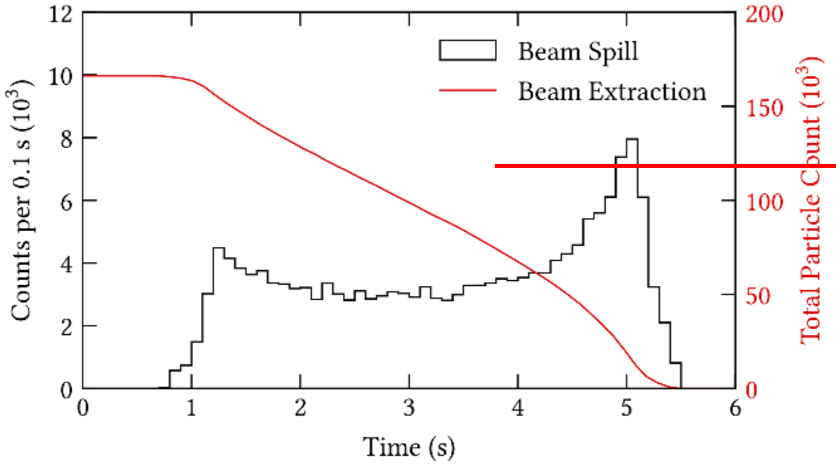
  => Reconstruction of (more or less) each individual beam particle
- Measure the extraction profile of the SPS beam spills to the North Area

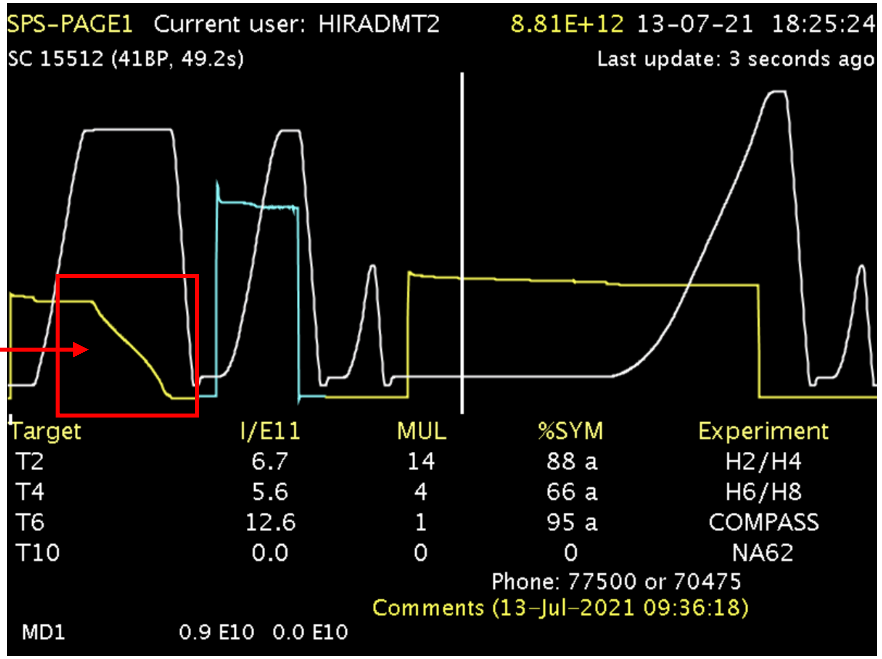
  => Compatible with SPS Page 1

Beam profile



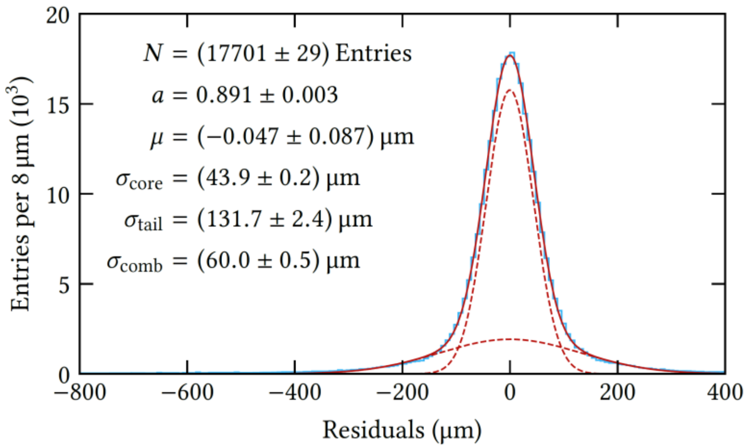
Spill and spill extraction during beam tuning phase

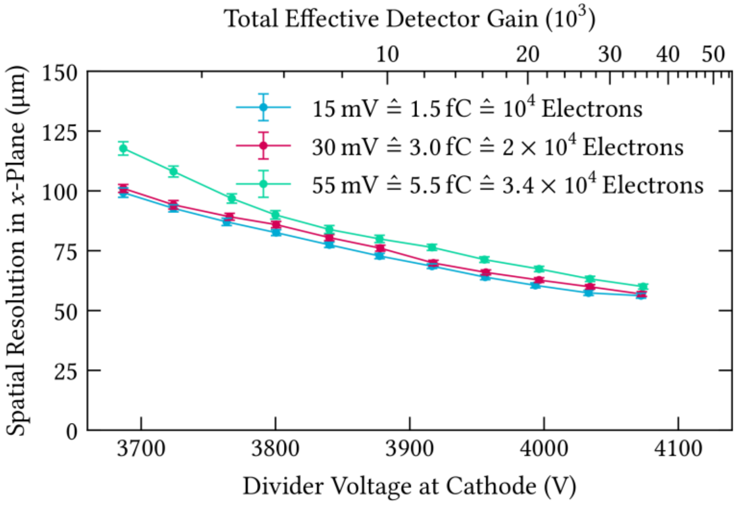


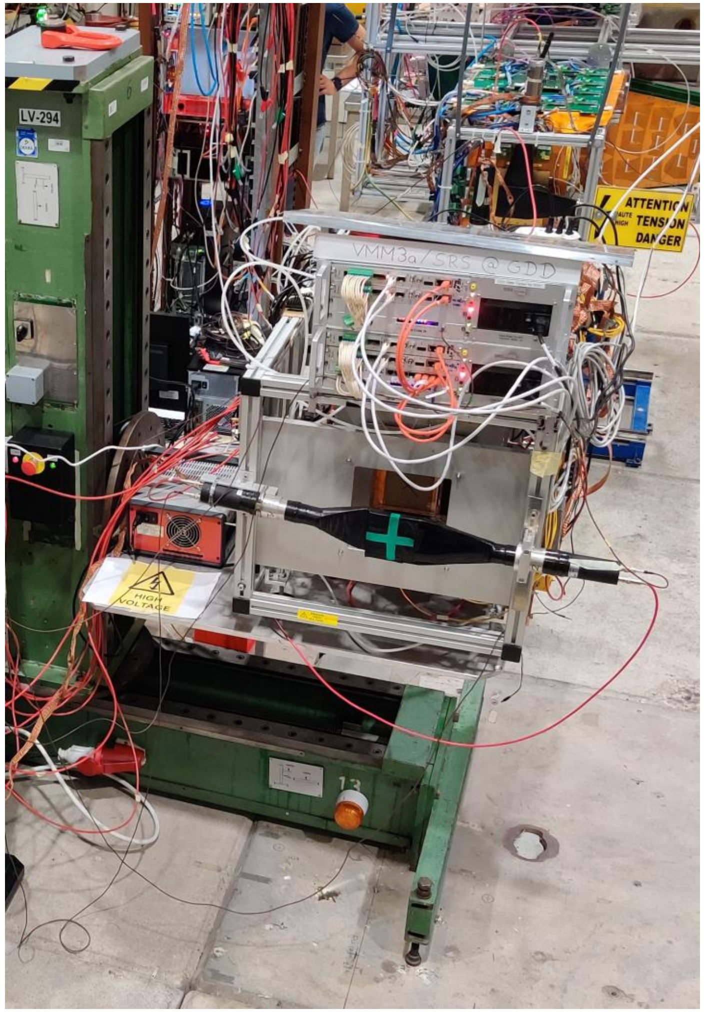


Spatial resolution measurements

- Spatial resolution measurements with beam telescope
- 3 tracking detectors + up to 3 DUTs + scintillator/PMT/NIM signals
  - 24 + 1 hybrid = 3200 readout channels
- Position reconstruction via **Centre-Of-Gravity** (COG)
- Due to diffusion: **spread of charge** over several read-out channels

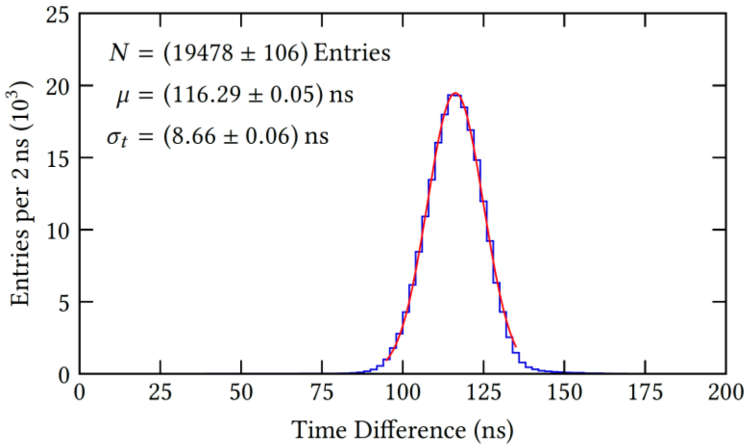


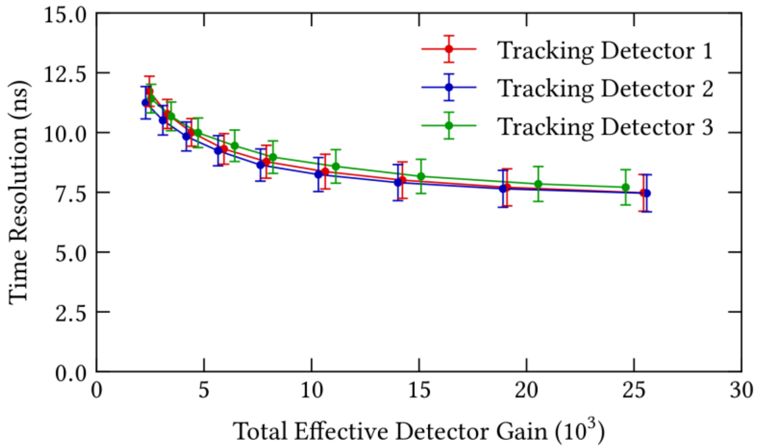


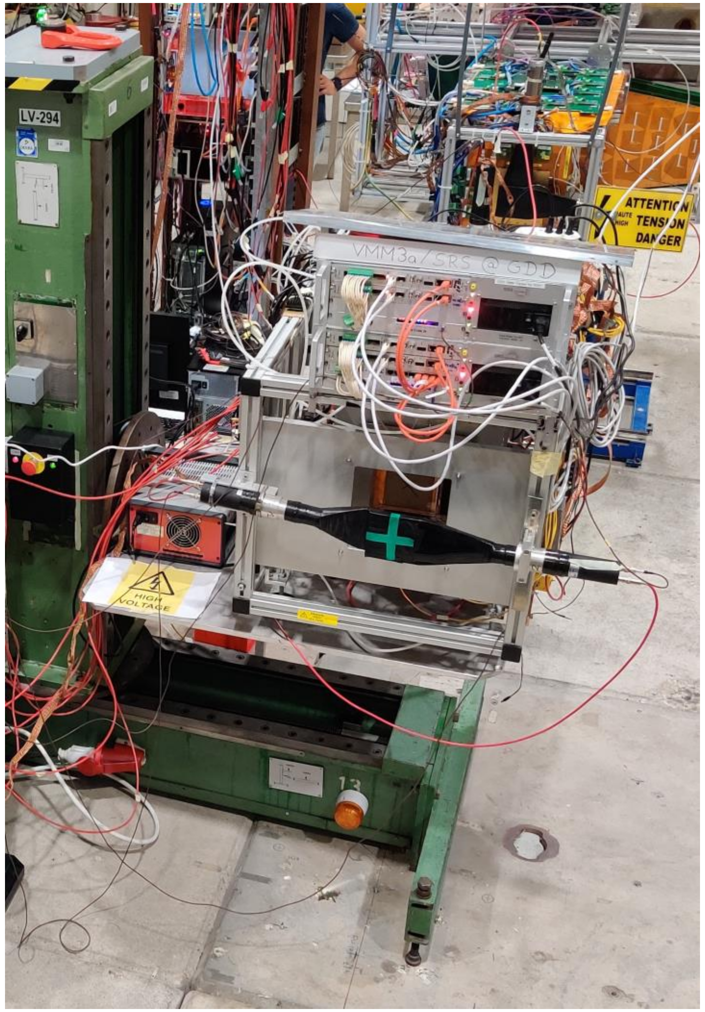


Time resolution measurements

- Time resolution of the electronics between 0.5 and 2 ns
  - With VMM3a/SRS: **no external TDC required**
  - Now: all integrated within a single system
- Time resolution determined by comparison with either the tracking detectors themselves or, as here, comparing with scintillator signals recorded with VMM3a/SRS

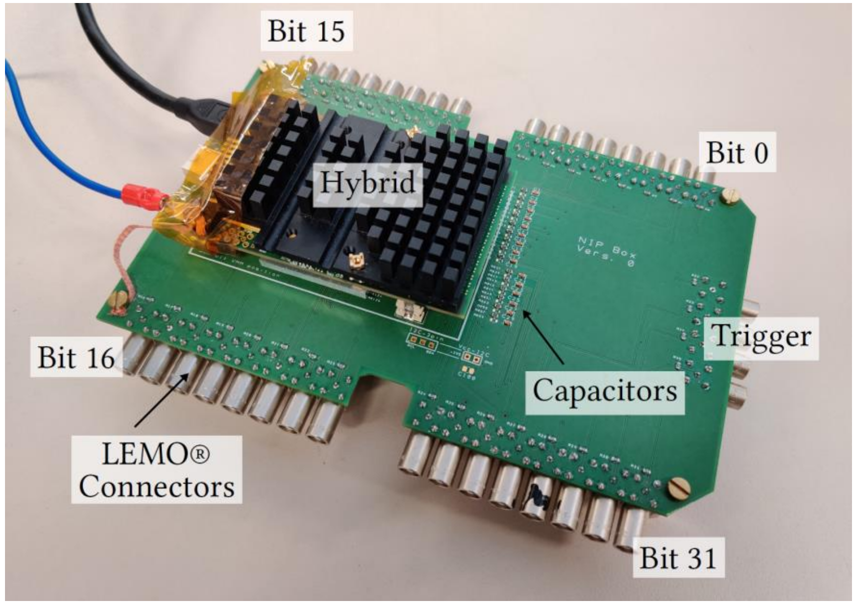




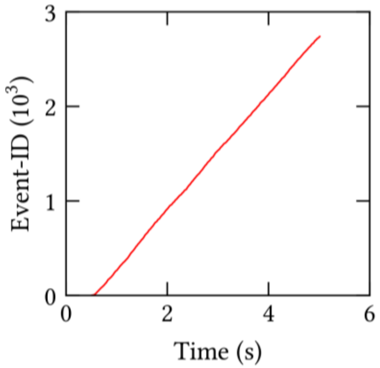


Self-triggered in a triggered experiment

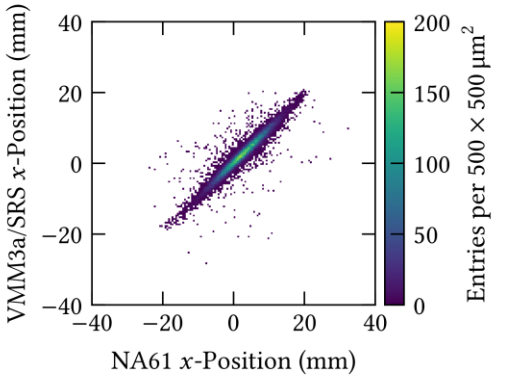
- Integration of self-triggered RD51 VMM3a/SRS beam telescope into triggered NA61/SHINE experiment at CERN SPS
- Inject event-ID generated from NA61 into VMM3a/SRS data stream
- From LVDS (@NA61 signals) to LEMO to charge pulse (capacitor @NIP board) to VMM3a input



Event-ID injector



Event-ID for one SPS spill in VMM data



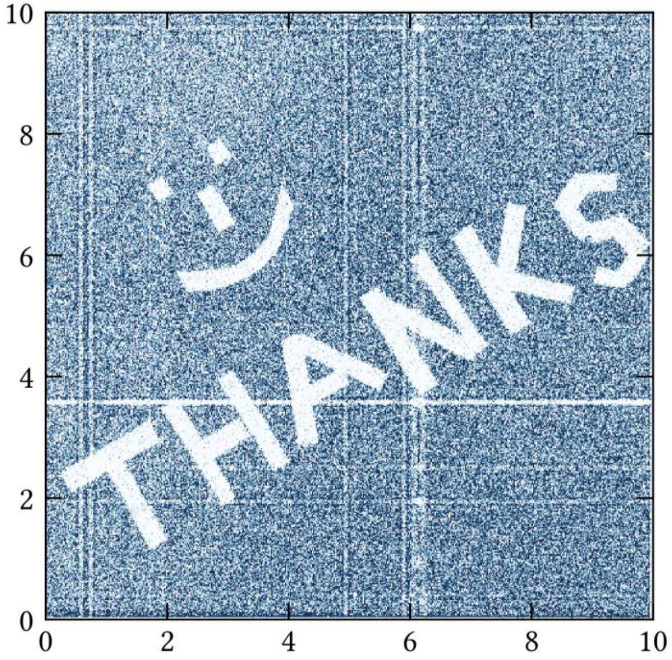
Coordinate correlation

Summary and outlook

- Particle physics experiments set new requirements on detectors and electronics
- By integrating the VMM3a into the RD51 Scalable Readout System, the requirements can be also tackled in small R&D setups and mid-sized experiments
  - MHz rate-capability
  - Nanosecond time resolution
  - Tens of micrometre spatial resolution
  - Large area coverage or multi-detector systems
  - Different detector technologies
- Efforts within the collaboration have been successful

- Upgrades in the future:
  - Spartan-7 on hybrid will allow integration of other readout modes in addition
  - New version of the FEC with higher bandwidth and processing power

For more details on measurements and applications with VMM3a/SRS:
https://doi.org/10.1016/j.nima.2020.164310
https://doi.org/10.1016/j.nima.2021.165576
https://doi.org/10.1016/j.nima.2022.166548



for your attention!

SPONSORED BY THE
Federal Ministry of Education and Research

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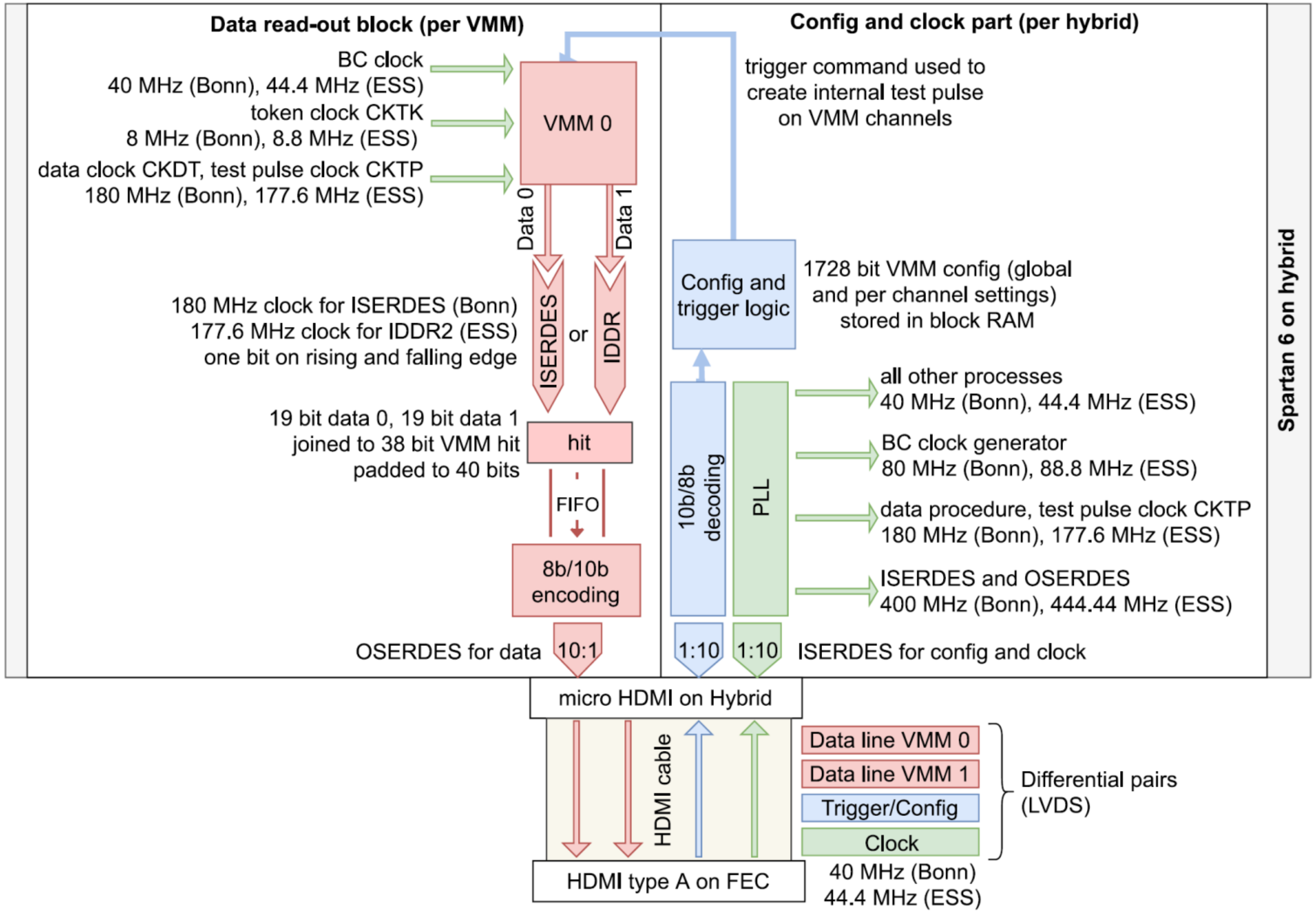
This project has received funding from the European Union's Horizon 2020 Research and Innovation programme under GA no 101004761.

EP R&D

The work has been supported by the CERN Strategic Programme on Technologies for Future Experiments. https://ep-rnd.web.cern.ch/

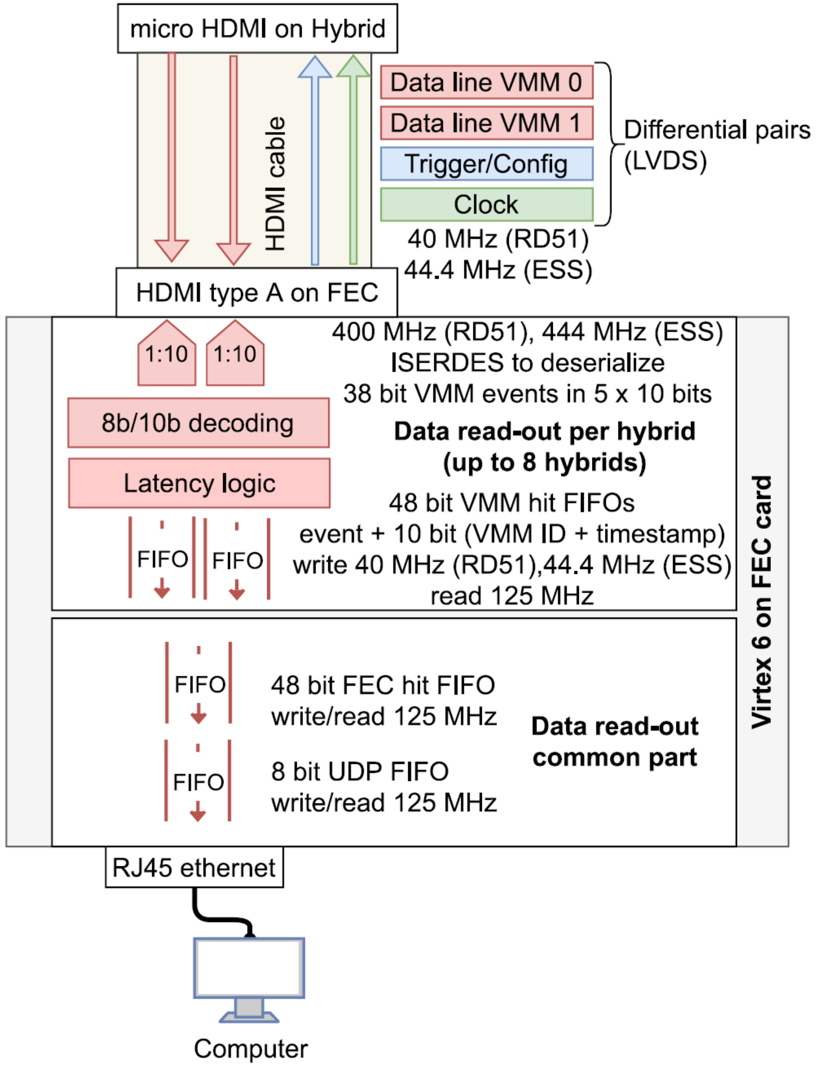
Back-up slides

VMM3a/SRS firmware (hybrid)



https://doi.org/10.1016/j.nima.2022.166548

VMM3a/SRS firmware (FEC)



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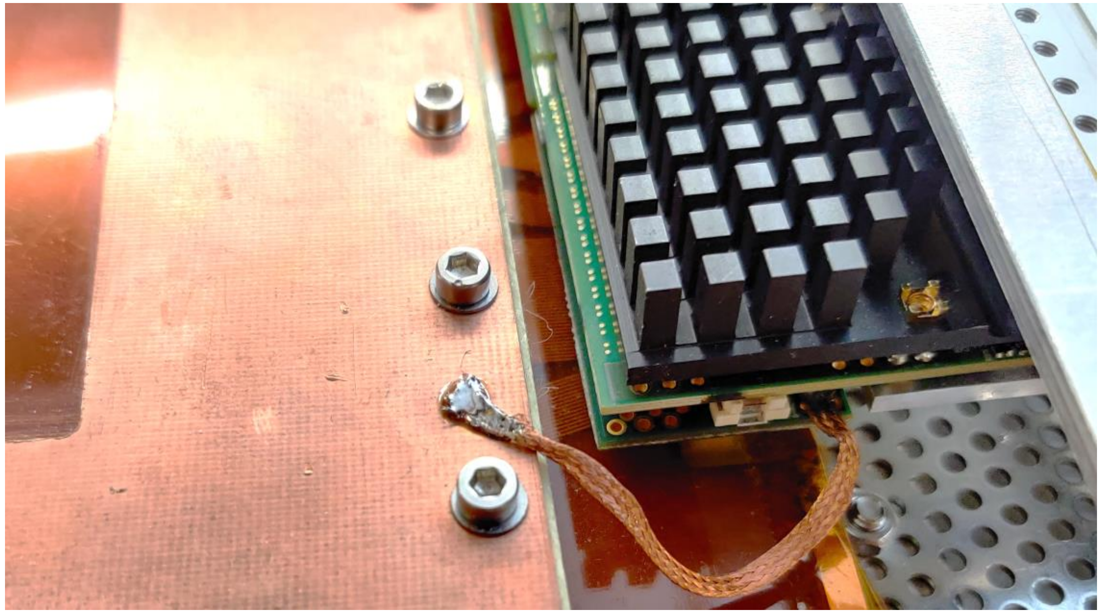
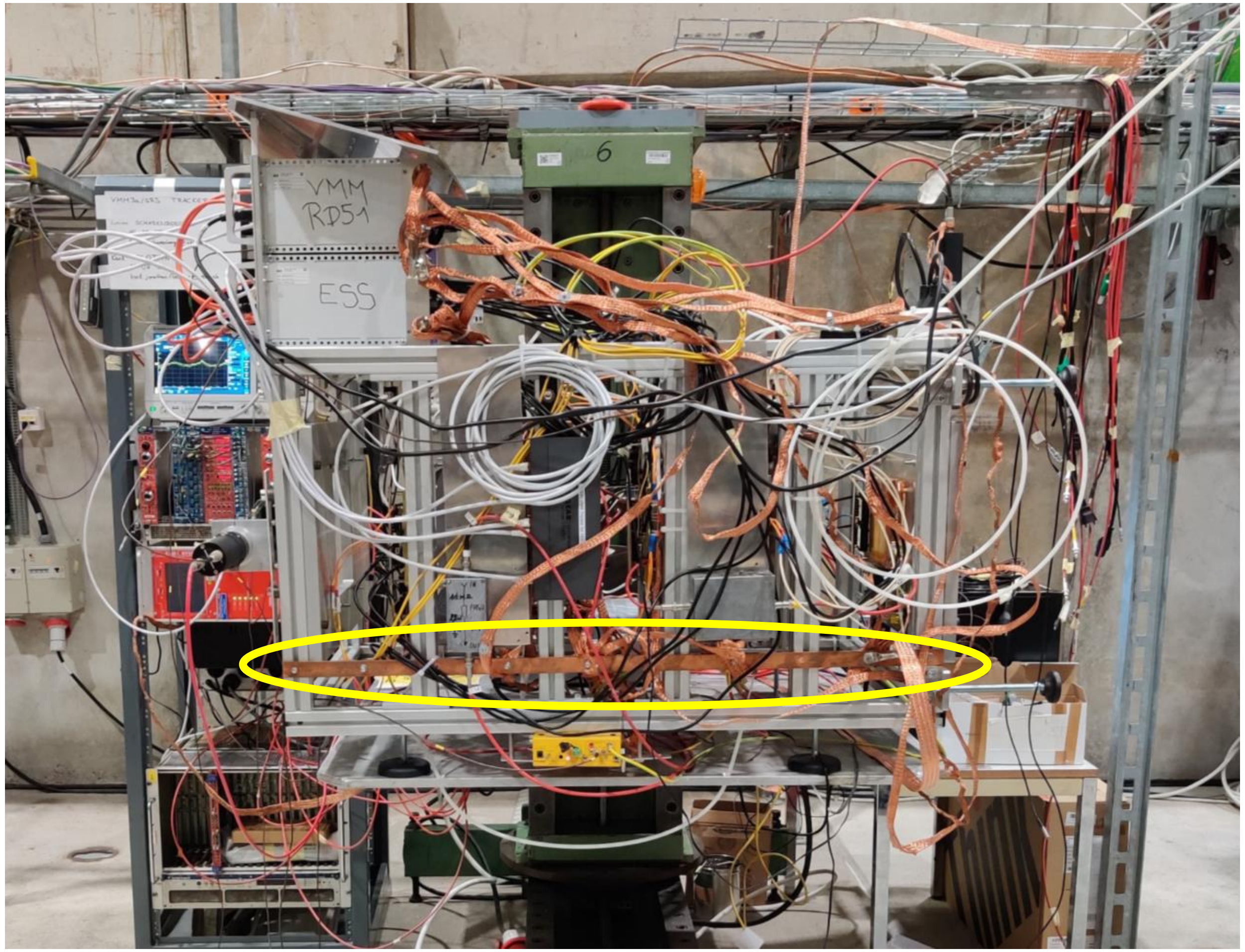
Grounding for low threshold operation

- Improved the common ground
- Improved the analogue and detector ground => Adapter between hybrid and old detector connector introduces lots of noise if not grounded





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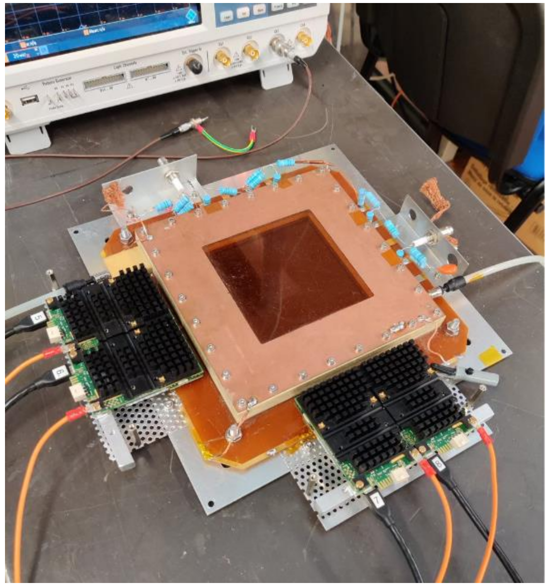
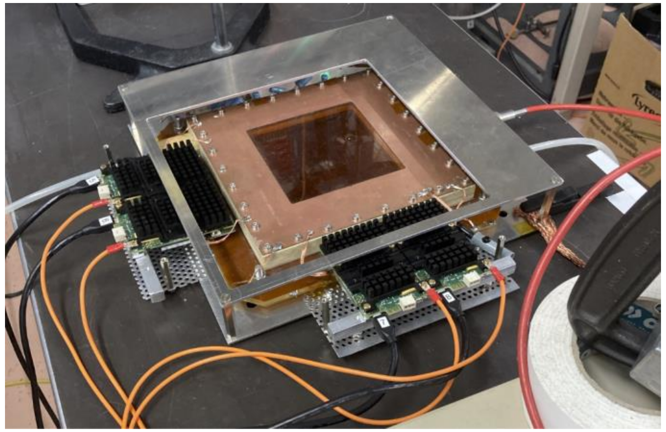
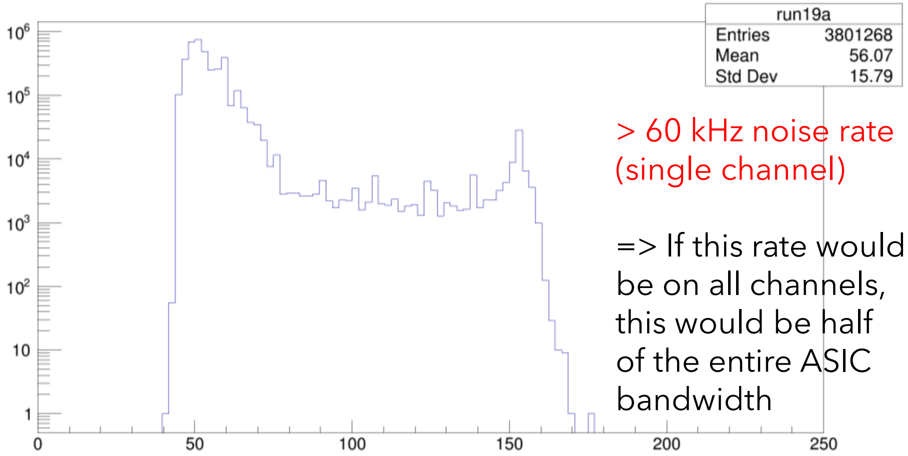


Common ground
Without HV
No adapter ground

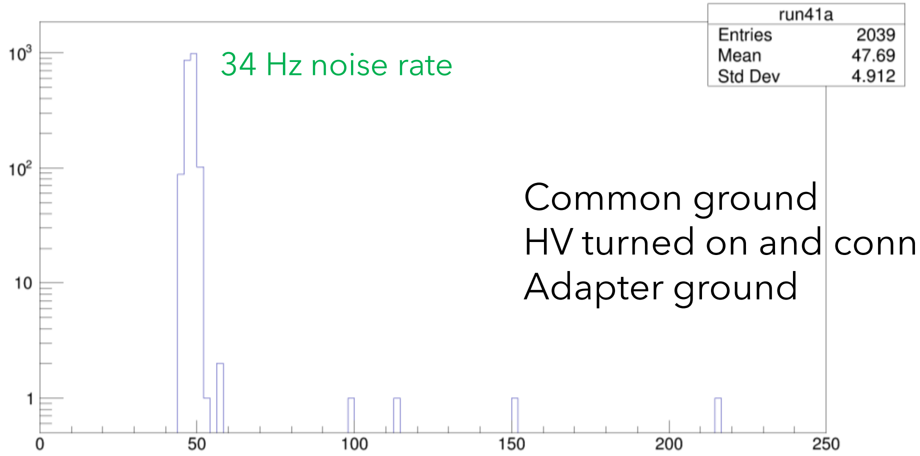




> 60 kHz noise rate
(single channel)

=> If this rate would be on all channels, this would be half of the entire ASIC bandwidth

5 mV THL
60 s of acquisition
Single channel

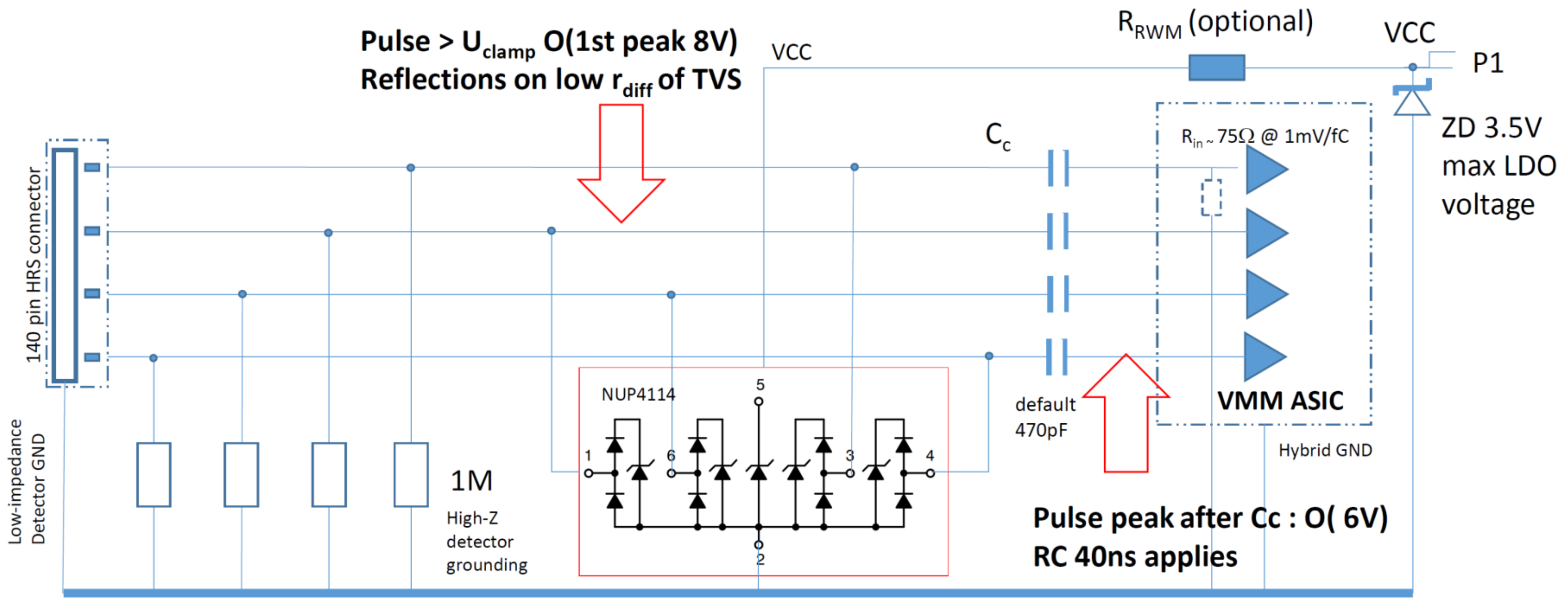


34 Hz noise rate

Common ground
HV turned on and connected
Adapter ground

Discharge protection circuit

VMM hybrid NUP411 input protection scheme



Courtesy of Hans Muller