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Status and recent extensions of the Caribou DAQ System

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Caribou is a flexible open-source DAQ system developed and used within several collaborative frameworks (CERN EP R&D, RD50, AIDAinnova) for laboratory and high-rate beam tests and easy integration of new silicon-pixel detector prototypes. It uses common hardware, firmware and software components that are shared across different projects, thereby reducing the development effort and cost for such readout systems significantly. This contribution presents the structure and capabilities of the DAQ system and shows example implementations for recent monolithic CMOS pixel sensors with sub-nanosecond precision requirements for timing measurements.

Summary (500 words)

Developing a new silicon detector requires significant effort for preparing the readout hardware and software for the prototype to be operated in the laboratory and in test beams. The Caribou DAQ framework significantly reduces the development effort and cost for such readout systems. By utilizing a Xilinx Zynq system-on-chip (SoC) platform, it combines programmable logic and a processing system and thereby brings unprecedented flexibility to the DAQ design. A universal interface card connects the SoC with the detector prototype, housing power supplies for biasing as well as DACs and ADCs for setting and measuring operational parameters, test pulses, etc. Through this versatile hardware and the modular design, the turnaround time for supporting new detectors is minimized. The system is completed by a set of configurable firmware blocks for commonly used functionality as well as the DAQ software Peary. Hardware and software interfaces to EUDAQ2 and SPIDR-based beam telescope DAQ systems allow for an easy integration in commonly used test-beam setups. The Caribou system is developed and used within several collaborative frameworks (CERN EP R&D, RD50, AIDAinnova).

This talk gives an overview of the Caribou system and presents recent applications and developments, such as the integration of new detectors: FASTPIX is a monolithic pixel sensor demonstrator with sub-nanosecond time resolution implemented in a modified 180 nm CMOS imaging process. The DPTS and APTS are monolithic prototype chips using a modified 65 nm CMOS imaging process. Readout of the 16 analog channels of the APTS is achieved using a 16 channel ADC with 14-bit resolution at 65 MSPS, which was integrated in Peary for beam-test measurements.

A Time-to-Digital-Converter (TDC) implemented on the Caribou FPGA is under development. It allows for precision timing over large time spans and is required for the Time-of-Arrival (ToA), Time-over-Threshold (ToT), and position encoding used in the FASTPIX and DPTS test chips with asynchronous digital readout. The DPTS readout requires a time resolution better than 100 ps for both rising and falling edges with no dead time for the position encoding, while at the same time a ToT on the order of tens of microseconds limits the achievable rate for the oscilloscope based readout currently integrated in Caribou. First timing results for the new FPGA TDC implementation obtained from test-pulse injections show that the required performance is achievable with a proper calibration of the TDC bins.

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