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# Design and Performance Optimisation of the Hexaboards for CMS HGCAL On-Cassette Readout Electronics

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We present the design and performance of the Hexaboard, a complex hexagonal multi-layer PCB equipped with multiple HGCROC ASICs to read out the signals from silicon pads with low noise and large dynamic range. The Hexaboards are glued to silicon sensors and connect to them via wire bonds through holes in the PCBs. The Hexaboard also connects to mezzanine boards for powering, data concentration and data transfer. More than 10 variants of the Hexaboard are required to cover the circular fiducial area of the CMS endcaps. Detailed performance measurements, and comparative PCB simulations using ANSYS SIWAVE, will be presented

## Summary (500 words)

The High-Granularity Calorimeter (HGCAL) is to replace the Endcap Calorimeter in ongoing phase-II upgrades for HL-LHC operations. The HGCAL is a 47-layer sampling calorimeter comprising electromagnetic (ECAL) and hadronic (HCAL) parts, using both silicon and scintillators as active materials. Silicon in 8”hexagonal shape comes in 3 different thicknesses (120 µm, 200 µm, 300 µm) and two pad sizes (0.51 cm2 & 1.18 cm2). Silicon will be used in the ECAL and the innermost layers of the HCAL sections, where the fluences are the highest, whilst plastic scintillator tiles coupled to SiPMs, will be used in HCAL, where dose and fluence permit.

There will be nearly 600 m2 of silicon sensors managed in the form of modules on cassettes. Modules are constructed from glued assemblies of rigid thermally conducting baseplates, silicon sensors, and hexagonal printed-circuit boards, known as Hexaboards, which will be the focus of this talk. Hexaboards use the HGCROC front-end ASICs to read the deposited energy from Si-diode pads wire-bonded via stepped through holes. Partial sections and the complex tiling of the cassette results in more than 10 Hexaboard variants and extremely demanding constraints. A specialized 8-layer stack-up with mid-layer bonding pads accessible by step holes, two layers with 100Ω controlled differential impedance for 1.28 Gbps and 320 MHz differential routing, and double-sided shield layers for the HGCROC analog channel connections from the Si pads. It must also provide a sensor bias voltage up to 1kV, guard ring, and module shield layer connections.

Besides its own design complexity and many design variants, the baseline architecture imposes very tough space constraints and many connecting mezzanine boards are to be adjusted in very limited vertical space.

Many prototypes of hexaboards were produced to optimize the design before mass production. The first version of hexaboards was produced with 8-layer stack-up where the most sensitive Analog channels of HGCROC that bonds to Si sensor routed on L5 were not dually covered by ground (GND) planes, and supply layer L3(VDDD) and L4(VDDA) were placed adjacent without any ground between them and have much digital modulated noise on analog channels.

Many iterations of HGCROC host boards were required, shielding the analog channels layer and keeping VDDD and VDDA on the same layer to avoid their mutual parallel coupling and placing a very close GND plane adjacent could reduce the digital noise coupling. Subsequently, the new stack-up was optimized through simulation study using ANSYS SIWAVE during the design phase, and these boards showed improved results under testing. A digital modulation superimposed on the pedestal value of all channels was reduced from ˜65

ADC counts to 3.7 ADC counts. Further measurements showed that the Hexaboard and HGCROC parasitics and grounding scheme have an important impact on the noise, which can be further reduced by a factor of 4 through the correct interconnectivity between the HGCROC and the Hexaboard grounds. This contribution will describe this optimization process and the important lessons learned throughout the investigation

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