Design and testing of long Flexible Printed Circuits for the ATLAS High Granularity Timing Detector demonstrator

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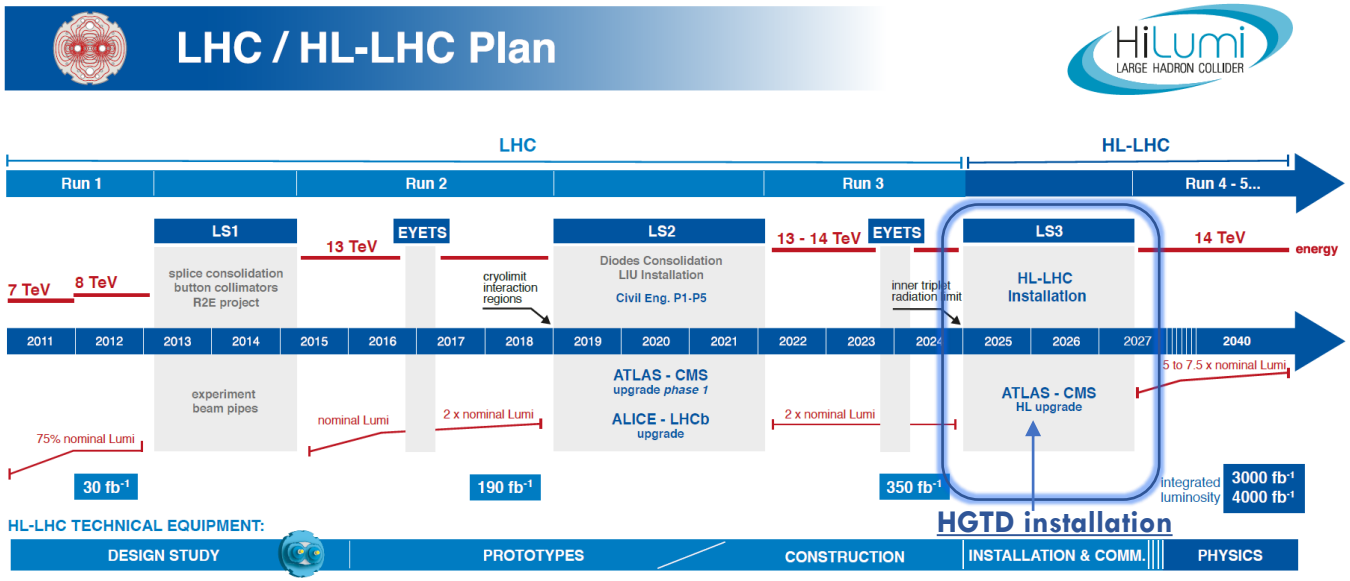
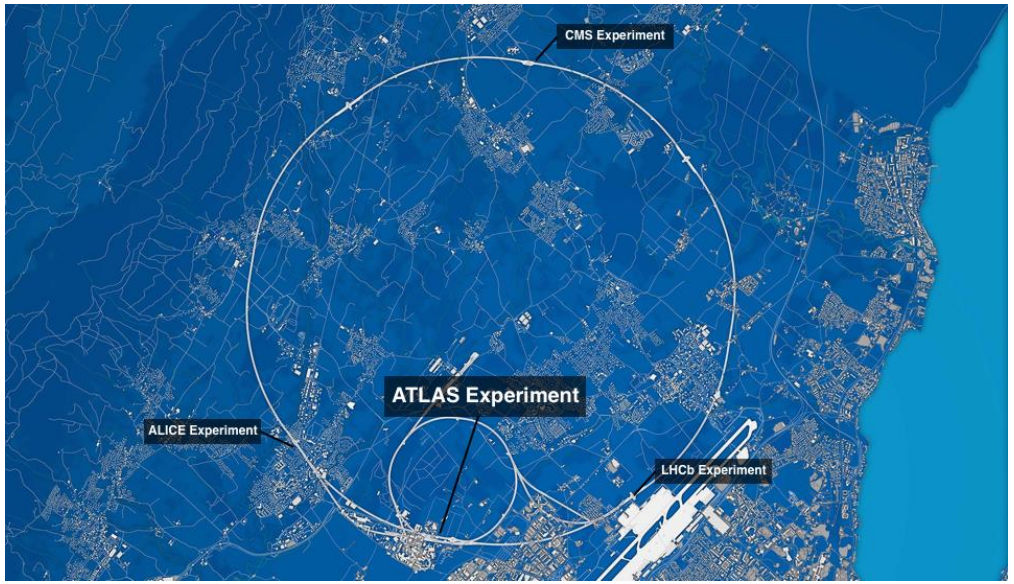
Topical Workshop on Electronics for Particle Physics

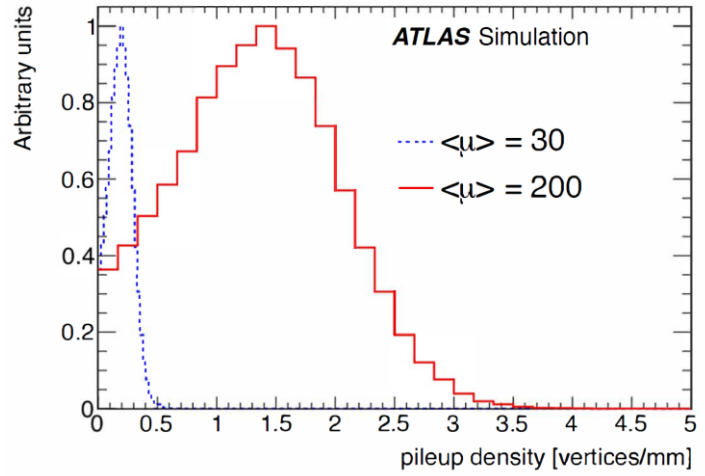
September 19th – 23rd 2022

High Luminosity Large Hadron Collider (HL-LHC) and ATLAS detector upgrade at CERN





- High Luminosity of the LHC → increase the pp collisions per bunch crossing
- Upgrade of the ATLAS systems: Inner Tracker (ITk), Calorimeter electronics, Trigger System. Addition of **High Granularity Timing Detector (HGTD)**
- **Technical Design Report approved in 2020**



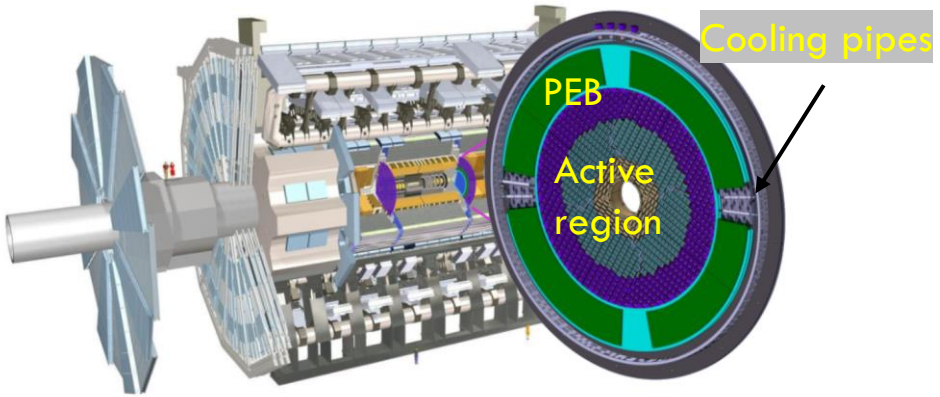
HGTD layout, positioning and main requirements

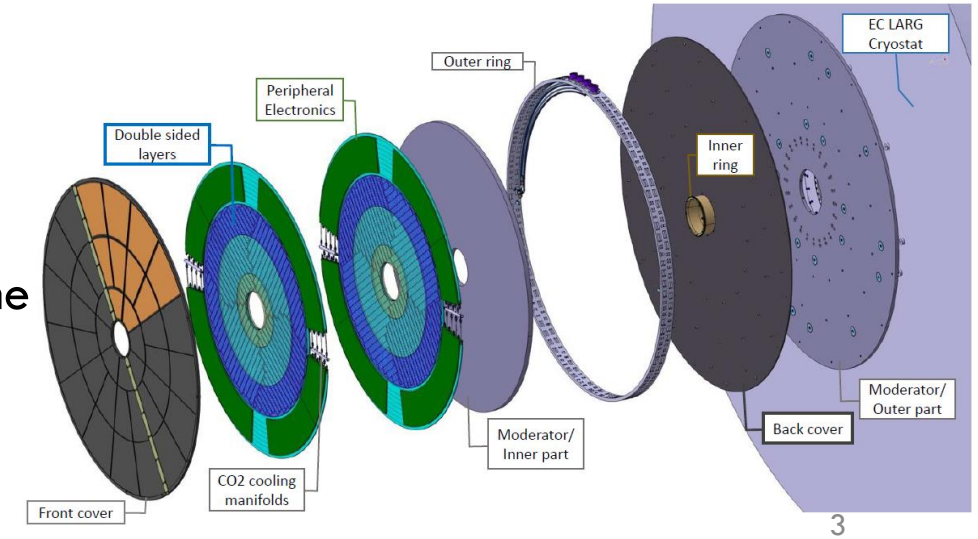
- The **HGTD** will be located between the barrel (outside the ITk volume) and the end-cap calorimeters at **z = ± 3.5m**

- Acceptance between a radius of 120 mm and 640 mm
  - $2.5 < \eta < 4.0$

- **Two instrumented double-sided layers per end-cap**
  - **Modules:** arranged for optimal overlap to achive
    - **σ_t = 30-50 ps per track**
    - Sensor choice: Si-based **Low Gain Avalanche Detector (LGAD),** thickness $\cong 50\ \mu m$

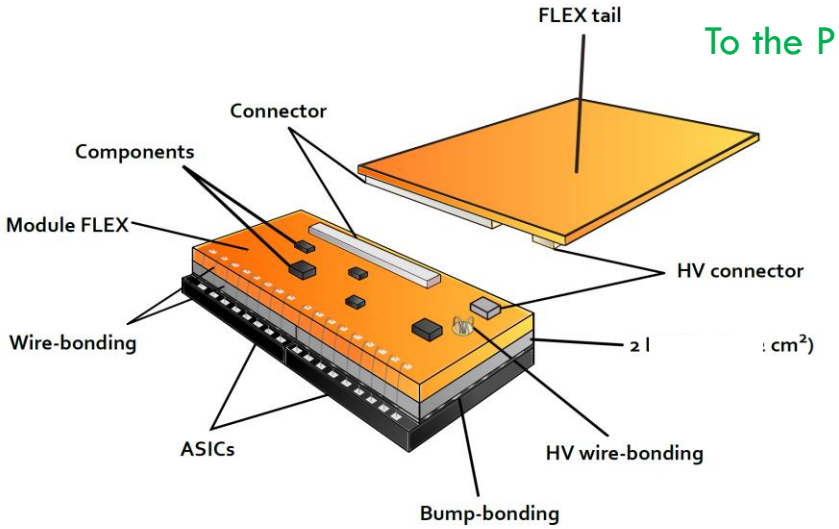
- **Working temperature -30°C** (CO_2 cooling system) to mitigate the impact of irradiation on sensors

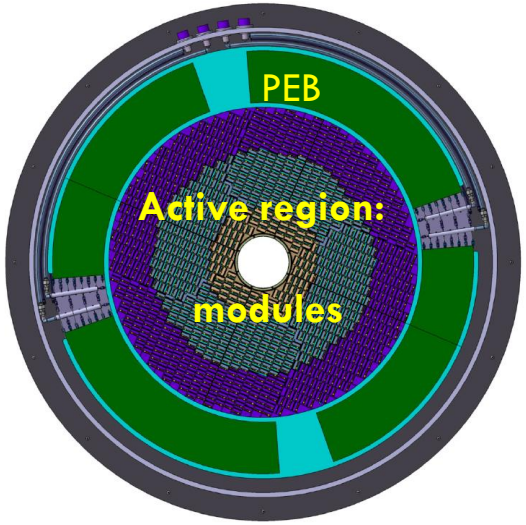




HGTD active detection region: module

- **Module**
  - **2 Sensors:** 2x2 cm^2 each, with 1.3 x 1.3 mm^2 pads
  - **2 ASICs (ALTIROC*):** 2x2 cm^2 each, bump bonded to sensor,
  - **Module FLEX:** wire bonded to the sensor (**bias voltage**) and to the ASICs (**signals and power**)
  - **Flex tail (Flexible Printed Circuit)**
    - Interconnection between the module and the Peripheral Electronics Boards (PEB**)



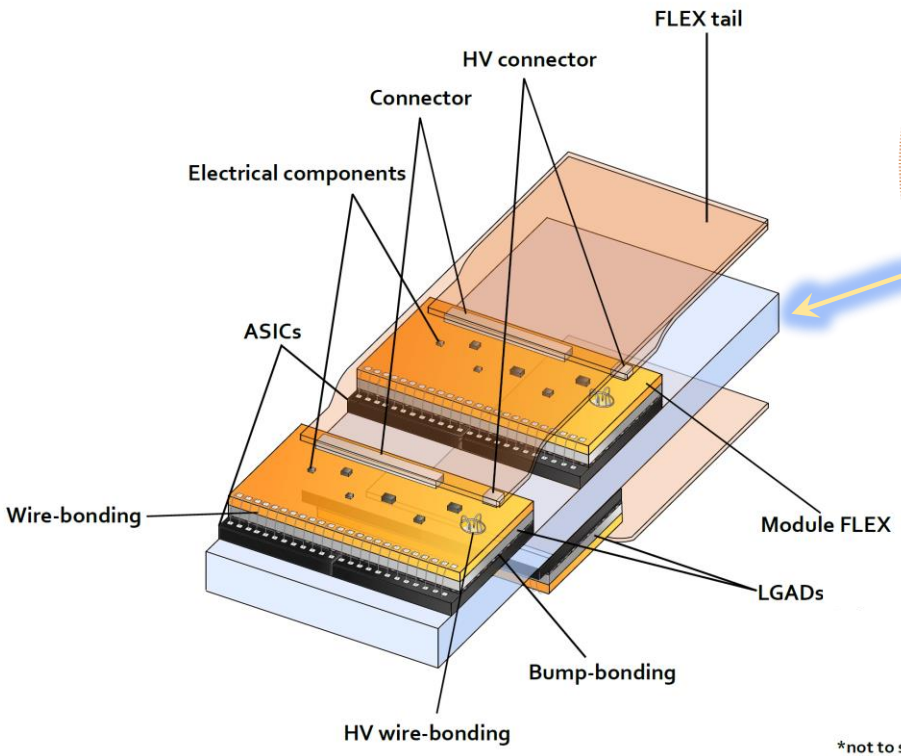


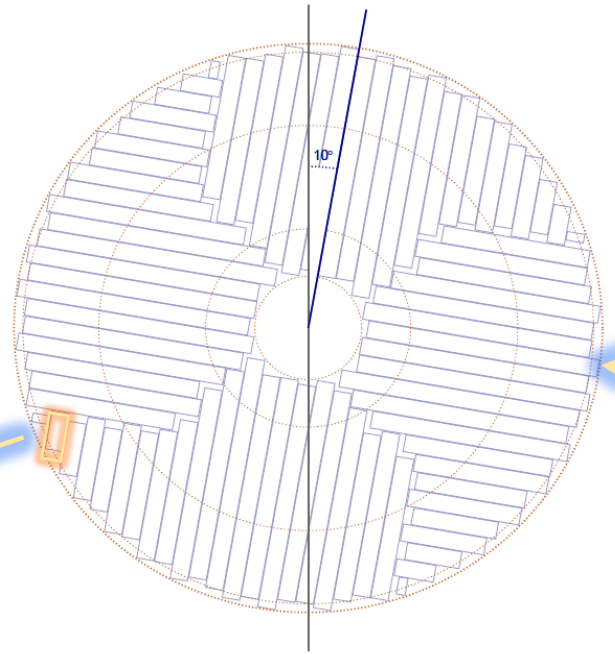
*Performance of ALTIROC2 readout ASIC with LGADs for ATLAS HGTD picosecond MIP timing detector – Maxime Morenas - -20 sept 2022, 14:00

*A high-resolution clock phase shifter circuitry for ALTIROC - Xing Huang -20 sept 2022, 16:40

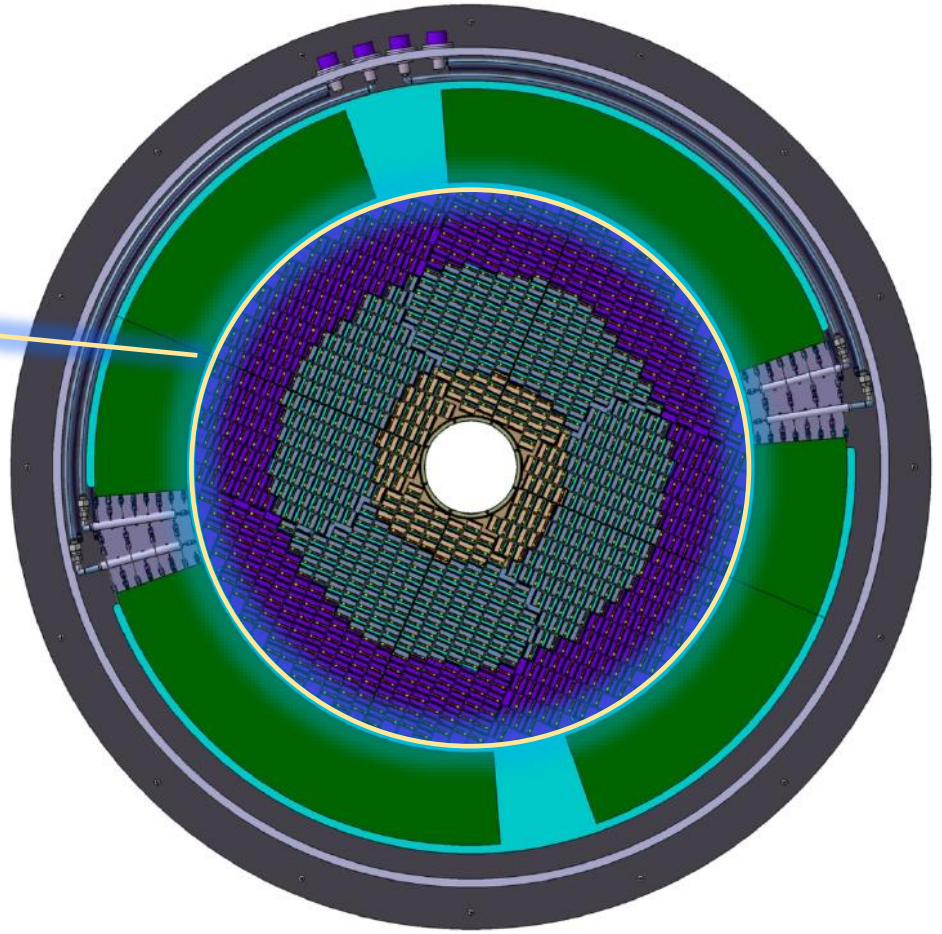
** MUX64, an analogue 64-to-1 multiplexer ASIC for the ATLAS High Granularity Timing Detector – Xu Zifeng – Poster session 22 September 2022 17:40

HGTD active detection region: readout-rows



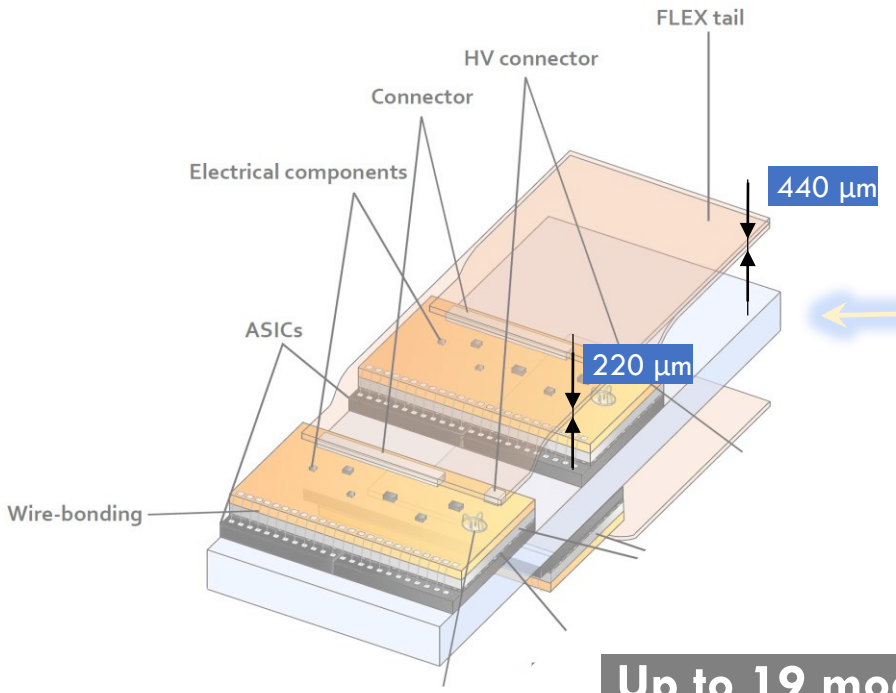


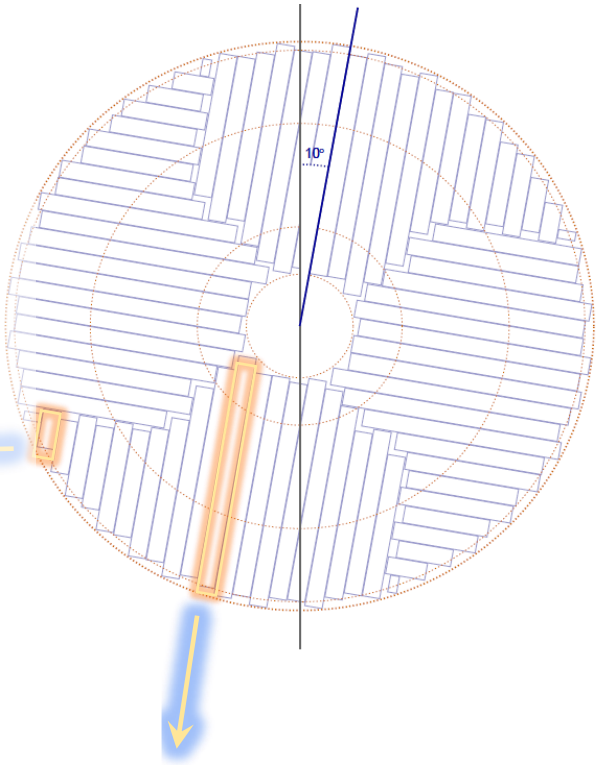
HGTD front view



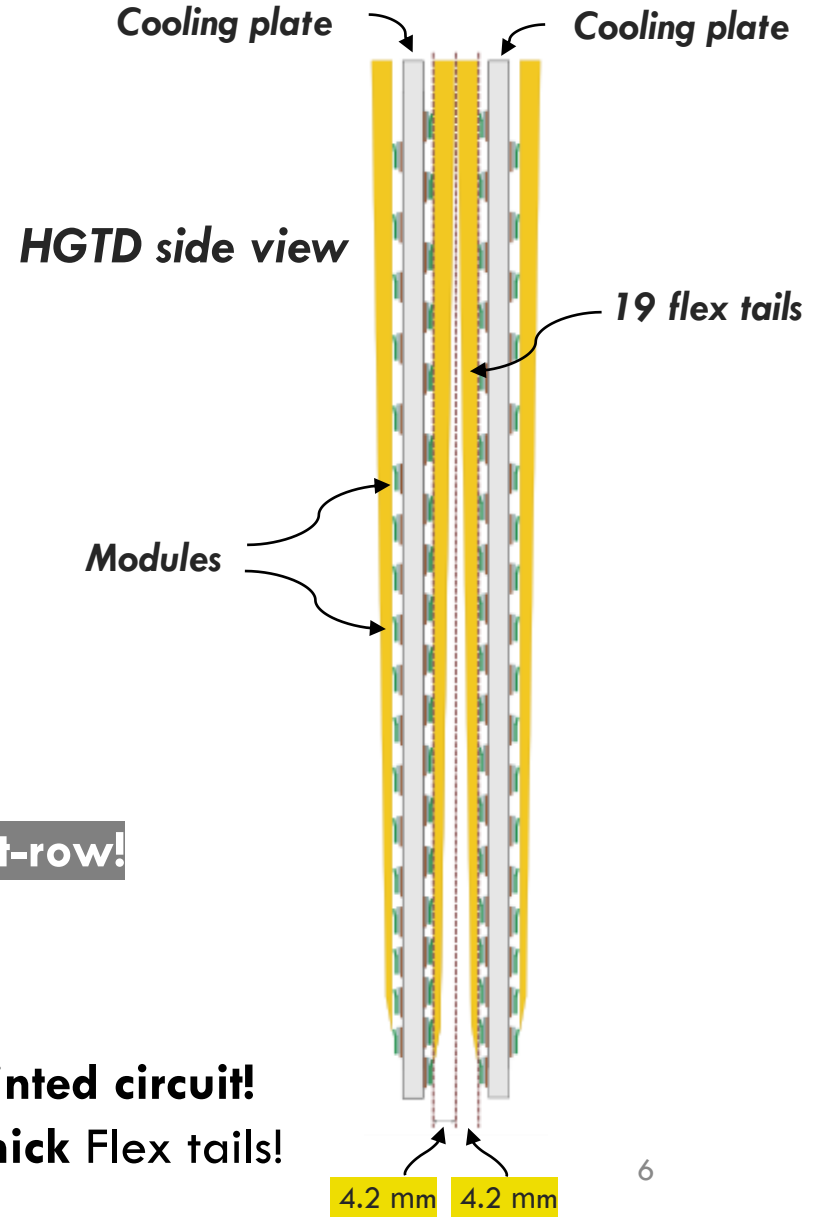
Modules mounted on the cooling plates in **readout rows,**
aligned along the x or y direction

HGTD active detection region: readout-rows and flex tails





Up to 19 modules + 19 flex tails per readout-row!



Different lengths of the flex tails depending on the module positioning

Distance between the innermost module and the PEB **69 cm → Long flex printed circuit!**

Also thickness constraints: *4.2 mm available to stack 19 flexes!* → **220 μm thick** Flex tails!

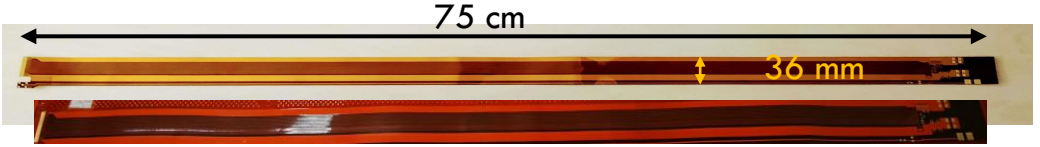
Type and number of lines in the flex tail

- Different type of signals:
  - **High Voltage** (HV) to bias the **LGAD**s
  - **ALTIROC**:
    - **Data transmission** (Luminosity, Timing)
      - **1.28 Gb/s max.**
    - **Clocks**
      - 40 MHz, 320 MHz
    - Monitoring
      - DC level
    - I^2C
    - Power and Ground dedicated planes
      - 1.2V at 1.0 A
  - **NTC** sensor to monitor temperature conditions soldered on the **module flex**

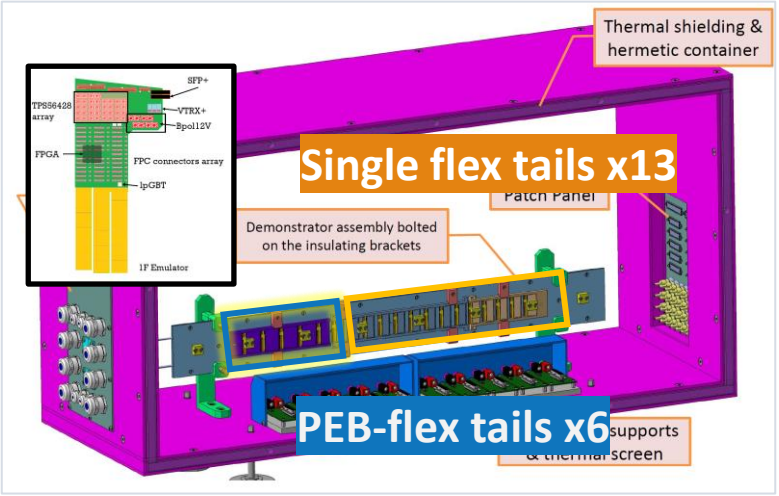
Name	Type	Description	Specification	Channels per module
HV	Power	Single HV line for both sensors. Max: 800V and 2.25mA	Insulation resistance > 800MΩ	1
ASIC LV	Power	Planes or lines for analog and digital power. Max: 1.5V, 1A	R < 2.7mΩ/cm	2
Ground	Power	Planes for analog and digital ground	R < 0.7mΩ/cm	2
I^2C Slow control	Open drain	SCL, SDA	45-65Ω impedance	2
I^2C Slow control	CMOS	Address	Static signal	3
Input clock	Differential CLPS pairs	320 MHz, Fast commands (opt. 40 MHz clock)	90-120Ω impedance	1 pair
Input commands	Differential CLPS pairs	Fast commands	90-120Ω impedance	1 pair
Timing data output	Differential CLPS pairs	Up to 1.28Gb/s speed	90-120Ω impedance	2 pairs
Luminosity data output	Differential CLPS pairs	Up to 1.28Gb/s speed	90-120Ω impedance	2 pairs
ASIC reset	Digital	General reset	45-65Ω impedance	1
Monitoring	DC voltage	Anolog output from each ASIC (including temperature), low voltages and ground common for both ASICs and NTC on module flex	A few mV to 1.2V	7
Debugging	Analog	For ASIC debugging, spare lines	45-65Ω impedance	2

Flex tail for the single readout-row demonstrator: design

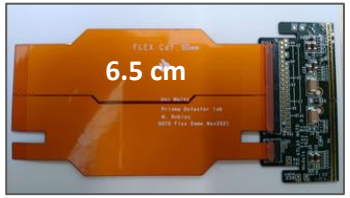
- **Flex tail for the demonstrator**



  - Design based **on previous flex tail design (75 cm long) and prototypes successfully tested:** electrically functional, first thermal expansion tests
    - Same design, seven prototypes from two different vendors
  - **Altiroc2 pinout**
  - **Assumed PEB 1F layout** 6 flexes attached per readout row (TDR PEB layout)
  - **Ground: two separate planes**
  - **Electrical specifications: voltage drop, impedance control, HV insulation**
  - **Single readout-row demonstrator: (validate the choice of the componentes during the R&D period of the HGTD)**
  - **Longest and most populated HGTD readout row: 19 modules**
    - 6 flexes attached to PEB and **13 individual flexes**
  - **Production of 13 different lengths** defined mainly by the position of the connector on the module loaded on the support unit and the connector on the PEB



Sketch of the one readout-row demonstrator vessel: the modules loaded on the support units are assembled on an Aluminum cooling plate



6.5 cm long flex cable tail prototype for the demonstrator attached to a module flex prototype

Flex tail prototypes: stackup

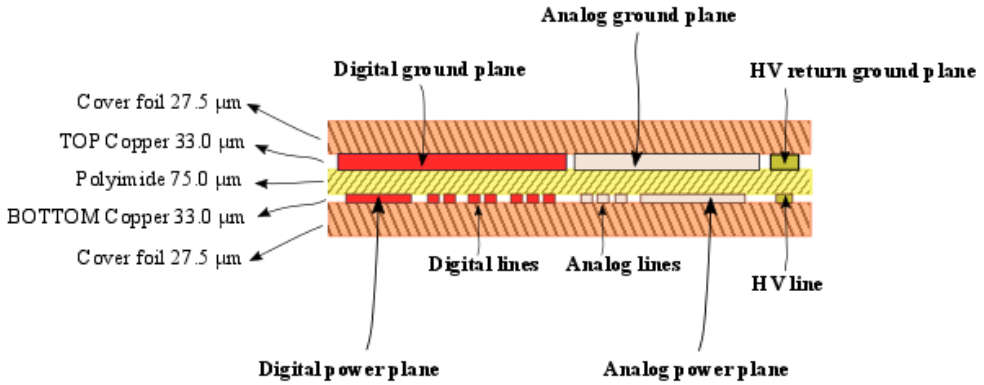
	Stackup Thickness [um]		
Layer	Prototype A	Prototype B	Prototype C*
Coverlay	27.5	13.0+25.0	50.0
Top (Cu)	33.0	28.0	38.0
Polyimide	75.0	50.0	50.0
Bottom (Cu)	33.0	28.0	38.0
Coverlay	27.5	13.0+25.0	50.0
Total thickness	206.0	182	226.0

*To be improved

- **Lines parameters optimized for impedance control:**
  - **Prototype A**
    - **Diff. pairs: 125 µm line - 300 µm gap**
    - **Single lines: 140 µm**
  - **Prototype B**
    - **Diff. pairs: 90 µm line - 335 µm gap**
    - **Single lines: 90 µm**

2-layers design

Prototype A stackup



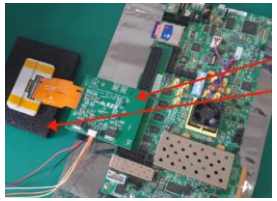
Prototype B stackup

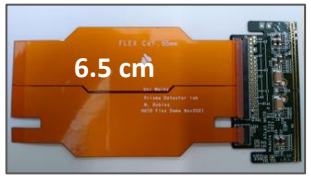
Two ends: flex+ stiffener=219 um ;

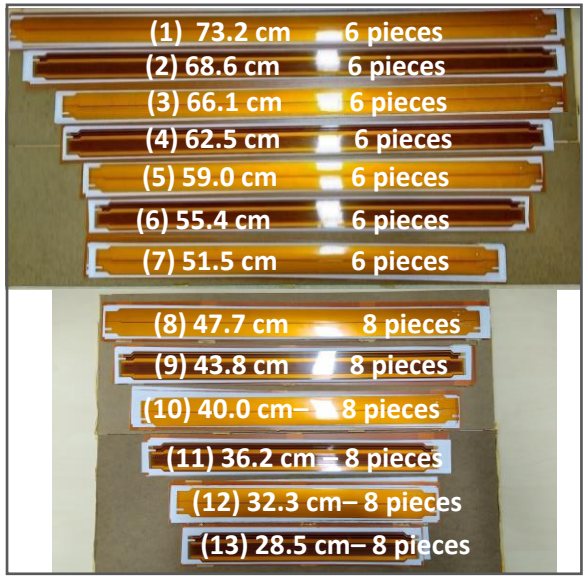
Flex =182 um

Flex tail for the single readout-row demonstrator: prototypes production

- **Prototype A**
  - **Design and production of 13 different lengths**
    - **90 prototypes from 28.5 cm to 73.2 cm length, 36 mm width**
      - **Extra length due to** separation between supports, flex tail being installation, thermal contraction
    - Additional length type (**6.5 cm long**) produced for **testing purposes** on sites (module qualification and DAQ demonstrator communications): **40 pieces**
    - **130 in total**

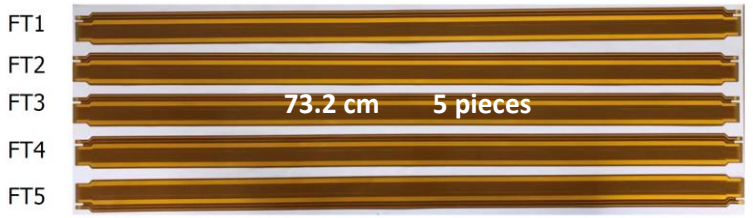






Flex cable tail prototypes for the demonstrator
13 lengths : 73.2-28.5 cm long (longest and shortest length)

- **Prototype B**
  - **5x prototypes of the longest length (73.2 cm)**
  - Production of additional lengths after electrical and geometrical test



- **Prototype C**
  - Prototype from previous design

Metrology tests: length, width, thickness

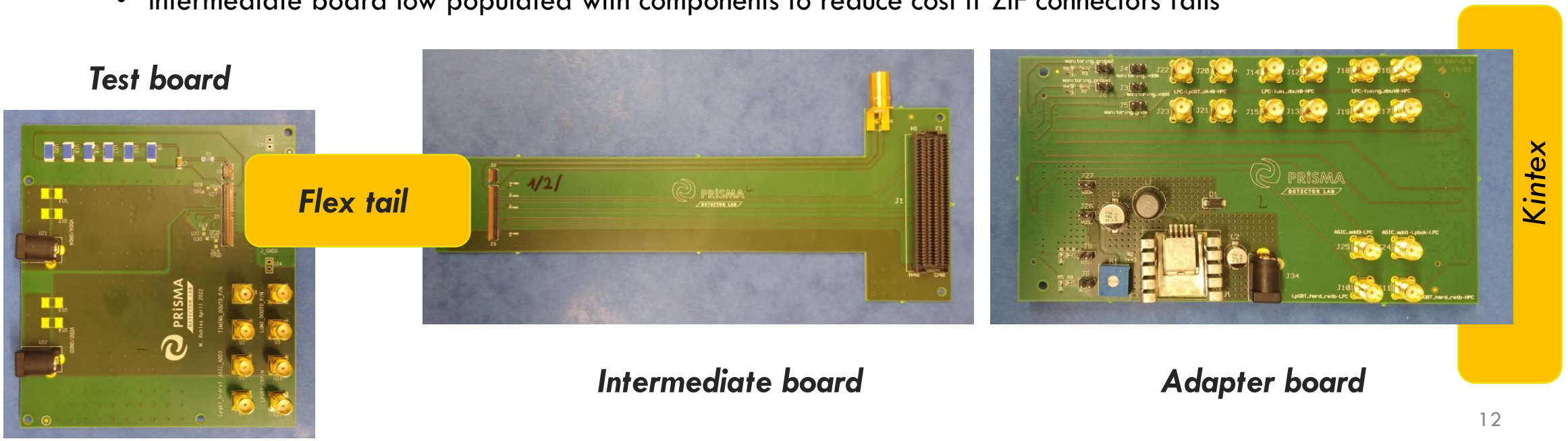
- **Length and width measurements**
  - **Length 732 ± 0.5 mm**
    - Rest of lengths: L ± 0.1 mm (given by the manufacturer)
  - **Width (caliper): 36.0 ± 0.1 mm**

- **Thickness: uniformity along the flex tail length**
  - Prototype A full production (stackup 206 µm): **[211, 221] ± 1 µm**
  - Prototype B production (stackup 186 µm): **[170,175] ± 1 µm**

Micrometer

Adapter, intermediate and test boards: electrical tests

- **Adapter boards designed for electrical tests purposes:**
  - FMC connection to FPGA (Kintex Ultrascale+ Eval. Board)
  - Selected differential pairs and single lines accessible via SMA connectors
  - Power delivery and voltage drop evaluation
  - HV delivery
  - Geometry adapted to flex tail placement within climate chamber for tests are operational temperature, -30°C
  - ZIF connector from Hirose: same as in PEB design. 10 life cycles, although testing show longer life cycles
    - Intermediate board low populated with components to reduce cost if ZIF connectors fails



Impedance control tests

- Impendance control from manufacturers (Vector Network Analyser):

	Impedance [Ω]	
Type of line	**Prototype A**	**Prototype B**
Diff. pairs	110.25*	109.07
Single lines	53.07*	51.21

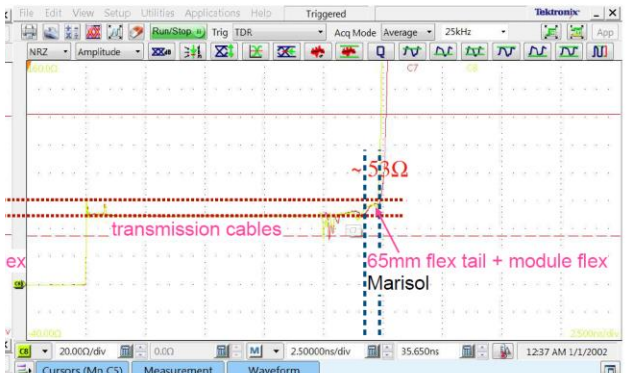
*Mean value for three prototypes: 362 mm, 400 mm and 732 mm. Measure in connection region

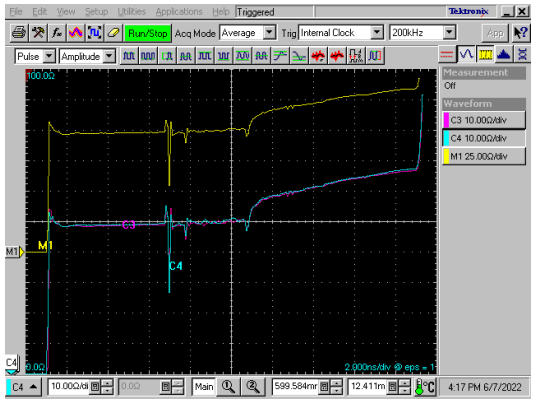
Specifications

Diff. pairs: [90, 120] Ω

Single lines: [50, 65] Ω

- Impedance control tests using **Time Domain Reflectromety (TDR) technique:**
  - Tektronix Digital Serial Analyser DSA 8200/8300 + TDR module
  - Tests on prototypes length: 73.2 cm, 28.5 cm and 6.5 mm
  - Results within specifications

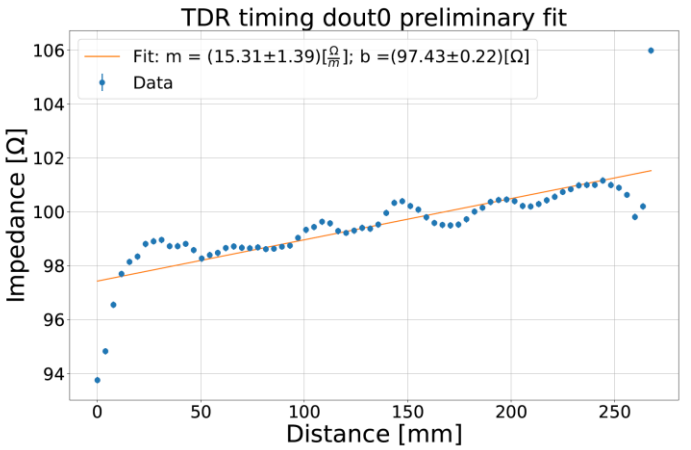




Flex Type	Quantity	Single Impedance (Specification: 50 ~ 65 Ohm)	Differential Impedance (Specification: 90 ~ 120 Ohm)
732 mm	5	55 Ohm	110 Ohm
285 mm	1	60 Ohm	120 Ohm
65 mm	2	53 Ohm	106 Ohm

Impedance control tests

- Characteristic impedance data analysis
  - Uniformity along the tracks
  - Slight increase of impedance along the lines (qualitatively expected, quantitatively to be understood)
  - Linear fit for all tracks: differential pairs and single lines

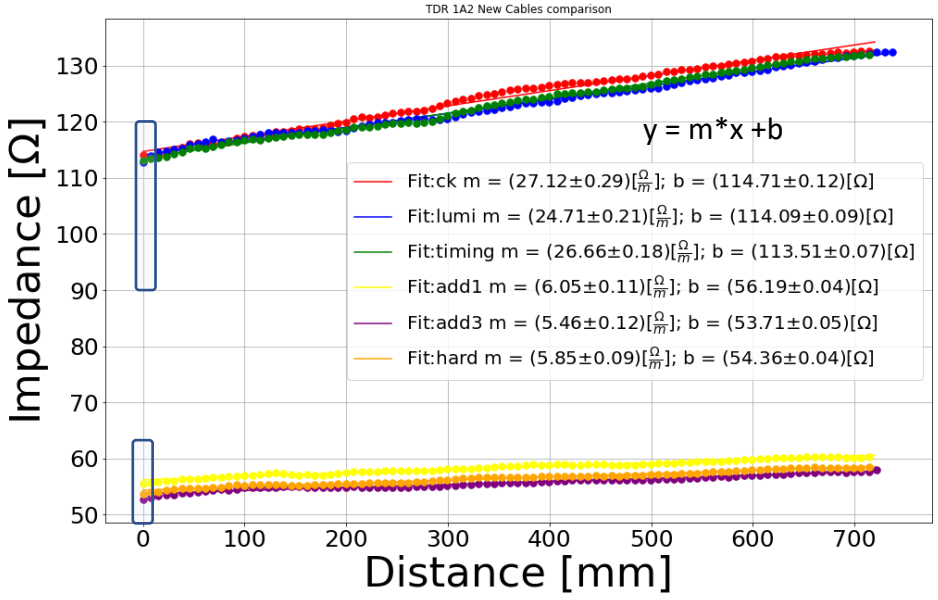


☐ Specifications

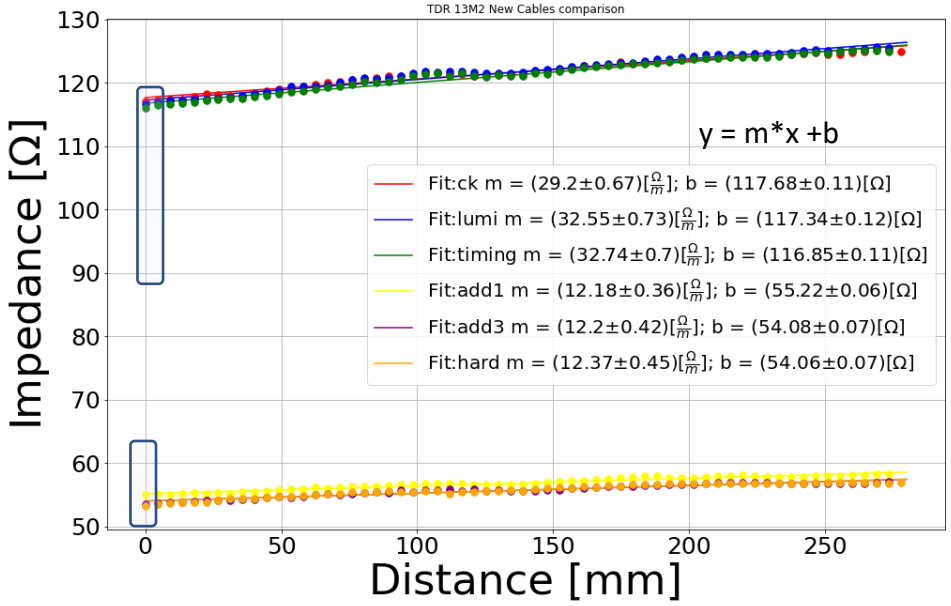
Diff. pairs: [90, 120] Ω

Single lines: [50, 65] Ω

L=73.2 cm

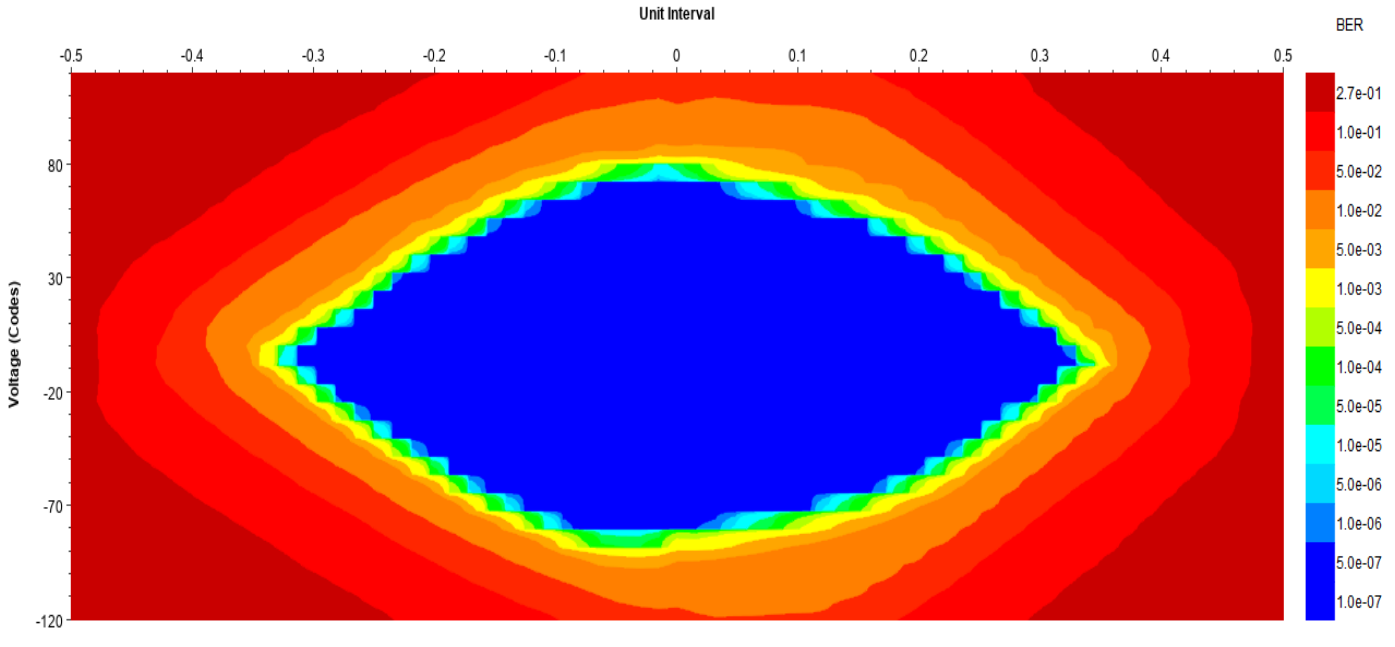


L=28.5 cm



Signal transmission tests

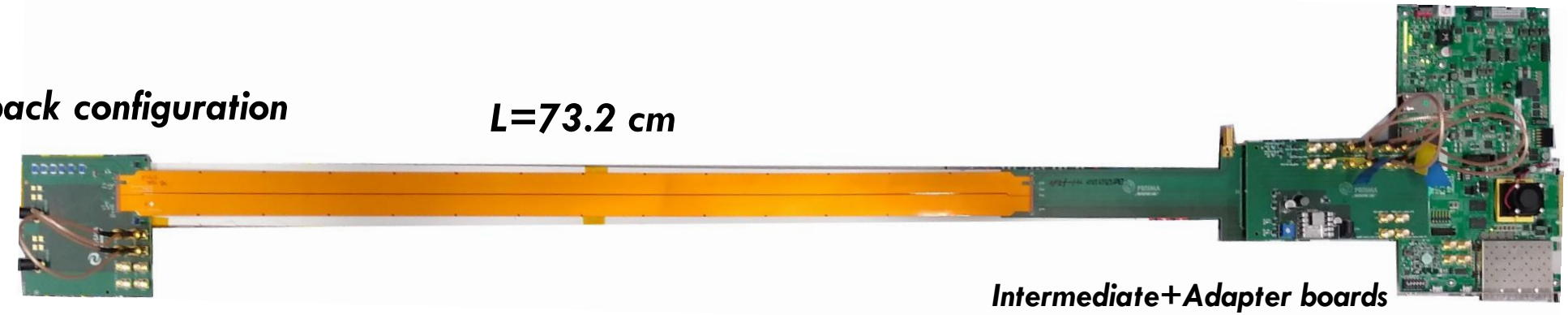
- Eye diagrams and Bit Error Rate (BER) tests at 1.25 Gb/s (Kintex Ultrascale+ Eval. Board)
  - **BER < 10^{-14}** no errors (maximum time of measurement reached**, 24 hours**)
    - **Specifications BER< 10^{-12} (~25 min)**
  - HV delivery in parallel: no errors in BER o influence on eye diagram



Kintex Ultrascale+

Loopback configuration

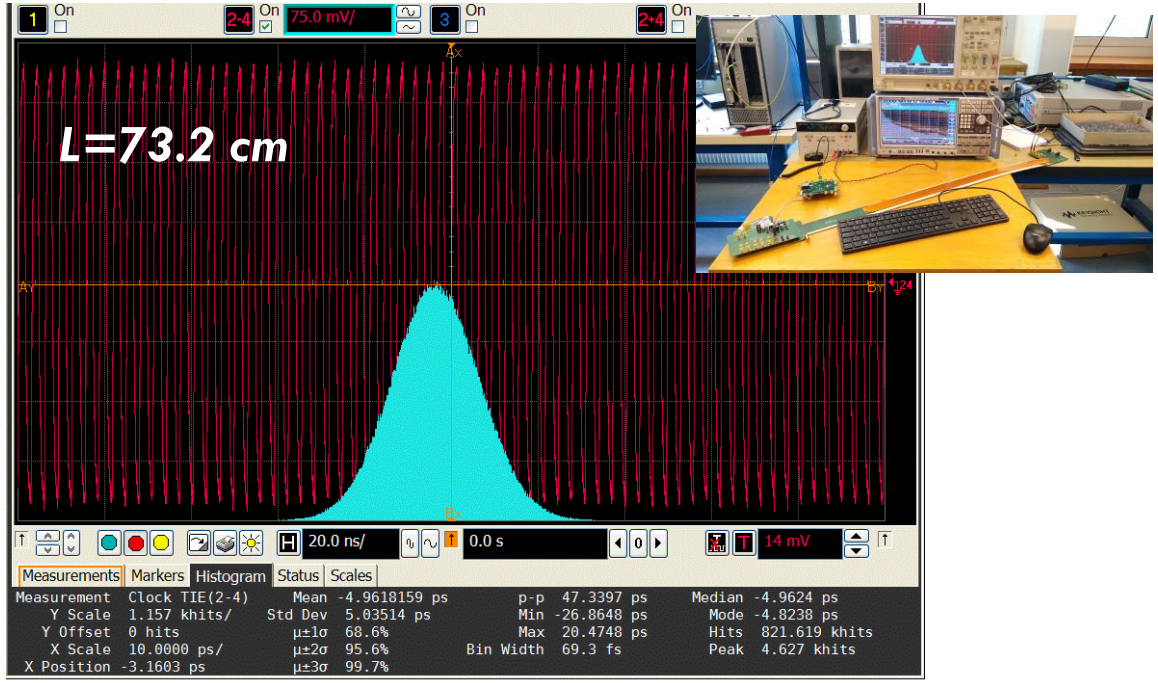
L=73.2 cm

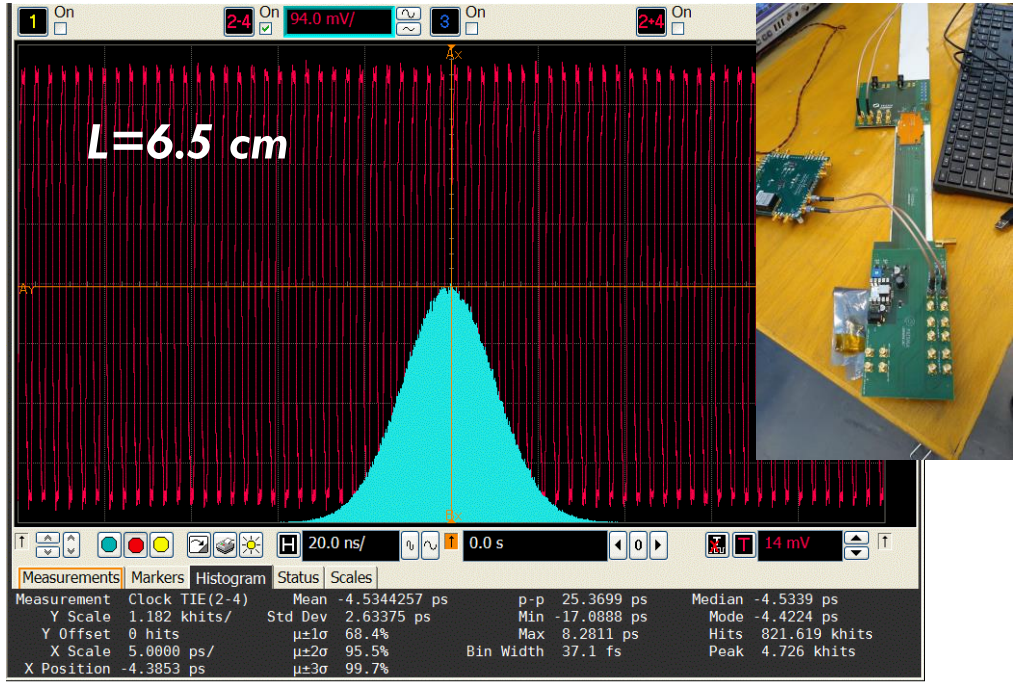


Intermediate+Adapter boards

Test board

Jitter



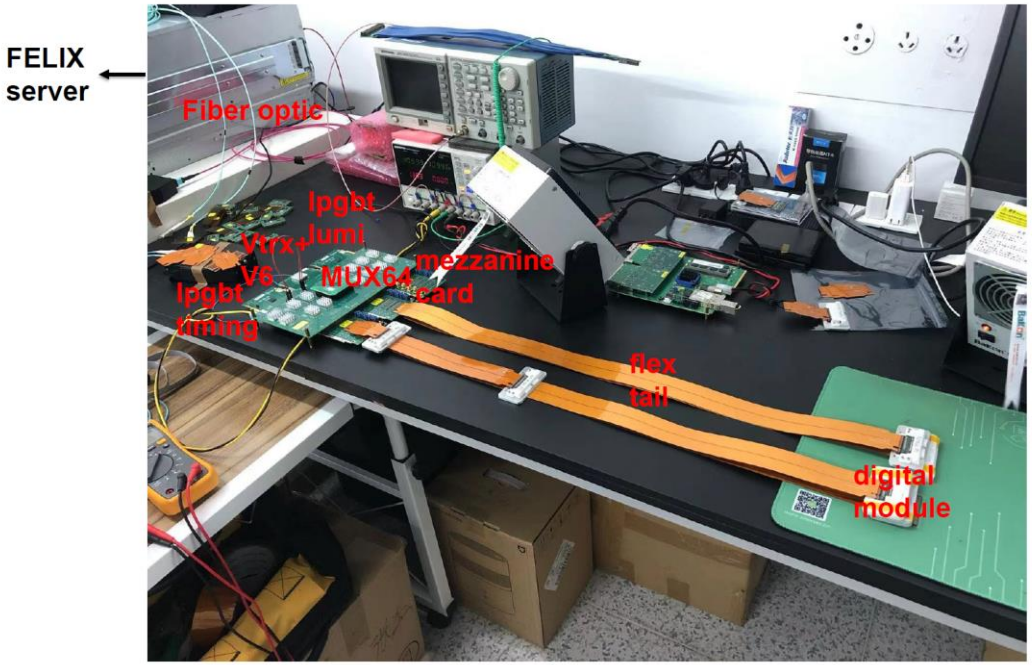


- **A set of flexes (13 lengths + 65 mm) measured at High Precision Timing Distribution* lab at CERN (Many thanks!)**
  - Jitter measured with Infiniium oscilloscope and **low jitter clock at 320 MHz.** Time Interval Error Method
    - Preliminary results including reference clock jitter:
      - **Jitter for longest (1A, 73.2cm) ~5ps and shortest length (6.5 cm) ~ 2.6ps**
    - **Jitter specifications < 5ps**

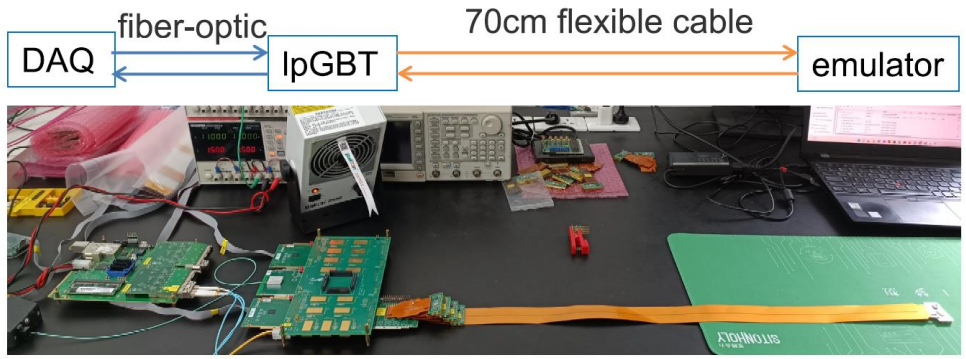
*TCLink: How much your clock phase can change between different runs?– Eduardo Brandao - 22 sept 2022, 15:30

Electrical tests at *system level*

- **Integration of the flex tail at system level**
  - Digital module: ASIC + module flex (no sensors)
  - Modular PEB (PEB prototype)
  - FELIX server
- Communication tests: **Multi I²C test for 7x digital modules + 7 flex tails**
  - Flex tail prototypes A and B stack

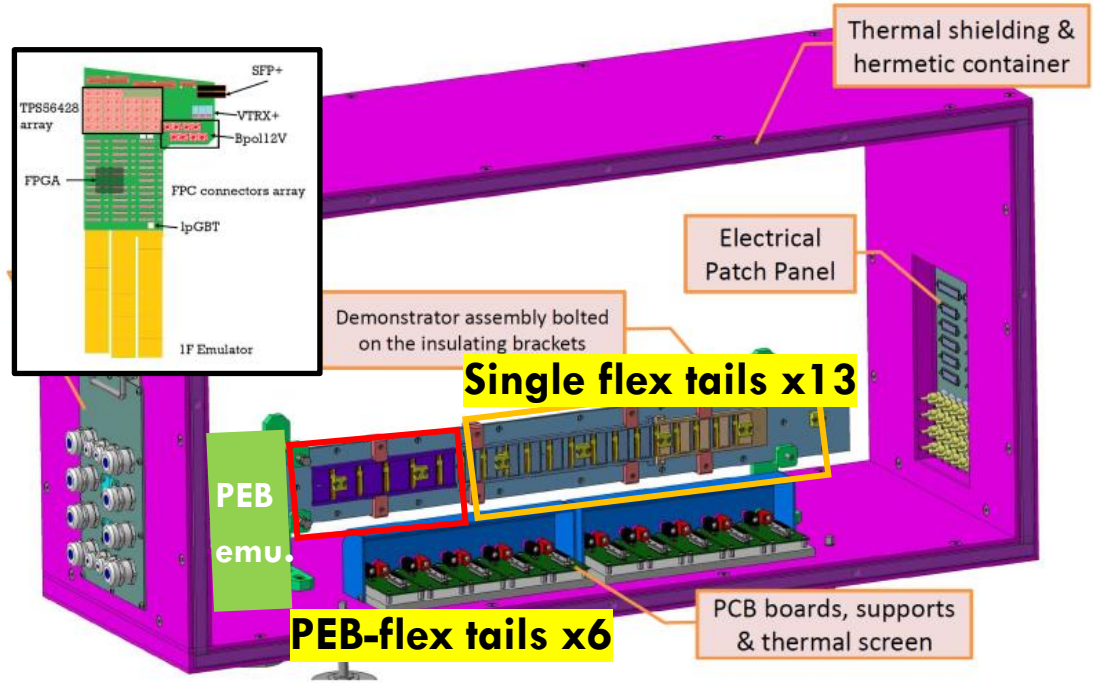


- **BERT PRBP-7** for **4x module emulators + 4x flex tails** and lpGBT at **320Mb/s and 1.28 Gb/s**
  - **BER ~ 10^{-12} no errors**



Flex tail integration in the HGTD demonstrator

- **Final step to integrate the flex tails in the demonstrator (ongoing)**
  - **Assembly:**
    - Connection to module to PEB prototype
    - **Length contribution** from different parts
    - 13 flex tails **stack**
    - Performance at **operational temperature and realistic environmental conditions**
  - **Electrical tests**
    - Communication tests between ALTIROC and PEB prototype
    - Power and HV delivery

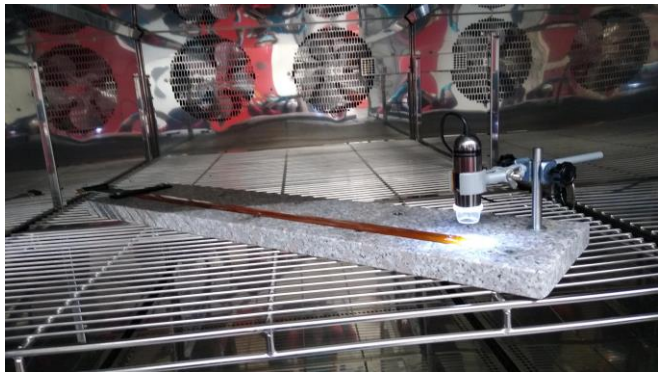


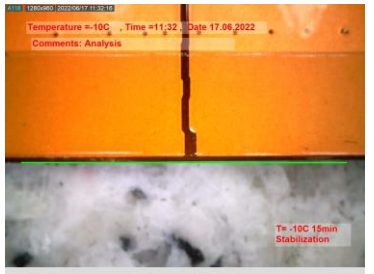
Summary

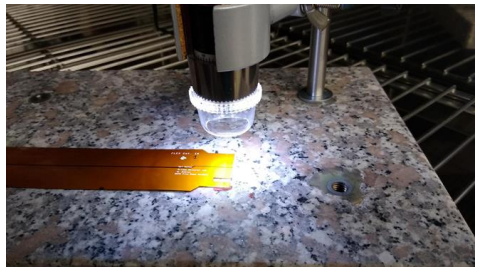
- Flex tail for the demonstrator has been designed, produced and being tested
- Electrical test results promising and within specifications for selected flex tails lengths: stand-alone and system level
  - Signal integrity crucial for proper signal transmission and communication
    - Impedance results for differential pairs [90,120] Ω and single lines [50,65] Ω within specifications and uniform along track length for different lengths and materials stackup
    - BER $< 10^{-14}$ (specifications BER$< 10^{-12}$)
    - Jitter < 5ps
- Next steps
  - Voltage drop standalone tests
  - Reproducibility of electrical tests for rest of flex tails lengths

Outlook

- Very important **mechanical challenges**
  - Operational temperature -30°C
    - Variations in length expected
      - Impact on connections to different parts
  - **Estimation of the Coefficient of Thermal Expansion (CTE)**
  - Tensile tests to estimate flex tails Young's module
  - **Mockup with 3D printed parts** to better understand **flex tail integration**

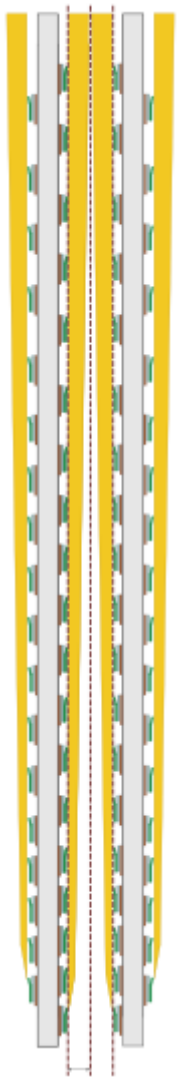


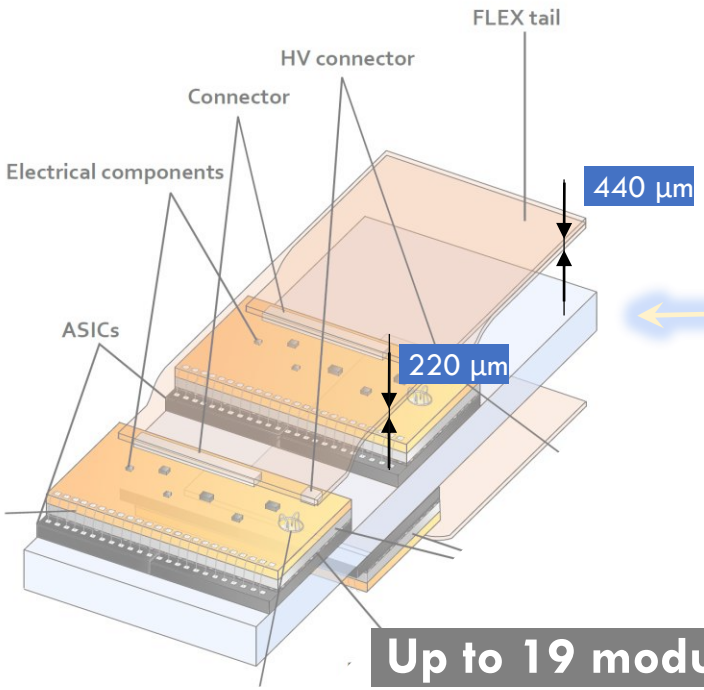


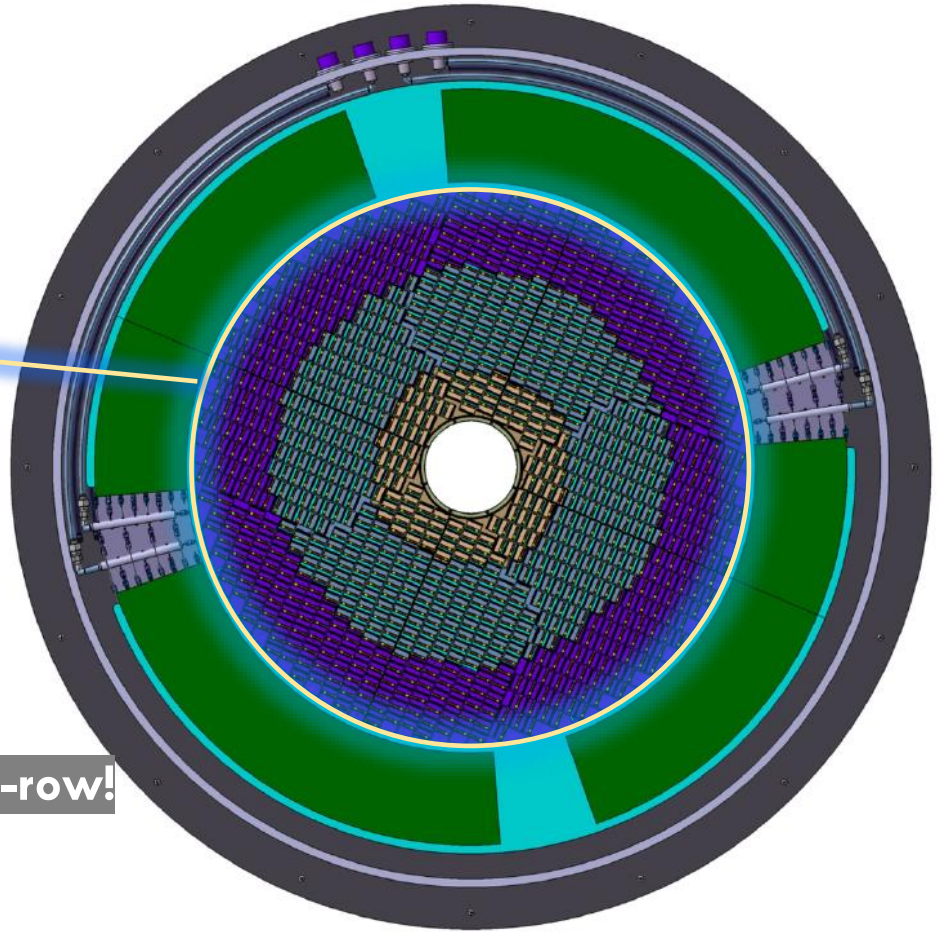


BACKUP slides

HGTD active detection region: readout-rows







Up to 19 modules + 19 flex tails per readout-row!

Different lengths of the flex tails depending on the module positioning

Distance between the innermost module and the PEB **69 cm → Long flex printed circuit!**

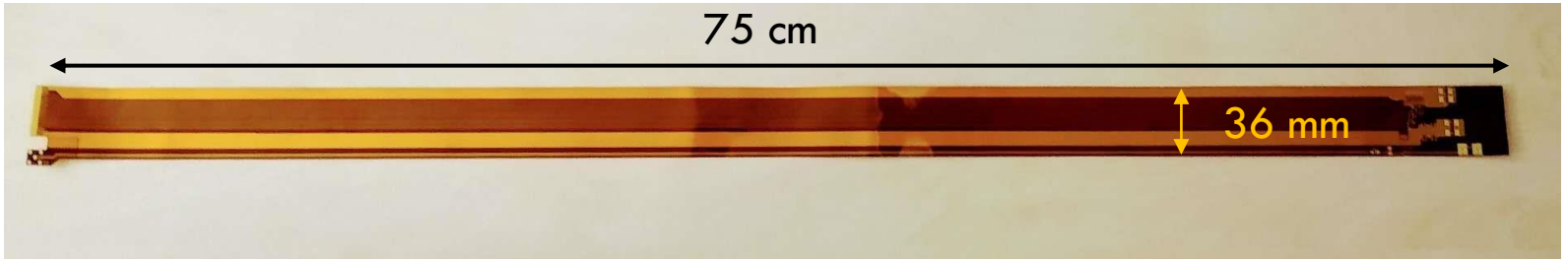
Also thickness constraints: *4.2 mm available to stack 19 flexes*! → **220 μm thick** Flex tails!

Flexible Printed Circuit: Flex tail prototype

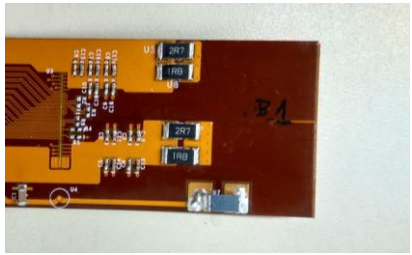
- A **75 cm x 36 mm** flex tail prototype is being tested as part of the R&D
  - The flex tail demonstrator prototype is based on this current prototype
  - **2-layers design:** differential pairs, single lines, power and ground, HV
  - Challenge for manufacturing due to the length
    - Impedance control (**100 Ω diff. pairs, 50 Ω single lines**)
    - Plane resistance requirements: **power <2.7 Ω/cm, ground (dedicated layer) < 0.7 Ω/cm**
    - HV insulation for **800 V at 3 mA** (clearance between HV line and planes)
    - **Bit Error Rate < 10^{-12}** defined by the Low powering Gigabit Transceiver in the PEB
    - Operation at -30°C:
      - Thermal contraction/expansion requirements to be defined

ZIF connection region

HV LEMO connector

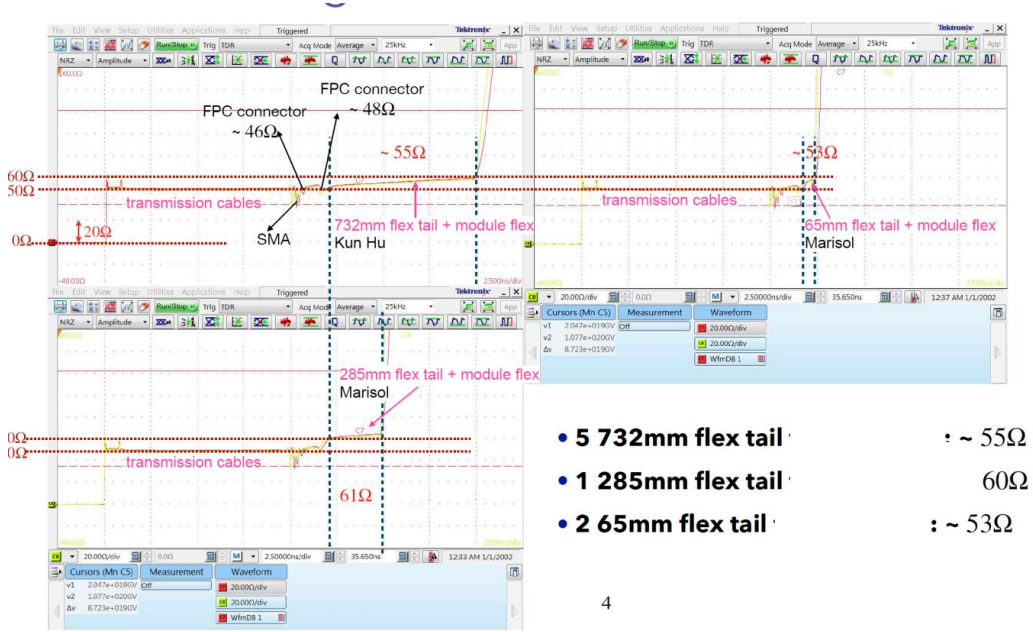


Bonding pads
LV and HV filters
Load resistors for testing

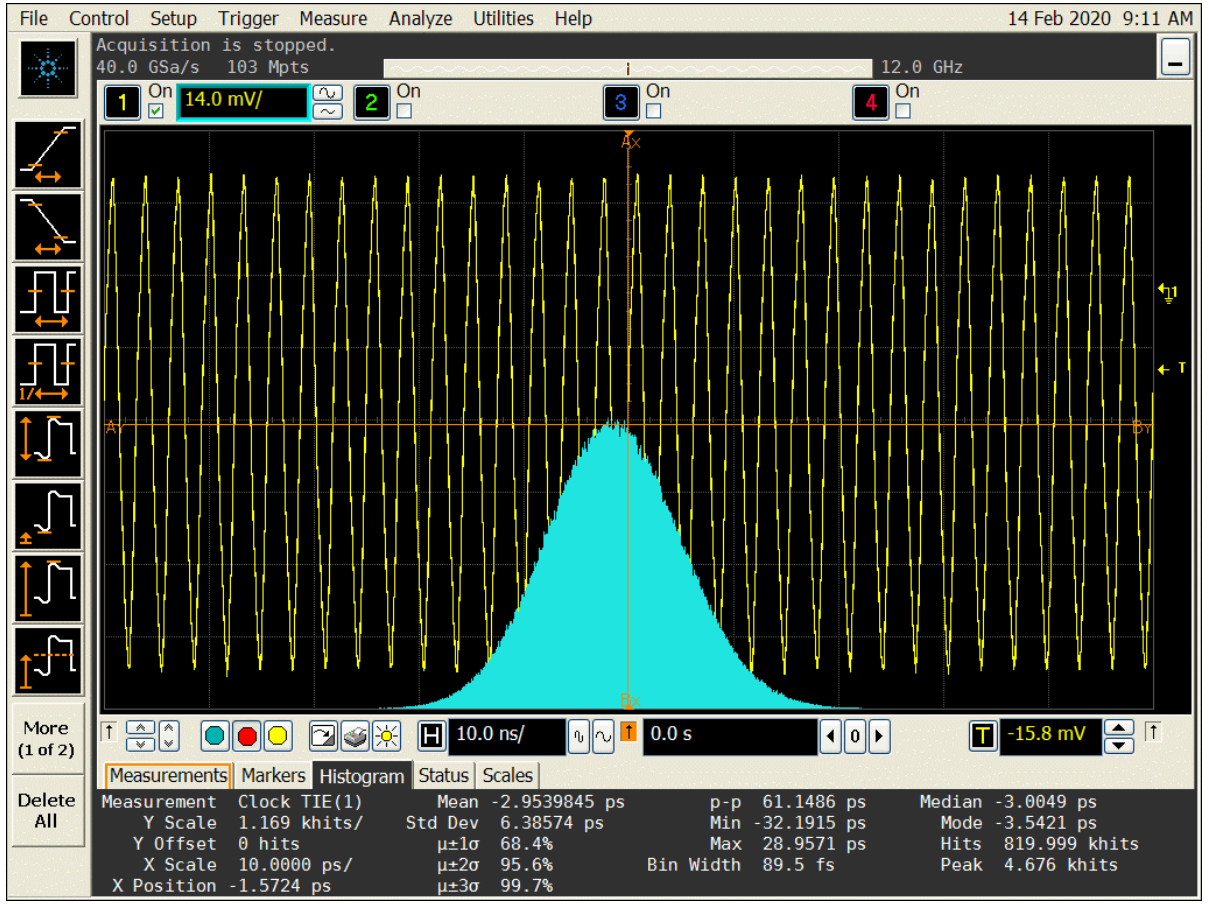


Impedance control tests

- **IHEP**
  - Tektronix Digital Serial Analyser DSA 8300 + TDR module
  - Differential pair (NC0, NC1) and single line accessible from PEB
  - TDR measurements from DSA
  - 3 lengths and two vendors (73.2 cm (Shandong), 28.5 cm and 6.5 cm (Mainz)) measured
  - Results within specifications



Oscilloscope Time Interval Error (time domain)



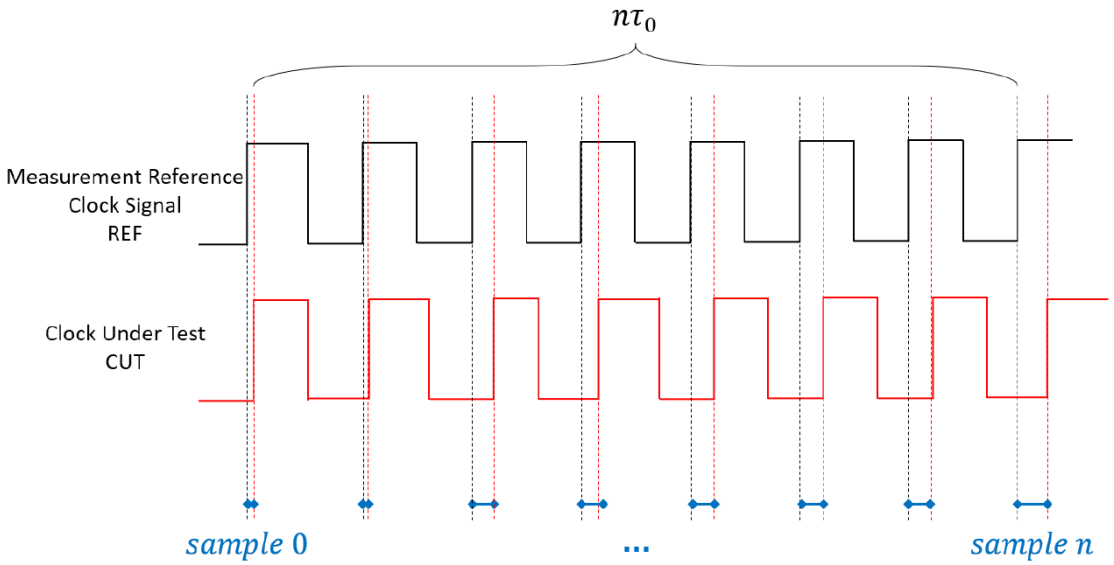


Figure 3: Time Interval Error Jitter

E. Mendes, S. Baron. EDMS Document Number **1974596**

Length of the flexes for the demonstrator

Category	Flex length [mm]
1A	732
2B	696
3C	661
4D	625
5E	590
6F	554
7G	515
8H	477
9I	438
10J	400
11K	362
12L	323
13M	285

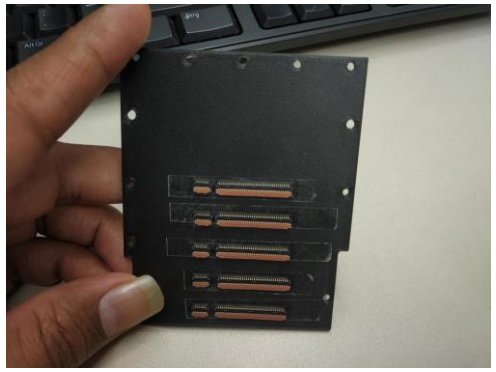
Mechanical tests: single readout-row mockup

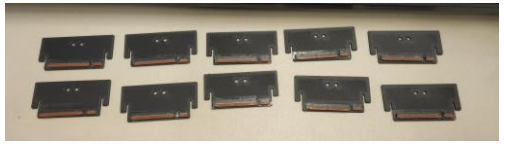
- **Mockup** at room temperature: 3D printed parts, estimation of the force on connectors

- Understand the length contribution each part (support units, flex tails bending, …)

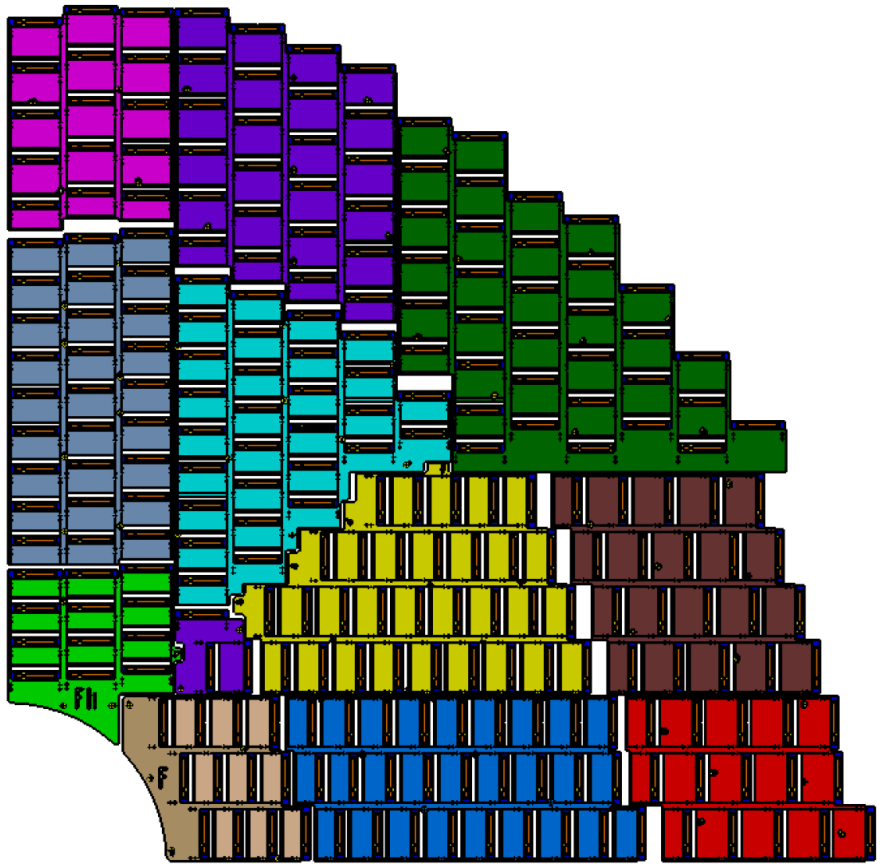
- Studies on how to fix the flex tails along the support unit to keep the thickness of the stack within specs (4.2 mm) and help to “absorb” extra length
  - First tests with tape to find optimal position before attaching holders

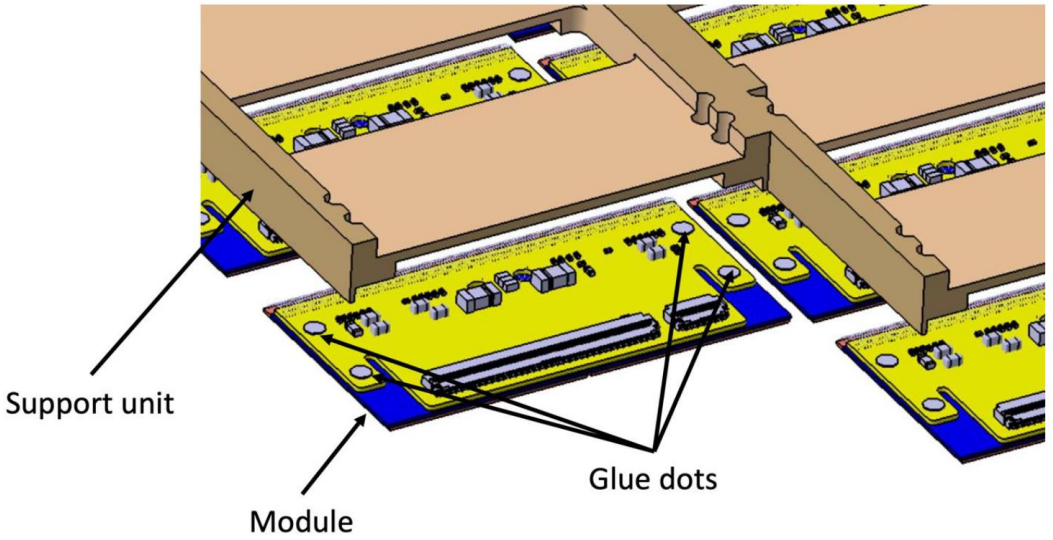
- Tests with tensile to find out flex tail Young’s module

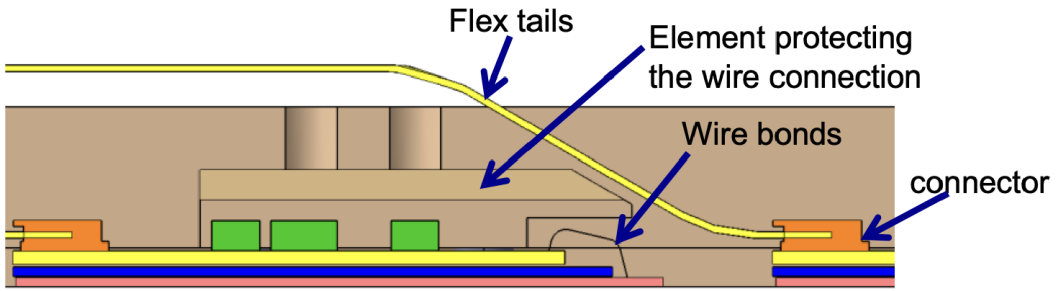




Detector units







QA/QC

Table 22. Acceptance tests and criteria for the specifications

Specification	Acceptance Test	Acceptance Criteria
11.3 Module flex and flex tail build	Visual inspection and optical measurements. Acceptance test for HV before assembly. Electrical functionality, see 11.6 Destructive test for delamination during R&D: thermal cycles with controlled moisture.	<1µA leakage current @800V HV. Dimensions within tolerance. No degradation of electrical functionality for the expected moisture conditions during detector operation.
11.6 Signal transmission on module flex and flex tail	Impedance verified with Time Domain Reflectometry. Transmission at maximum rate tested based on BER. Measure jitter TIE.	Impedance for differential pairs from 90Ω to 120Ω, for the single lines from 45Ω to 65Ω. Bit Error Rate < 10^{-11} at 1.28Gb/s. Jitter (TIE) < 5ps
11.7 Low voltage drop in module flex and flex tail	Verification via post-layout simulations and with dedicated measurements of LV drop on the module flex and flex tail.	Power plan resistance less than 2.7mΩ/cm on average (can be more in the module flex alone) and ground plane resistance less than 0.7mΩ/cm for 1.2V at 1A.
11.8 Connection of the flex tail to the PEB	Electrical contact resistance per pin: Mate applicable flex PCB, measure at the open circuit voltage 20mV maximum and short circuit 10mA maximum. Number of connection/ disconnection cycles: Insert	Maximal dimensions of the connector: 30mm width, 2mm height and 3.2mm length. Electrical contact resistance per pin of 100mΩ.

14 Reliability Matters

14.1 Quality Control to Validate Reliability Specifications during Production

The detailed production and test procedure will be described in a separate document, to be updated for PDR and FDR and finalized before the qualification of assembly and loading sites.
Here a short list of the minimal quality control steps to be performed during production to check the fulfilment of specifications is given:

8. Flex tail acceptance tests (in dedicated sites)
    a. Visual inspection for mechanical damage
    b. Metrology
    c. Tests for electrical continuity