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Design and testing of long Flexible Printed Circuits for the ATLAS High Granularity Timing Detector demonstrator

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The High Granularity Timing Detector for the ATLAS upgrade is under construction to meet the challenges of the HL-LHC. In order to connect a module, the basic detector element, to the surrounding peripheral electronic board, a flexible printed circuit (FPC) is proposed as an interconnection for data transmission and power distribution. Identical design for the FPC is required except their length, depending on the module positioning on the detector active area.The design and qualification of the FPC, manufactured in 13 different lengths (from 28.5 to 73.2 cm), are presented.

Summary (500 words)

The High Granularity Timing Detector (HGTD) for the ATLAS Phase II upgrade is being built to meet the demands of the High Luminosity LHC and provide a time measurement per end-cap track with a resolution of about 30ps.
This detector consists of two double-sided disks equipped with 8034 modules, two ASICs bump-bonded to two Low Gain Avalanche Detectors (LGAD) in turn glued to a flexible PCB, and is contained in a 75mm thick vessel.
The Peripheral Electronic Boards (PEB), PCBs dedicated for power and readout, surround the ring-shaped active area where the modules are arranged in the readout rows.
The interconnection between each module and the PEB is realized by a Flexible Printed Circuit (FPC), called flex tail.
The compact design of the HGTD requires a custom design of the flex tail, constrained geometrically by the space available between two disks and the number of modules (220µm thickness maximum) as well as the positioning of the modules and their connection on the PEB, defining the length.
As a result, the flex tail lengths range from 3cm to 69cm.
The electrical constraints are similarly challenging, including dedicated differential pairs for signal transmission for a 1.28Gb/s maximum rate, together with dedicated lines for clock distribution and control.
Moreover, planes for powering (1.2˜V at 1˜A) and grounding are required for the ASIC in addition to a High Voltage (HV) line to bias the LGAD sensors (800V at 3mA).
The impedance of the lines is required to be between 90 and 120Ω for the differential pairs and 50 to 65Ω for single lines for a proper impedance matching. Those constraints require a careful design, precise manufacturing and exhaustive testing.

As part of the R&D program of the HGTD, a demonstrator to validate the assembly and functionality of the different elements for a single readout row with 19 modules is under construction and will be tested.
A 2-layer FPC has been designed for the demonstrator in 13 lengths ranging from 28.5 to 73.2cm manufactured and tested. Custom adapter boards were designed for that purpose.

The impedance of the lines was verified via a Time Domain Reflectometer (TDR) and the Integrated Bit Error Test (IBERT) available on a Kintex Ultrascale+ evaluation board provides valuable information to assess the signal transmission.
The influence of the HV bias on the high-speed digital logic is also estimated.

The voltage drop of the power and ground planes are also evaluated and compared with post-layout simulations.
Those tests are performed at room temperature and at -30°C, the HGTD operational temperature to understand the electrical performance dependency in that temperature range.
Moreover, the temperature variation has an impact on the flex tail material which requires dedicated test to estimate their coefficient of thermal expansion as well as tests to understand the temperature influence on the mechanical integration of the flex tail during the assembly of HGTD. For that reason, a single readout row mockup for the 13 flex tails is under construction.

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