

## Development of novel low-mass module concepts based on MALTA monolithic pixel sensors – Summary

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The MALTA CMOS monolithic silicon pixel sensors have been developed in the TowerJazz 180 nm CMOS imaging process. They entail an asynchronous readout scheme, compatible with HL-LHC requirements, and have been tested to be radiation resistant to  $3 \cdot 10^{15} \text{ n}_{\text{eq}} \text{ cm}^{-2}$ .

A significant effort is now made to develop large area and light-weight modules with MALTA1 and MALTA2 sensors, reducing the material budget and using dense packaging while ensuring a scalable production to cover large detector surfaces. The MALTA sensors include 40 high-speed CMOS data transceivers with 1 ns peaking time

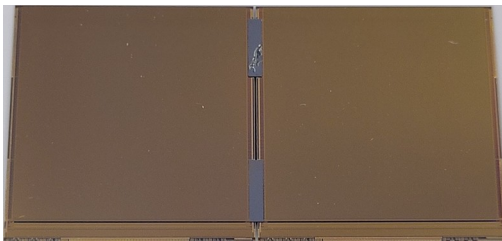


Figure 2: Silicon bridge replacing wire bonding between neighboring sensors.

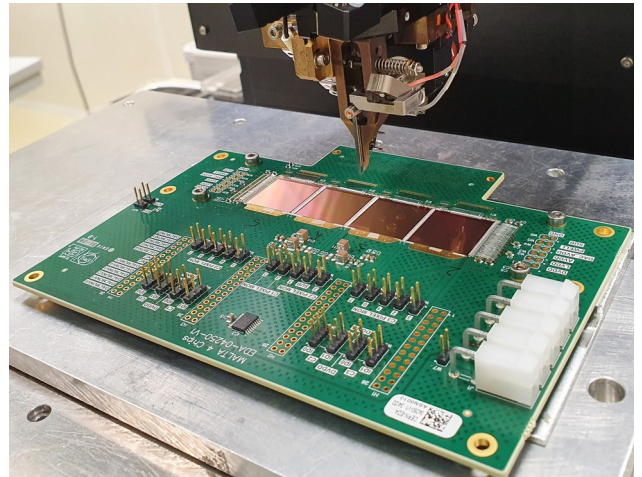


Figure 1: Picture of a 4-chip board with MALTA 1 sensors. The data transfer from chip to chip is realized using direct wire bonding between neighboring chips.

on two sides of the die for chip to chip data transfer in a master-slave configuration, allowing multiple chips to be read out by one master. We developed a 4-chip rigid PCB with MALTA 1 sensors, using Al wedge wire bonding to validate this direct transfer of data and read out the data of the entire module via one chip only. The tests conducted on this module include electrical tests, tests with sources as well as measurements in test beams. Further tests have been carried out by replacing the wire bonds with a flip-chip-connected silicon bridge. In parallel, several novel interconnection technologies such as ACF (Anisotropic Conductive Film) and nano-structured pads (nanowires) have been studied using different MALTA chip generations. These technologies are essential to overcome the minimal distance requirements of the wire bonding process and reduce the inductive load, resulting in a denser packaging and therefore a higher active area. To validate the performance of these interconnection technologies, a test structure has been designed to perform electrical tests and to study the performance of the different technologies.

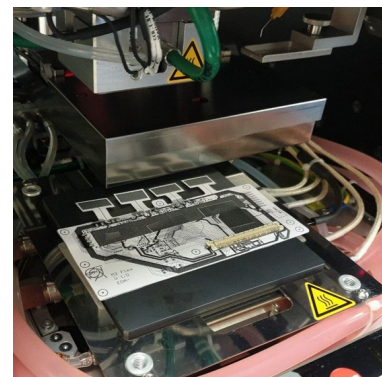
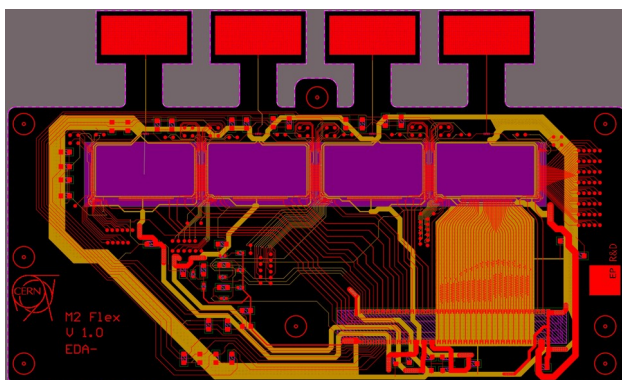


Figure 3: MALTA2 flex PCB layout (left) and mock-up in the flip-chip machine to verify the setup (right).

To further reduce material and achieve a compact multi-chip module, a flexible PCB with a thickness  $< 50 \mu\text{m}$  and track widths down to  $17 \mu\text{m}$  have been developed. The MALTA2 chips are directly flip-chip mounted on the flex circuit. The interconnection method is required to deliver a high connection yield while being able to bond a pad size of  $88 \times 88 \mu\text{m}^2$  with a minimum clearance of  $32 \mu\text{m}$ . ACF, and in a second step nanowires have been chosen as interconnection technology.

This contribution will summarise the test results of demonstrator modules as well as of the interconnection studies. An outlook for a compact silicon pixel module concept for future experiments, with a high active area, minimal material, and high potential for scalability will be presented.