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A Dedicated and Versatile System for Testing the Radiation Hardness of Various Integrated Circuits

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This work presents a versatile system that is dedicated for the testing of various integrated circuits in radiation (e.g., FPGAs, ASICs). This system allows to power the device under test (DUT), and to monitor and read out in real time various parameters: power consumption (100 μ V and 100 μ A resolution), and various operational parameters. The system has built-in features to detect and test for SELs, SEUs and to monitor the DUT for TID and annealing phenomena. A graphical user interface allows the user to connect to the test bench through TCP/IP from a safe zone, and to record measurements data.

Summary (500 words)

This talk is dedicated to the introduction of a test bench and system that is designed for the testing of certain integrated circuits in special condition of strong radiation environment and in other special environments. We will focus on radiation-hardness testing of integrated circuits, single event effect counting and cumulative radiation effect measurement and parametrization. Examples of ASICs, commercial FPGAs and radiation-hard integrated circuits are considered.

We present a versatile system that was patented and designed for the testing various integrated circuits in radiation. The system was optimized during more than 5 years of testing campaigns for various integrated circuits in particles and ion beams. We have gathered information about the requirements of a such system and how to design it to accommodate a broad range of circuits. This system allows for high-speed readouts, and can perform multiple operations on signals and data stream. It is made of 3 main components: a master FPGA-based board, a power delivery mezzanine card and a slave FPGA-based board. The master FPGA board controls the whole system and performs all the functionality tests to the device under test (DUT). It is connected via an TCP/IP connection to a PC and embeds SFP optical link capable to read out the DUT over multiple optical fiber connectors by using the slave FPGA board as a communication interface. The power delivery mezzanine is able to provide up to 8 power rails within a voltage range between 0.8 –5 V and can deliver a maximum current up to 8 A. Each power rail is monitored with a fast-sampling rate up to 1 kHz, and with a very good resolution of less than 100 μ V and 100 μ A over the full range. The power is provided to the DUT over long distance cables, 5 to 10 meters long, and any voltage drop that may occur on the cable is compensated using a special feature of a hardware differential remote feedback block.

The master FPGA board and the power delivery mezzanine card are closely inter-connected and are placed in the experimental area at a safe distance from the irradiation area. The slave FPGA board is connected to the DUT test board and is localized in the irradiation area, near the beam exit window. The entire system is built in a way to protect the system itself against any radiation-induced failures. Several built-in features were implemented in the system like: SEL detection and counting, and SEU counting and classification and precise TID effects and annealing measurements, all for time intervals from few microseconds to several weeks. A graphical user interface (GUI) allows the user to monitor in real time and control the system and the DUT. The test data are saved in files for later analysis.

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