Radiation studies performed on the High Luminosity ATLAS TileCal link Daughterboard

The **ATLAS** Hadronic **Tile Calorimeter (TileCal).**

TileCal is a sampling calorimeter that identifies and measures hadronic jets, and transverse missing energy. It is divided in four cylindrical barrels composed of 64 wedge-shaped modules where plastic scintillator tiles are used as active material interleaved with steel plates used as absorbers. Light from two sides of a pseudo-projective cell composed by a group of scintillators is collected by wavelength shifting fibers and read out by two photomultiplier tubes (PMTs). To face the higher radiation levels and increased rates of pileup of the High Luminosity Large Hadron Collider (HL-LHC), the TileCal electronics will be upgraded with a new design that will provide continuous digital read-out of all TileCal with better timing, better energy resolution.

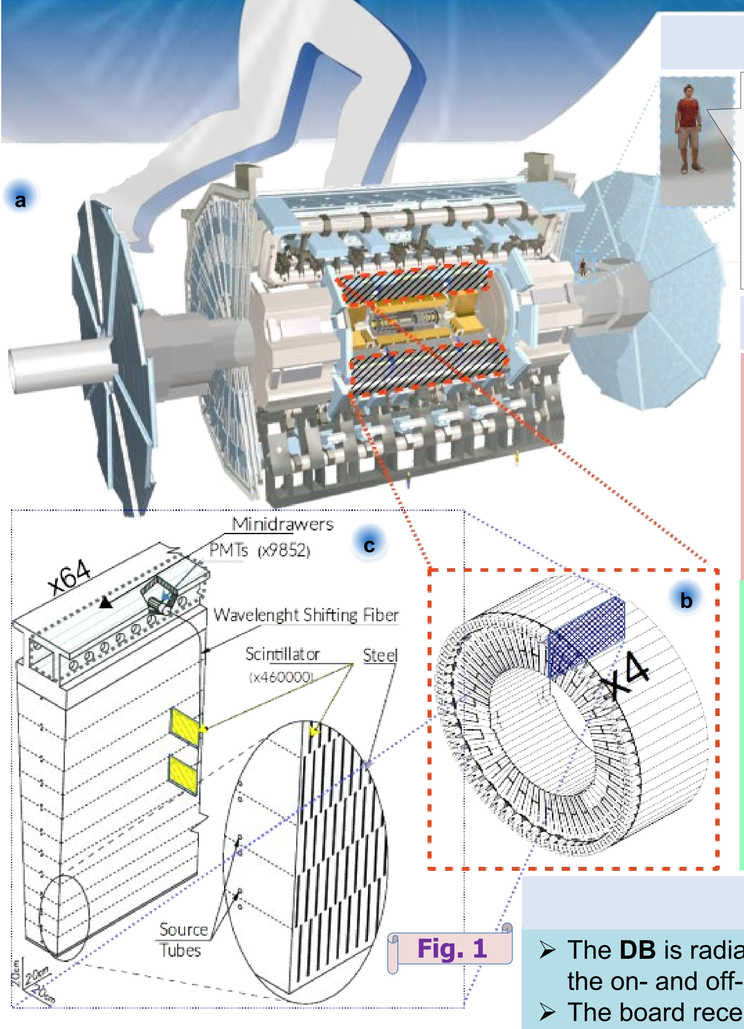


Fig. 1

Tilecal read-out system for the **HL-LHC** .

The **off-detector electronics** (Fig. 2) will provide digitized signals at 40 MHz to the **Level 0 (L0)** trigger system through the **Trigger and DAQ interface (TDAQi),** and the **FELIX** system will read-out data stored in pipelines in **Tile Preprocessors (TilePPr)** at 1 MHz. The **TilePPrs** will interface the on- and off-detector electronics through multi-GBps optical links

The power will be monitored and distributed to the on-detector electronics by:

- **Detector Control System (DCS)** to interface with the **Low Voltage Power Supply (LVPS)**
- **High Voltage Power Supply (HVPS)** to provide high voltage to each **PMT**

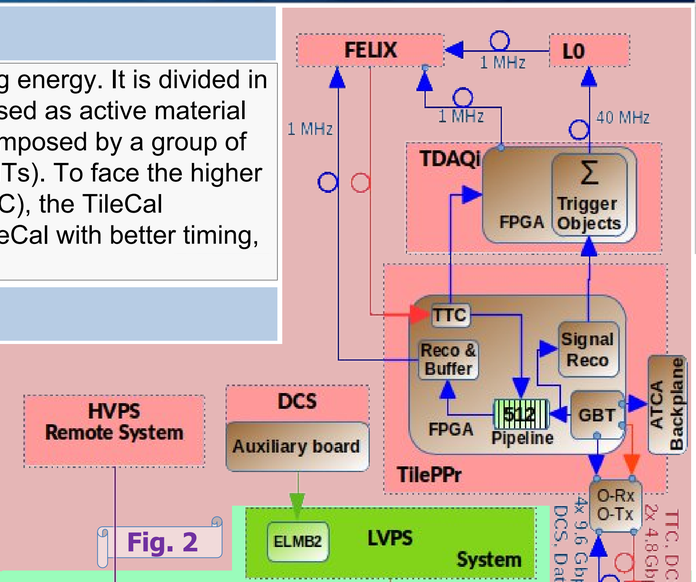


Fig. 2

The on-detector is comprised by **896 Minidrawers (MDs, Fig. 3),** in which data from all TileCal PMTs will continuously be sampled at **40 MHz** (Fig. 3). Each **MD** will host up to **12 channels** by means of:

- **12 PMTs** to turn light pulses to electric signals.
- **12 Front-End Boards (FEBs)** to shape and condition the PMT signals,
- **a Mainboard (MB)** to continuously sample and digitize **two gains** of shaped PMT signals,
- **a Daughterboard (DB, Fig. 4)** to distribute **LHC synchronized timing**, configuration and control to the front-end, and **continuous read-out** of the digital data from all the MB channels to the off-detector systems via multi-Gbps optical links,

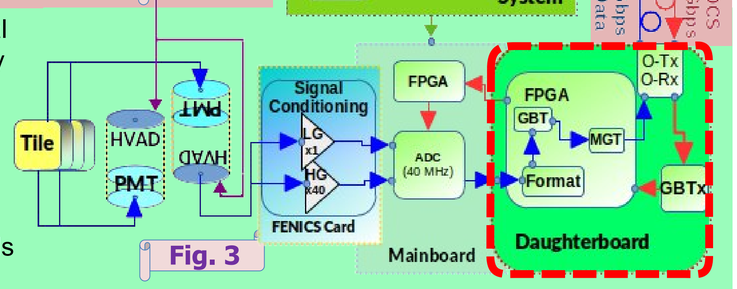


Fig. 3

The **Daughterboard revision 6.**

- The **DB** is radiation tolerant board with a redundancy layer of two functionally-equivalent halves that interconnects the on- and off-detector by means of a **400-pin FMC** connector and **four SFP+** respectively.
- The board receives commands and clocks from the off-detector by means of **CERN rad-hard GBTx ASICs** through **4.8 Gbps GBT-FEC downlinks**.
- Two 20 nm planar featured **Xilinx Kintex Ultrascale (KU) FPGAs** distribute clocks and configuration received from the GBTx to the MB, while reading slow integrator data and fast digitized data from two different gains of the PMT channels.
- The xADCs of the KU FPGAs sample temperature, voltage stability, currents. A over-current protection circuit triggers a power cycle in the case of the presence of high currents.
- Each KU FPGA sends data off- detector by means of two copies of GBT-FEC protected words through two 9.6 Gbps uplinks.
- The board radiation tolerance is achieved by the **redundancy layers** in the design, using the **Xilinx Soft Error Management (SEM), Triple Mode Redundancy (TMR)**, **GBT-FEC** protocol, and **GBTx** ASICs.

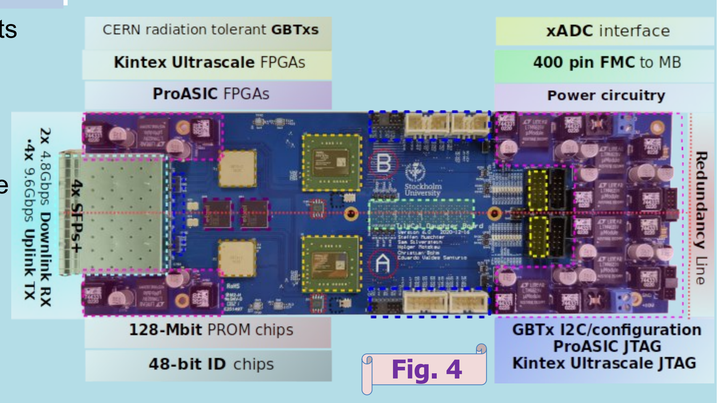
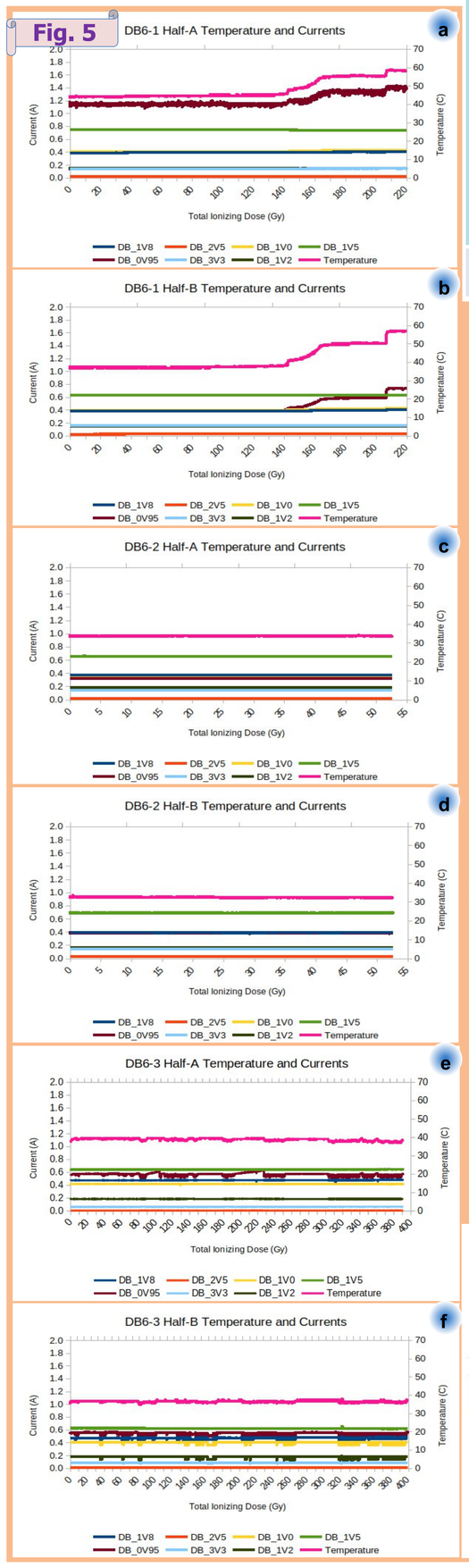


Fig. 4



Radiation tests.

Two separate tests were performed for **Total Ionizing Dose (TID).** The KU FPGAs and all the currents were monitored for each of the voltages of each half of the two boards (Fig. 5) Special interest was put in the total of ten Coretek SFP+, the six KU FPGAs, the six Microsemi ProaSIC3 FPGAs and the reconfiguration FLASH memories. None of the components were damaged by the deposited TID:

- **DB6-1** was irradiated with Gamma radiation at Co^{60} at the CERN CC60 facilities to 220 Gy at a rate of 3.37 Gy/h (Fig 5. a, Fig 5. b). The increase in the current measured in the 0.95 V of both sides at around 140 Gy was proven to be correlated with the failure of the active components of the fan used to keep the KU FPGAs cool leading to the increase of temperature on the FPGA.
- **DB6-2** was irradiated with Gamma radiation at Co^{60} at the CERN CC60 facilities to 54 Gy at a rate of 0.33 Gy/h (Fig. 5 c, Fig 5. d). Currents and the temperatures were stable during the full run.
- **DB6-3** was irradiated in the AIC-144 cyclotron proton beam line with 54 MeV protons at the IFJ in Krakow to 381 Gy for half-A FPGA and 400 Gy for half-B FPGA at a rate of 2.88 Gy/h (Fig. 5 c, Fig 5. d). All the currents and the temperatures were stable during the full run. The higher fluctuations compared with DB6-1 (0 to 140 Gy) and DB6-2 are due to active Single Event Upset (SEU) corrections by the Xilinx SEM and resets applied when an uncorrectable SEU appeared during the run.

Two separate tests were performed for **Single Event Latchups (SEL)**, one as described for the **DB6-3** with 54 MeV protons, where the FPGAs were irradiated to a fluence of 2.62E+11 p/cm2. In the second test, two Trenz TE0841 boards (each with the same KU FPGA used in the DB design), a Lattice ICE40LP FPGA and a ProASIC3E A3P31500 FPGA were irradiated with 226 MeV protons to a fluence of 1.11E+12 p/cm2, for which all the currents of the FPGAs were monitored (Fig. 6).

- No **SEL** were observed in the units under test. The fluctuations of the currents in the TrenzTE081_3v3 curve is due to LCMXO2 CPLDs malfunctioning after 5.4 kRad of TID.
- In all the tests, the ProASIC3 FPGAs firmware functionality was recovered from TID effects on the configuration memory after annealing. The VPUMP of the devices was damaged so reconfiguration not possible (in agreement with reports from Actel). Similarly the PROM devices also could not be re-configured after ~200Gy of TID, however the memory contents were not damaged in any of the devices.

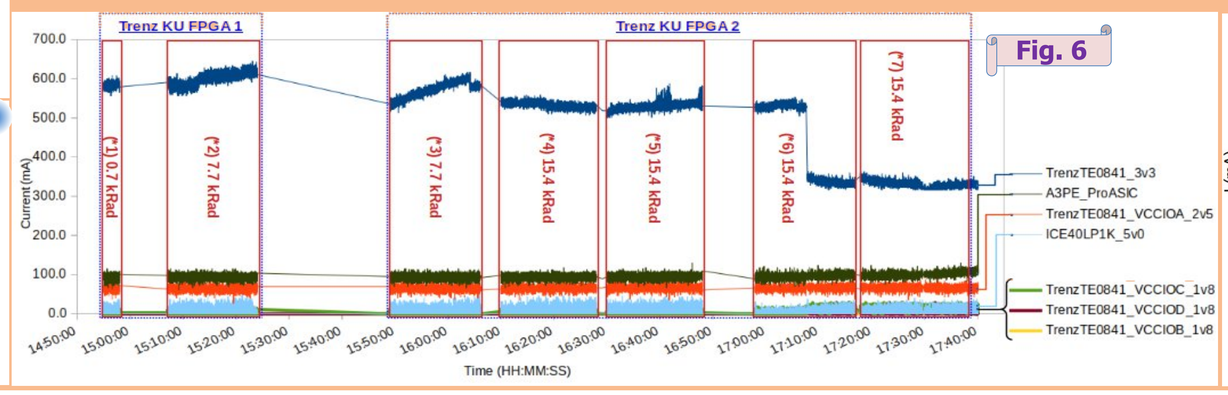
A set of tests was setup to cover the **Non-Ionizing Energy Losses (NIEL)** tolerance, where a DB (**DB6-0**) and a set of test boards with non-radiation qualified DB components were irradiated to a fluence of 14E+12 (1 MeV equivalent n)/cm2.

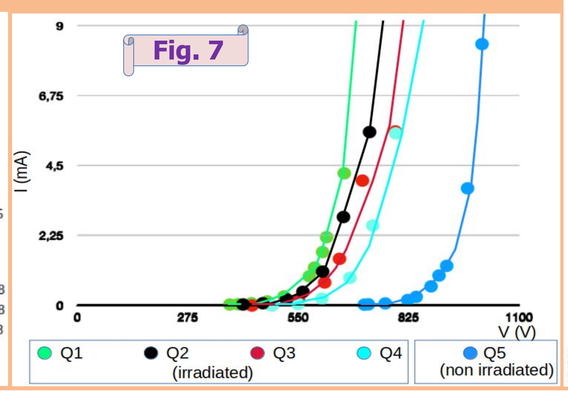
The post-radiation tests performed on **DB6-0** demonstrated the radiation tolerance of the KU FPGAs up to the exposed fluence. In the case of the ProASIC, some after effects could be seen where the firmware functionality was recovered after annealing and in some cases re-configuration capability was recovered as well. The same applies to the PROMs where after annealing some of the devices recovered the re-programing capabilities, with all the contents of the memory not being affected in any of the devices.

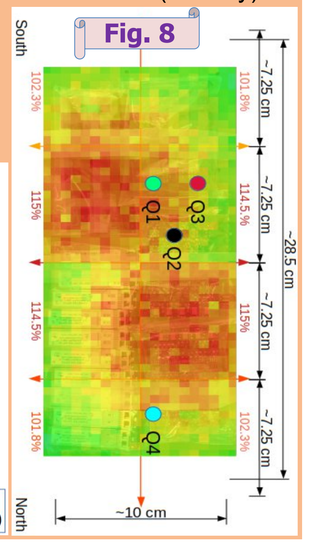
- Four different variants of 10 Gbps multi-mode SFP+ devices were tested: AVAGO, CORETEK, FS-Europe and Direktronik, where only the AVAGO devices failed to pass the test. To further test the rest of the variants, extra tests are being performed with 10 devices of each brand to account for batch variability.
- It was seen that the threshold voltages for the MOSFETs used in the design shifted with the exposure (Fig. 7) due to the Gamma component present in the reactor (195 Gy)

The asymmetrical profile of the flux in the cavity (Fig. 8) was used to probe the shifts of the thresholds in the MOSFETs.

- Out of fifteen QUAD oscillators irradiated, four failed to pass the post irradiation tests, therefore the device needs to be removed from the design.
- The rest of the components (Schottky diodes, oscillators, operational amplifiers) passed the post radiation tests with no issues.







Conclusions.

The DB6 design radiation test campaign qualify all the parts and components to fulfill the HL-LHC requirements. Exhaustive radiation tests have proved that the design is TID and SEL-resistant. The extra protection added to the design for SEL appearances in the form of a over-current circuit has to be removed due to the shift in the threshold of the MOSFETS used in the implementation. Similarly, the QUAD oscillators used to de-couple the phase of the DC-DC converters has to be removed from the design, and extra studies has to be performed to assess the impact of this design modification on the board noise. Future plans include producing extra prototypes that include the aforementioned modifications, performing Single Event Upset tests, and following-up in the tests to finalize the selection of the SFP+. Around 930 DB6 will be produced as the contribution of Stockholm University to the HL-LHC era for TileCal.

Eduardo Valdes Santurio, on behalf of the Tile Calorimeter System. (TWEPP 2022)
Phd Student at Fysikum, Stockholm University. Email: **eduardo.valdes@fysik.su.se**, **eduardo.valdes@cern.ch**
Co-authors: Samuel Silverstein, Christian Bohm, Suhyun Lee, Katherine Dunne, Holger Motzkau, Christophe Clement.