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Radiation studies performed on the High Luminosity ATLAS TileCal link Daughterboard

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The new electronics of the ATLAS TileCal for the HL-LHC interfaces the on-detector and off-detector electronics by means of a Daughterboard. The Daughterboard is positioned on-detector featuring commercial SFPs+, CERN GBTx ASICs, ProASIC FPGAs and Kintex Ultrascale FPGAs. The design minimizes single points of failure and and mitigates and radiation damage by means of a double-redundant scheme, Triple Mode Redundancy, Xilinx Soft Error Mitigation IP, CRC/FEC for link data transfer, and SEL protection circuitries. We present an updated summary of the TID, NIEL and SEE qualification tests, and performance studies of the Daughterboard revision 6 design.

Summary (500 words)

The upgrade programme for the ATLAS Hadronic Calorimeter (TileCal) for the HL-LHC has motivated progressive redesigns of a radiation tolerant link Daughterboard (DB). The DB interfaces the on-detector with the off-detector electronics via two 4.6 Gbps downlinks and two pairs of 9.6 Gbps uplinks driven by four COTS SFP+ Optic transceivers. LHC synchronous timing and configuration and are received and propagated to the front-end via two Microsemi ProASIC FPGAs, two CERN rad-hard GBTx ASICs and two Kintex Ultrascale FPGAs. Simultaneously, the Kintex FPGAs transmits continuous high-speed readout of digitized PMT samples, detector control system and monitoring data through the uplinks. The design mitigates radiation damage and minimizes single points of failure by means of a set of techniques such as: a double-redundant scheme for redundant read-out of a same TileCal cell, Triple Mode Redundancy (TMR), Xilinx Soft Error Mitigation (SEM) in the FPGAs to mitigate Single Event Upset (SEU) rates, Cyclic Redundancy Check (CRC) and Forward Error Correction (FEC) in the link data transfer, and dedicated over-current protection circuits to cover any unexpected Single Event Latchup (SEL).

Around 930 Daughterboards will be produced as the contribution of Stockholm University to the the ATLAS Upgrade for the HL-LHC era. Radiation test campaigns have taken place to qualify the different components of the DB for Total Ionizing Dose (TID), Non Ionizing Energy Losses (NIEL) and Single Event Effects (SEE). The Kintex Ultrascale FPGAs, the ProASIC FPGAs, the configuration FLASH memories and a range of commercial SFPs+ available were tested for TID, SEE and NIEL. TID tests included two DB exposed to different dose rates of gamma radiation where currents and temperatures were monitored during the whole radiation time. NIEL tests were performed with neutrons over a DB with two configuration FLASH memories, two Kintex Ultrascale and two ProASIC FPGAs, and AVAGO and Coretek SFPs+. SEU rates were estimated during the SEL tests in a 224 MeV proton scanning beam and re-verified in a dedicated test performed in a 54 MeV proton circular beam, in both tests all the voltages, currents and temperatures were monitored during the radiation period.

We present a summary of the studies that took place to verify the reliability and resiliance of the Daughterboard revision 6 design after the radiation qualification test campaigns. The summary includes a design status and discussion about the future design changes to cover the results of the studies performed.

Primary authors: VALDES SANTURIO, Eduardo (Stockholm University); FALTOVA, Jana (Charles University (CZ)); VALDES SANTURIO, Eduardo (Stockholm University (SE))

Presenter: VALDES SANTURIO, Eduardo (Stockholm University (SE))

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