Digital cells radiation hardness study of TPSCo 65nm CIS technology by designing a Ring Oscillator

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Introduction

The CPPM group has long been designing and testing HV-CMOS blocks to complete monolithic chips in various technologies (TJ180, LF150, AMS) in the framework of several collaborations. In 2020, we participated in the MLR1 run in TowerJazz 65 nm technology through CERN's EP-R&D WP1.2, by designing a ring oscillator test chip. Its aim is to characterize the standard cells of this technology and evaluate their radiation hardness against TID as well as their behavior at different temperatures.

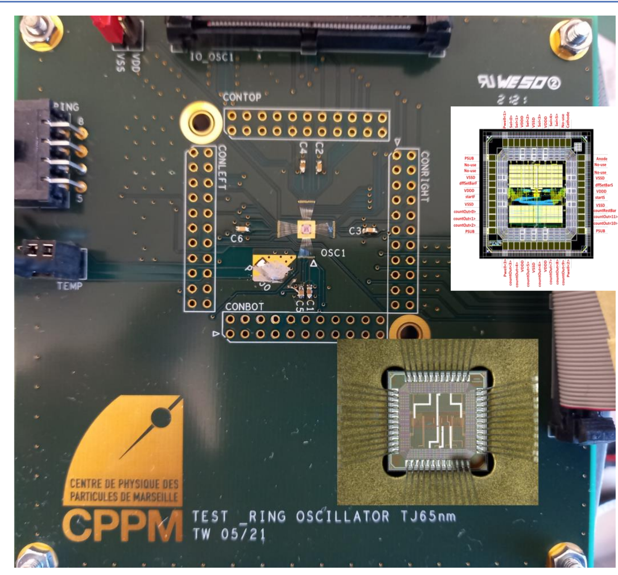

Fig1. DUT board, layout, pinout and bonding of the chip.

Description

24 ring oscillators were designed and duplicated to form two banks: the **Functional** (F) bank which is made to oscillate during irradiation and the **Static** (S) bank, under bias in a static state while the chip is being irradiated. Each ring oscillator is composed of a chain of 101 cells, to count a realistic frequency, interrupted by an AND gate, that commands the start/stop of the cell. They differ from each other by the type of cells they are made of, with variations of length, threshold and input locations.

Low V_T		Super Low V_T	
Size Min	Size+	Size Min	Size+
INV0_LVT	INV4_LVT	INV4_SLVT	INV8_SLVT
NOR1_LVT_A	NOR4_LVT_A	NOR4_SLVT_A	NOR8_SLVT_A
NOR1_LVT_B	NOR4_LVT_B	NOR4_SLVT_B	NOR8_SLVT_B
NAND0_LVT_A	NAND4_LVT_A	NAND4_SLVT_A	NAND4_SLVT_A
NAND0_LVT_B	NAND4_LVT_B	NAND4_SLVT_B	NAND4_SLVT_B
DFF1_LVT	DFF4_LVT	DFF1_SLVT	DFF4_SLVT

Table1. the 24 ring oscillators

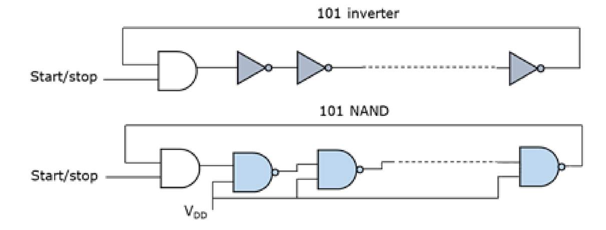

Fig2. Two ring oscillators (inverter, NAND1)

Measurement set-up

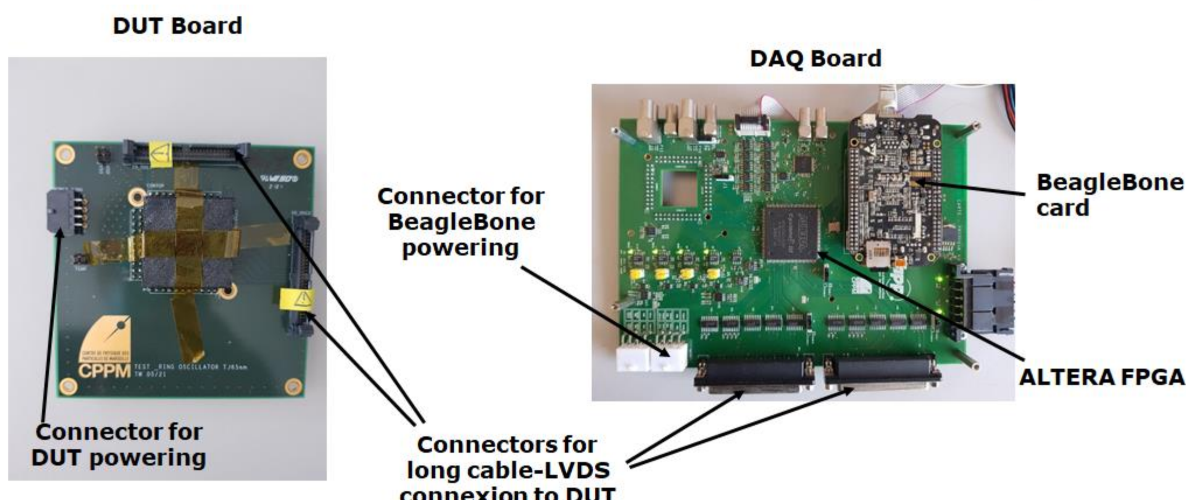

Fig3. The DUT and DAQ boards used for the characterization of the chip

The test chip is bonded on a DUT board connected to a Beaglebone DAQ system (Linux Os embedded).
For the communication, each sequence is described in VHDL inside a FPGA and launched thanks to a C++ script. Data recorded are analyzed with python programs.

Temperature tests

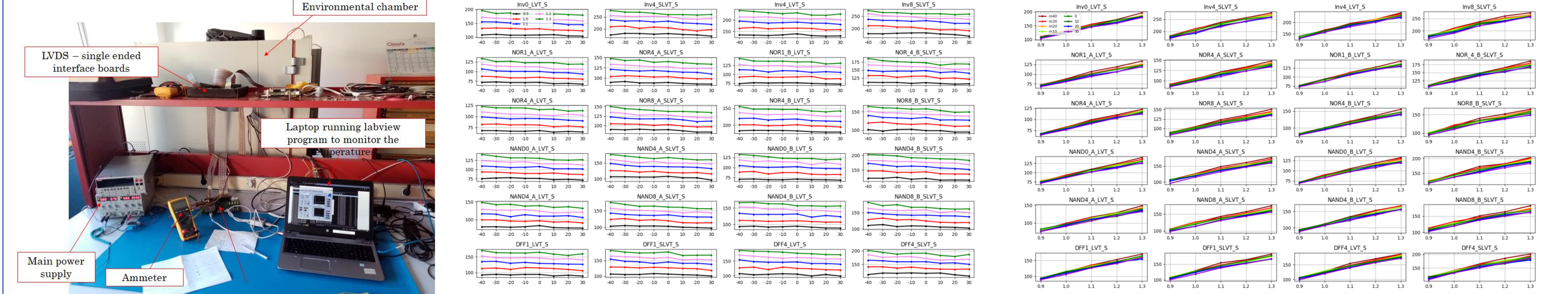

Fig4. Temperature tests set-up *Fig5. Frequency vs t°C for different Vddd* *Fig6. Frequency vs Vddd for different t°C*

A climate chamber regulating the temperature from -40 to 80°C was used for the temperature tests that were performed for different Vddd. **Each RO exhibits a decrease of the frequency while the temperature increases (5-10 % over 70°C).**

Irradiation campains

Fig7. Left: global view of the irradiation setup. Right: installation inside of the X-ray machine.

Two chips (1 and 2) have been irradiated, at ambient temperature with an X-ray machine, **up to 830 and 520 Mrad respectively** (20% attenuation can occur due to a 3µm thick stack-up of copper on the top side). The dose rate delivered was 20 kRad/mn (calibration performed with an AXUVH5 photo-diode + 150 µm thick Al filter before each campaign). During the exposure time, the ring oscillators from the functional bank were kept oscillating while the ones from the static bank were not. Regular measurements of the frequencies, with both banks put in oscillating mode, were performed along the irradiation periods.
During the first period (spring) the temperature was stable around 25°C in the chamber, while during the second one (summer) we suffered from warm temperature that affected the X-ray tube cooling system and we had to stop at a lower TID (520 Mrad). Nevertheless, **both chips responded similarly to the irradiation and exhibited a decrease (up to 25%)** of the frequencies. We observed differences between ring oscillators, depending on the type, length, and threshold of the transistors of the base cells.

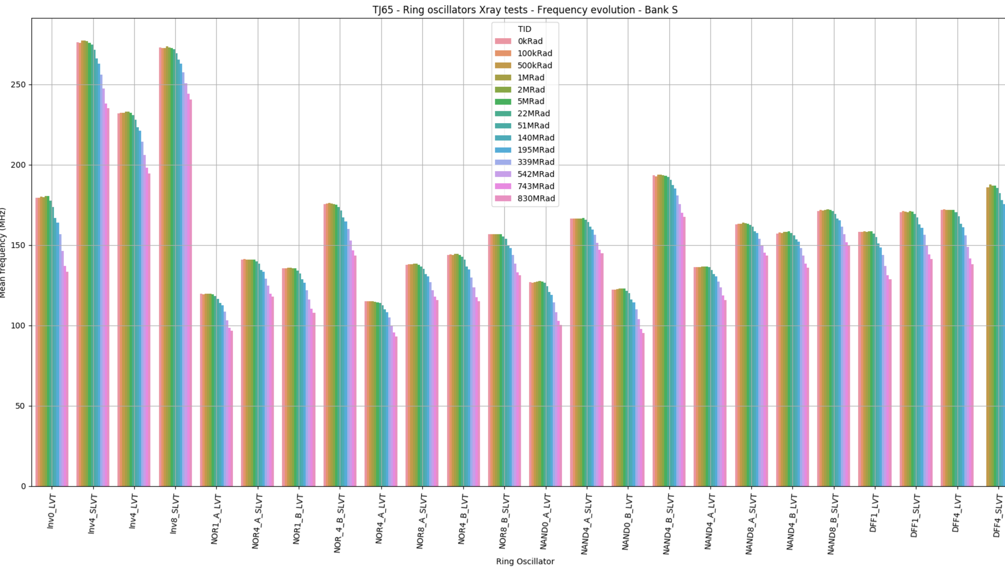

Fig8. Frequency for each TID and each RO (chip1, bank S).

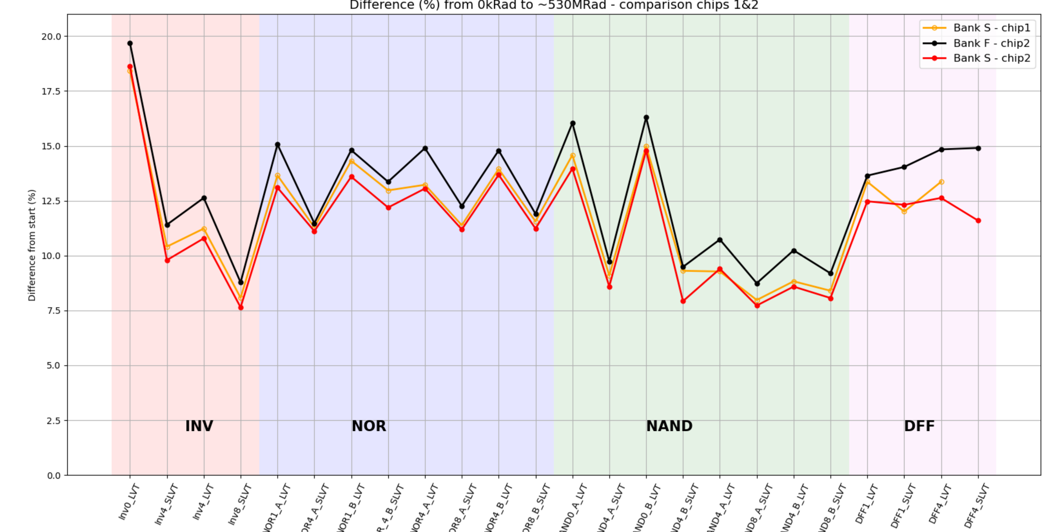

Fig9. Relative frequency difference (before-after irradiation) for each ring oscillator (chip1, bank S, chip2 banks F & S).

It is worth noticing that the functional bank of the chip1 was incorrectly configured during the irradiation and therefore was also kept static. This resulted in measurements similar for the two banks of this chip. For chip2, **the two banks were configured properly and differences (few %) between static and functional banks were observed**.

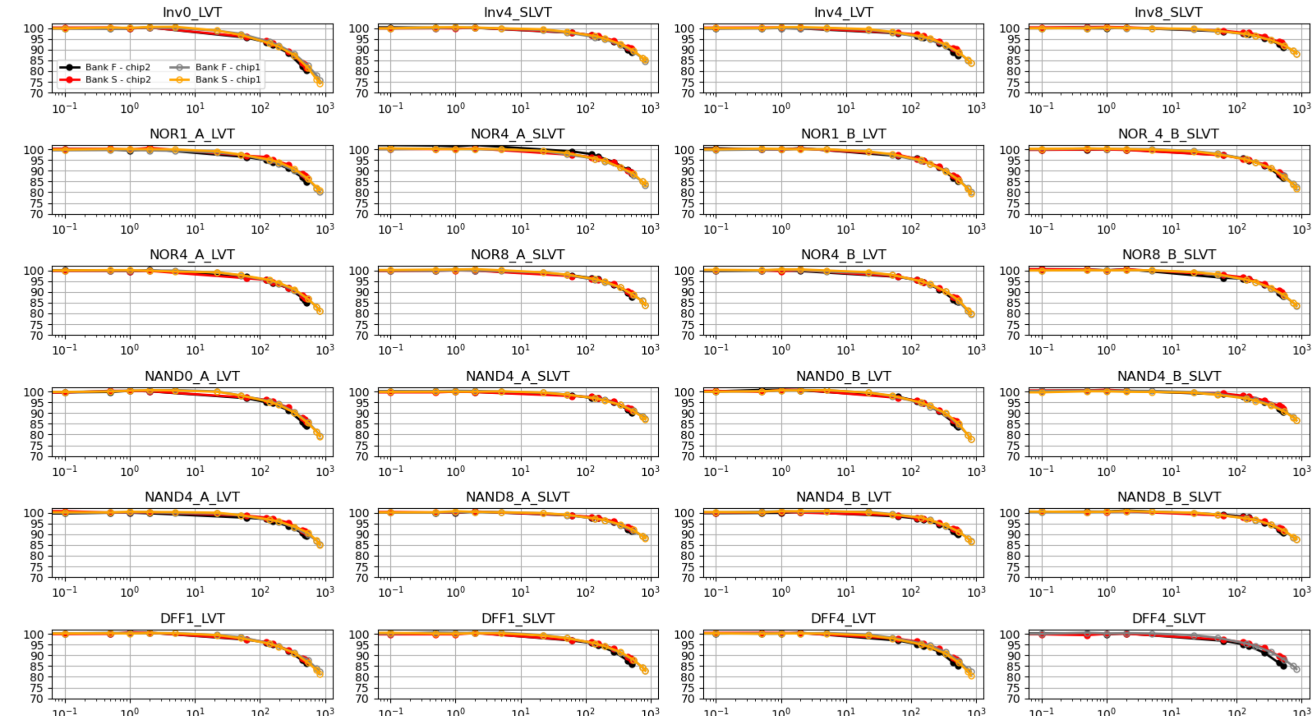

Fig10. Relative frequency vs TID (log scale) for all ring oscillators, both chips and banks.

Annealing

After irradiation, the chips went for annealing periods at three different temperatures, successively -20, 25 and 80 °C, following a procedure described in a document from the ESA (E. B. S. No, *22900,"Total dose steady-state irradiation test method," Issue 3 (2007)*).
The duration of each period was adjusted from 1 week to several weeks.
At -20°C, the DUT board was installed in a freezer and the DAQ system on a table next to it.
At 25°C, the DUT board was relocated next to the DAQ system in a regulated room. Finally at 80°C the DUT board was installed in the same climate chamber used for the temperature tests.
We applied a correction to take into account the temperature difference of the three annealing periods. **For all the ring oscillators, we observed no recovery at cold temperature (-20°C), a small recovery at room (25°C) and what looks to be a reverse annealing at warm temperature (80°C).**

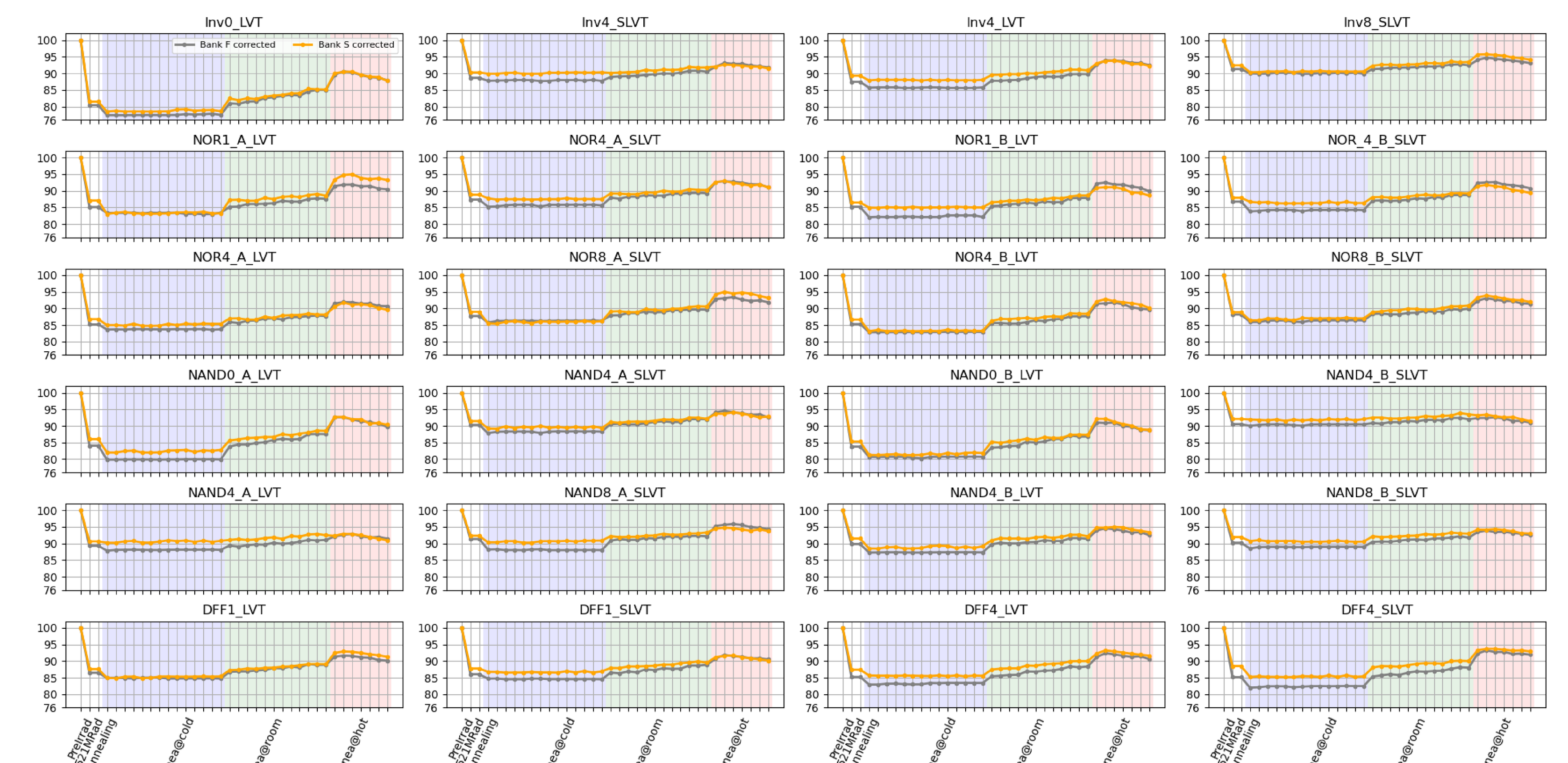

Fig11. Relative frequency vs TID and annealing time for all ring oscillators and both banks (chip 2).

Conclusions

The study of radiation hardness of TPSCo 65nm (TJ65) technology based on ring oscillators measurements showed relevant results. The frequencies decreased for all types of ring oscillators exhibiting different impact of the TID (**from 12 to 25% at 830 Mrad**). This limited degradation **opens perspective** for the usage of digital cells of this technology in high radiation environments. The temperature has an impact that can be quantified and corrected. Finally, the annealing period at high temperature (80°C) can be interpreted like a reverse annealing behavior and must be considered for the future developments in this technology.