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Digital cells radiation hardness study of TPSCo 65nm ISC technology by designing a Ring Oscillator

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The CPPM group has long been designing and testing HV-CMOS blocks to complete monolithic chips in various technologies (TJ180, LF150, AMS) in the framework of several collaborations. In 2020, we participated in the MLR1 run in TowerJazz 65 nm technology through CERN's EP-R&D WP1.2, by designing a ring oscillator test chip. Its aim is to characterize the standard cells of this technology and evaluate their radiation hardness against TID. There were 48 ring oscillators formed of different cells with different sizes and two thresholds. In 2022, characterization, temperature and Xray irradiation tests took place, leading to encouraging results presented here.

Summary (500 words)

Since more than a decade, the CPPM group participated, within international collaborations, in the design and tests of Depleted CMOS circuits developed in several technologies such as TowerJazz 180nm. Recently, in 2020, we joined a common effort (CERN EP-R&D work package 1.2) aiming to submit blocks or test chips in TPSCo 65nm ISC technology.
Our task was to design a large set of ring oscillators differing from each other by the type of cells they are made of (Inverter, NAND, NOR and DFF), with variations in length (e.g: Inv0, Inv4 and Inv8) and threshold (Low VT and Super Low VT). In total 24 different ring oscillators were designed and duplicated to form two identical banks: the Functional (or "F") bank which is made to oscillate during irradiation and the Static (or "S") bank, under bias in a static state while the chip is being irradiated. The objective is to study the effect of Total Ionizing Dose (TID) on various library cells, as well as the difference in damage due to irradiation, between static logic cells and commutating logic cells.
Each bank is controlled by a Start/Stop signal, that puts the entire bank into oscillation mode while high. All the ring oscillator outputs are being multiplexed into the input of a single 12-bit counter at the bottom of the chip. From the outside, the tester has access to the 12 bits, which can be read in DC mode to determine the number of oscillations in a certain time window. The counter bits can also be used as frequency dividers to monitor any ring oscillator in real time. Each ring oscillator is composed of 101 cells forming a chain, interrupted by an AND gate, that commands the start/stop of the cell.
The chip, powered with 1.2V, has dimensions of 1.5 mm x 1.5 mm, and a total of 48 pads. It was tested on a DUT board developed at CPPM. The test set-up comprises a BeagleBone mother board, with a dedicated firmware, running a c++ script used to configure and measure the ring oscillators individually or sequentially. Pre-irradiation, the frequency standard values are typically ranging from 100 to 300 MHz (post-layout simulation and characterization at room temperature).
Two main test campaigns were carried out after initial standard functioning: temperature tests within a climate chamber with the temperature of the device under test locally regulated by a Peltier system, and irradiation tests (TID) with an Xray machine providing a dose rate of 20kRad/mn.
The simulation and laboratory measurements showed little influence of the temperature on the ring oscillator frequency: typical 5% decrease from -40 to 30 ℃.
The irradiation measurements, up to extreme total ionising doses, showed a decrease of the frequency value from 12% to 25% depending on the cells and no clear sign of difference between the two banks.

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