Radiation hard True Single Phase Clock Logic for high-speed circuits in 28 nm CMOS

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Motivation

The **DART28** is an ASIC being developed in the context of the Experimental-Physics Department research programme for the development of detectors and detector systems for the future High Energy Physics experiments at CERN. Circuits designed in this framework are implemented in a 28 nm CMOS technology and have to be optimized for performance and radiation hardness. The 28 nm devices suffer from high leakage currents due to total ionizing dose (TID) radiation effects. This is problematic for dynamic True Single Phase Clock (TSPC) Flip-Flops. In such a Flip-Flop information is stored dynamically as a charge on a node capacitance. Excessive leakage currents lead thus to data corruption. This poster presents an in-depth analysis on the requirements and mitigation strategies for the TSPC Flip-Flops.

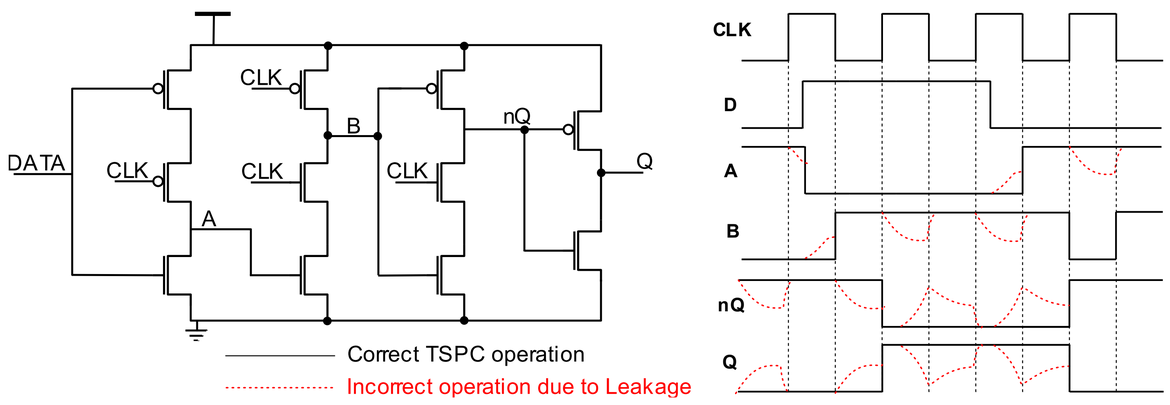

Figure 1. Schematic of the TSPC FF [1] with waveforms demonstrating the leakage problem in that circuit

Leakage current modeling

A leakage simulation model was developed based on the detailed characterization of the selected technology, performed in [2] and [3]. It is shown that the TID-induced leakage current increase is caused by two main effects: (i) V_T shift and (ii) radiation-induced drain to source leakage. Both effects are included in the developed VerilogA model:

- **V_T shift** – The model includes a static TID-dependent gate voltage offset. The value of the offset voltage is width dependent. Measurement data is stored in a database and linearly interpolated.
- **Radiation-induced drain-source leakage current** – Caused by parasitic lateral devices. It is modelled by the equation presented by Zhang et al. in [3]:

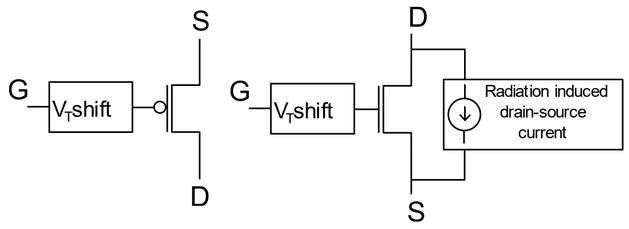

Figure 2. Schematic of the pMOS and nMOS models with TID-dependent VerilogA models

$$I_{Leakage}(TID) = I_{PreRad}\left(\frac{TID}{TID_{critical}}\right)^{k},$$

where k is a Length dependent coefficient and $TID_{critical}$ is the radiation dose at which current from the parasitic devices is equal to main channel leakage. A dependency on V_{DS} was implemented in the VerilogA model to represent realistic circuit behaviour, extrapolated from foundry models. The I-V characteristics of each transistor size were approximated with a polynomial to approximate I_{PreRad} for different conditions. The pMOS transistors have no drain-source leakage model because the oxide traps in fact cause a leakage current decrease.

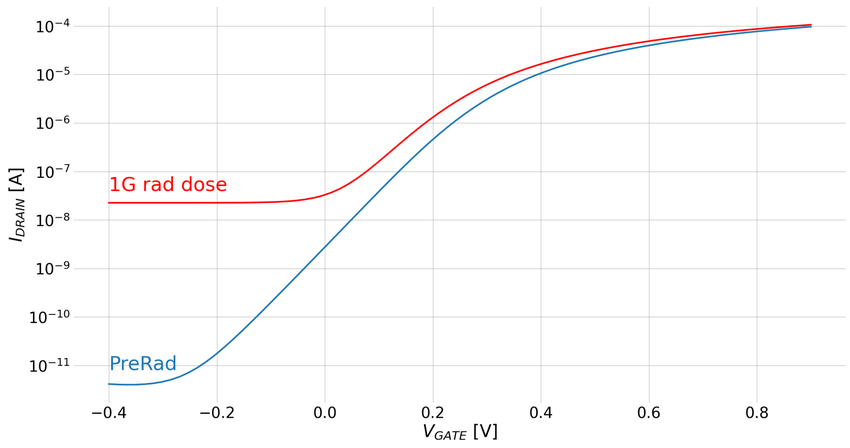

Figure 3. Characteristics of nMOS transistor obtained with the designed model for different TID (V_{DS} =V_{DD})

Analyzed circuits

To assess the benefits and risks of using dynamic logic (Flip-flops and Latches) in 28 nm technology, three types of circuits have been analysed:

- **Static -** master-slave CMOS architecture
- **TSPC -** Basic architecture (without keepers) (see **Figure 1**)
- **TSPC with leakage protection -** Uses additional weak gated inverters (keepers) on the sensitive nodes (see **Figure 4**)

All test circuits have been simulated with the described leakage models

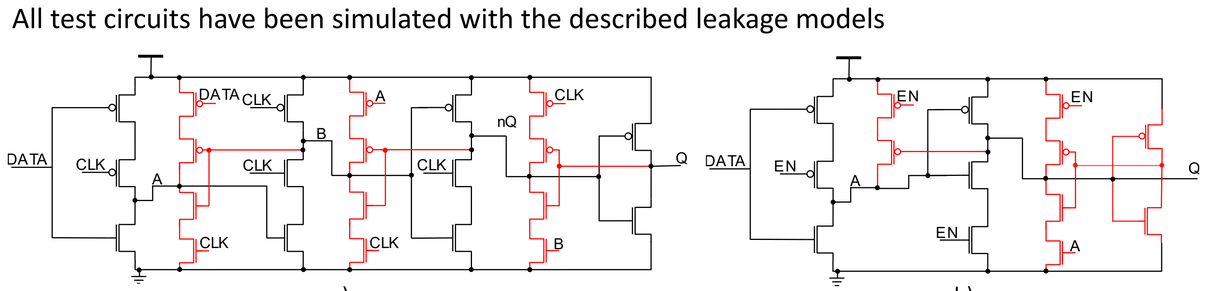

Figure 4. Schematic of (a) TSPC FF [4] and (b) TSPC Latch; both with leakage protection devices in red

TID simulation results

Simulations for doses up to 1 Grad have been performed. The minimum clock frequency was defined as a frequency at which the FF is not able to retain the previously stored value due to leakage current. The threshold values of 65 % and 41 % of the supply voltage were used for high and low levels, respectively.

Table 1. Results of the analyzed Flip Flops

Parameter	Static		TSPC		TSPC protected	
	PreRad	1 Grad	PreRad	1 Grad	PreRad	1 Grad
Minimum Frequency [MHz] nominal PVT case	0	0	104	302	**0**	**0**
Minimum Frequency [MHz] Max Leak. PVT case (FF – High T)	0	0	3500	7470	**0**	**0**
Maximum Frequency [GHz]	50	50	95	86	**73**	**73**
Energy per bit [fJ/bit] (PreRad)	6.86		4.26		**4.85**	
Area [um^2]	3.04		2.53		**3.88**	

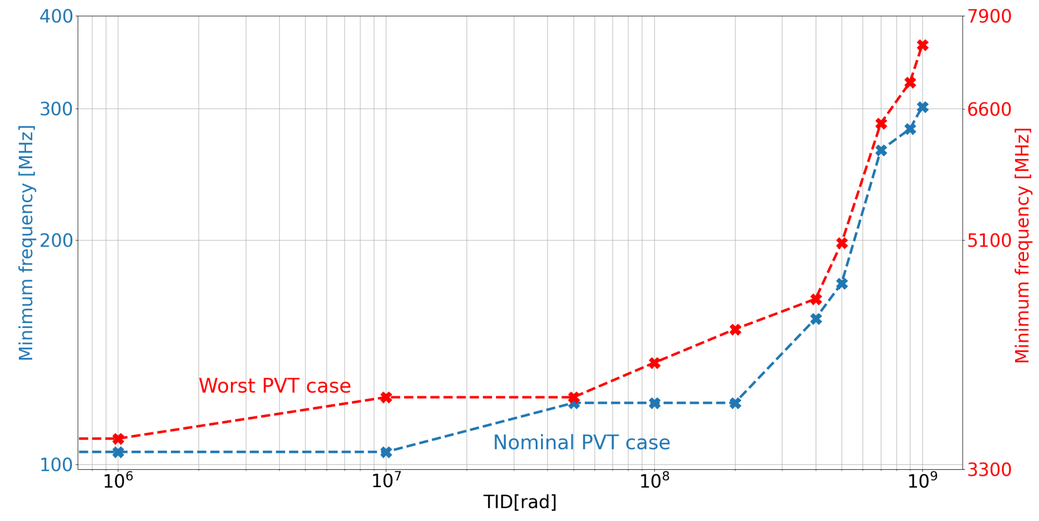

Figure 5. The minimum frequency (due to leakage current) with TID for TSPC FF

The results were obtained for the nominal and the worst leakage corner. The increase of the minimum frequency is significant which can triple at 1 Grad. This significantly limits the application of the standard TSPC in radiation environments. The circuit with leakage protection is robust against radiation-induced leakage, retaining its data even at 1G rad TID, at the cost of a moderate power/area penalty. Figure 5 shows that the most significant increase of minimum frequency occurs above 200 Mrad when leakage current becomes significant and affects the storage nodes. A similar investigation was done for dynamic latches, but here standard TSPC architecture is even more problematic due to bigger transistors and more direct influence of the leakage current on the output state.

Table 2. Results for the analyzed Latches

Parameter	Static		TSPC		TSPC protected	
	PreRad	1 Grad	PreRad	1 Grad	PreRad	1 Grad
Minimum Frequency [MHz] nominal PVT case	0	0	300	970	**0**	**0**
Minimum Frequency [MHz] Max Leak. PVT case (FF – High T)	0	0	3780	5750	**0**	**0**
Maximum Frequency [GHz]	38	38	70	70	**62**	**62**
Energy per bit [fJ/bit]	6.83		2.39		**3.24**	

Critical charge simulation results

To compare the Single Event Upset (SEU) sensitivity of the topology considered, the critical charge was analysed. In order to estimate this charge, a double exponential current pulse [5] with time constants, t_r= 15ps, and t_f=50ps was injected into all nodes of the circuit. The charge was gradually increased until an upset was detected at the output. Simulations have been performed for the nominal corner.

Parameter	Architecture		
	Static	TSPC	TSPC protected
Critical charge for Flip Flop [fC]	25.6	0.8	**10.7**
Critical charge for Latch [fC]	23.1	1.6	**10.8**

Results show that the protected Flip Flops and Latches have a critical charge an order of magnitude higher than standard TSPC architecture, but still smaller than the static circuits.

Conclusions

A strategy for circuit validation in terms of leakage has been developed. The validation process showed that TSCP Flip Flops with leakage protection are not sensitive to TID-induced leakage up to 1 Grad with only a **23%** decrease in speed, a **14%** increase in power consumption, and a **53%** increase in the occupied area. At the same time, the proposed circuit is still showing a much better performance than a static master-slave flip flop. According to the results, leakage protection must be considered in high TID and high-temperature environments. Based on the obtained critical charges, the protected TSPC FF shows a higher SEU robustness than the classic TSPC FF.

References

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