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Radiation hard True Single Phase Clock logic for high-speed circuits in 28 nm CMOS

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TSPC dynamic logic is widely used in high-speed circuits like high-speed SERDES or frequency dividers. TSPC flip-flops are characterized by their high operation speed and low power consumption when compared with static flip-flops. Due to the relatively high leakage currents in the modern CMOS process, the use of leakage protection techniques of the storage nodes of TSPC logic is mandatory. In this paper Single Event Upsets (SEU) are investigated by quantifying the critical charge needed to upset the leakage protected TSPC flip-flops. The results are compared to both the static and traditional TSPC circuits without leakage mitigation.

Summary (500 words)

The True Single-Phase Clock (TSPC) dynamic logic family is often used in high-speed circuits because of its capability to work at multi-GHz frequencies combined with reasonable power consumption and area. In serial communication systems, TSPC flip-flops and latches are used in serializers and frequency dividers which operate at the highest system frequencies and therefore pose the biggest design challenges. For High Energy Physics applications, these circuits should exhibit sufficiently high maximum operating frequency as well as be robust against high levels of Total Ionization Dose (TID) and Single Event Upsets (SEU) robust.

Unfortunately, implementing such circuits in deep-submicron technologies, such as in 28 nm bulk CMOS, reveals a severe leakage issue that causes the charge stored in the dynamic nodes to drain rapidly. For different Process Voltage and Temperature (PVT) conditions, the leakage current could vary by more than two orders of magnitude, causing operational failures even at frequencies as high as 1GHz, since dynamically stored nodes leak so quickly. Moreover, research on the TID influence in 28 nm shows that the leakage current could increase by almost one order of magnitude after 1 Grad of the total dose. Therefore, for robust design, an additional margin for the TID-induced leakage is required. To overcome this problem, a design with leakage mitigation structures was adopted. The solution uses gated inverters as state keepers when the sensitive nodes are in the hold state to prevent signal level degradation. Those inverters are using additional PMOS and NMOS transistors as a key to control the activation of the inverter which inverts data stored in the preceding node of the TSPC device. Such a circuit protects against leakage in all PVT corners and ensures a large margin to address the TID-induced leakage, guarantying robustness up to 1 Grad while decreasing the maximum operating frequency by only 15% with a similar increase in power consumption.

In this work, the architecture, performance, critical charge, and TID robustness of leakage-protected TSPC flip-flops and latches are compared to standard static and TSPC flip-flops without leakage protection. The results are obtained by simulation. To verify the leakage mitigation strategy, the excess leakage current at higher TID levels has been modeled and injected into the sensitive nodes. The critical charges for various nodes have been estimated through simulations to study the SEU sensitivity of the modified TSPC architecture. The obtained results are compared to other architectures. Detailed results will be presented at the conference.

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