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Radiation effect evaluation of digital building blocks in a 28 nm CMOS technology

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The 28nm bulk CMOS technology is a promising candidate as most advanced node for future design in the High Energy Physics (HEP) community. Three ASICs have been designed to evaluate performances and radiation tolerance, both against Single Event Effects and Total Ionizing Dose, of the digital standard cells libraries and foundry SRAMs. This contribution aims at presenting the custom-developed structures together with the obtained test results, providing crucial information for assessing the sensitivity of this technology to extreme radiation environment and allowing designers to take adequate mitigations techniques in this technology node.

Summary (500 words)

Application-Specific Integrated Circuits (ASICs) instrument all particle detectors at the CERN Large Hadron Collider (LHC). In the context of the Strategic R&D on Technologies for Future Experiment, the 28nm bulk CMOS process has been targeted as common technology for the implementation of the future ASICs in HEP applications. Its performances far exceed those of previous technologies and early tests have shown it to be particularly robust to Total Ionizing Dose (TID), possibly enabling the design of ASICs capable of operating in multi-Grad environments. For this reason, a family of 3 ASICs (EXPloit28 (EXP28)) has been designed to fully characterize radiation effects on this technology node. The three chips are called EXP28_SEE, EXP28_TID and EXP28_ANA. Each of them has been designed to study a specific aspect of the radiation response of the technology.

Test structures in the EXP28_SEE chip allows to evaluate Single Event Effects (SEE) sensitivity of the digital standard cell libraries of the technology and SRAMs from foundry compilers. A Single Event Transient (SET) measurement circuit, based on inverter chains and Vernier delay lines is implemented to measure both the cross section and time duration of the SEE-induced transients on minimum size inverters (over a total sensitive area of ˜400x80 µm2). 7 matrices of 4096 D Flip Flops of different flavors and placed with different distance are used to evaluate cross section of Single Event Upsets (SEUs) on sequential elements. The structure is derived from a similar one used in 65nm CMOS technology, which proved to be efficient in detecting multi-bit upsets (MBUs). Four different foundry SRAM types (single and dual port, standard and high density) have been instantiated multiple times, covering a total active area of 0.76mm2 to evaluate SEU and Single Event Latch-up (SEL) on the different types of memories. Serialization and deserialization logic allows performing read and write operations on the SRAMs with a refresh rate guaranteeing the detection of MBUs.

EXP28_TID chip aims at studying the TID-induced degradation of digital standard cell libraries and memories. The investigation of dose effects on standard cells involves 368 ring oscillators (ROs), divided into 23 libraries with 16 standard cells for each library. Measurement of the change in oscillation frequency of the ROs will allow evaluation of the impact of TID in the operation of MOS transistors. The impact of TID in the memories is evaluated by four different types of foundry SRAMs. Each of them is integrated with dedicated Built-In Self-Test (BIST) circuitry that can be used to detect SRAM faults under different operating conditions and received dose.

SEL test structures embedded in the EXP28_ANA chip will allow evaluating the minimum distance between substrate contacts (taps) needed to prevent SEL.

This technology characterization step is of fundamental importance to the entire HEP community before starting any design for harsh radiation environment. The results presented in this contribution will guide ASIC developers to estimate the error rates in the envisaged application and develop circuit-level countermeasures to achieve reliable functionality in extreme radiation environments.

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