Fab-to fab and run-to-run variability in 130nm and 65nm CMOS technologies exposed to ultra-high TID

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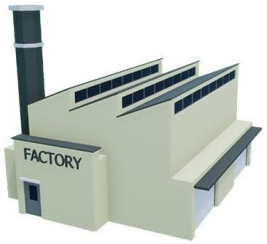
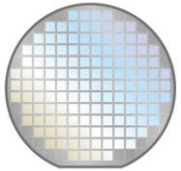
Fab 06



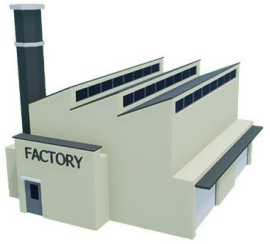


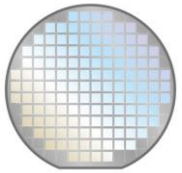
production run no.1
.
.
.
production run N

run-to-run variability

fab-to-fab variability

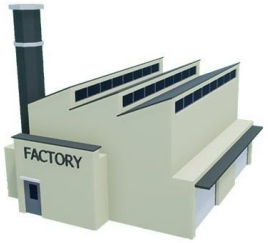
Fab 12

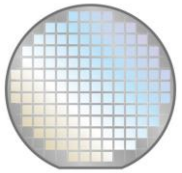




production run no.1
.
.
.
production run N

Fab 14





production run no.1
.
.
.
production run N

Large variability observed in the radiation response of 130/65nm CMOS technologies

technology monitoring chips added to each production run of ASICs designed in ME section

Rezzak, Nadia, et al. "The impact of device width on the variability of post-irradiation leakage currents in 90 and 65 nm CMOS technologies." *Microelectronics Reliability* 52.11 (2012): 2521-2526.

Gerardin, S., et al. "Enhancement of transistor-to-transistor variability due to total dose effects in 65-nm MOSFETs." *IEEE Transactions on Nuclear Science* 62.6 (2015): 2398-2403.

Over the last 8 years…

130nm

22 chips from 3 different fabs:

Fab 06 → 13 production runs
Fab 12 → 5 production runs
Fab 14 → 4 production runs

65nm

11 chips from 2 different fabs:

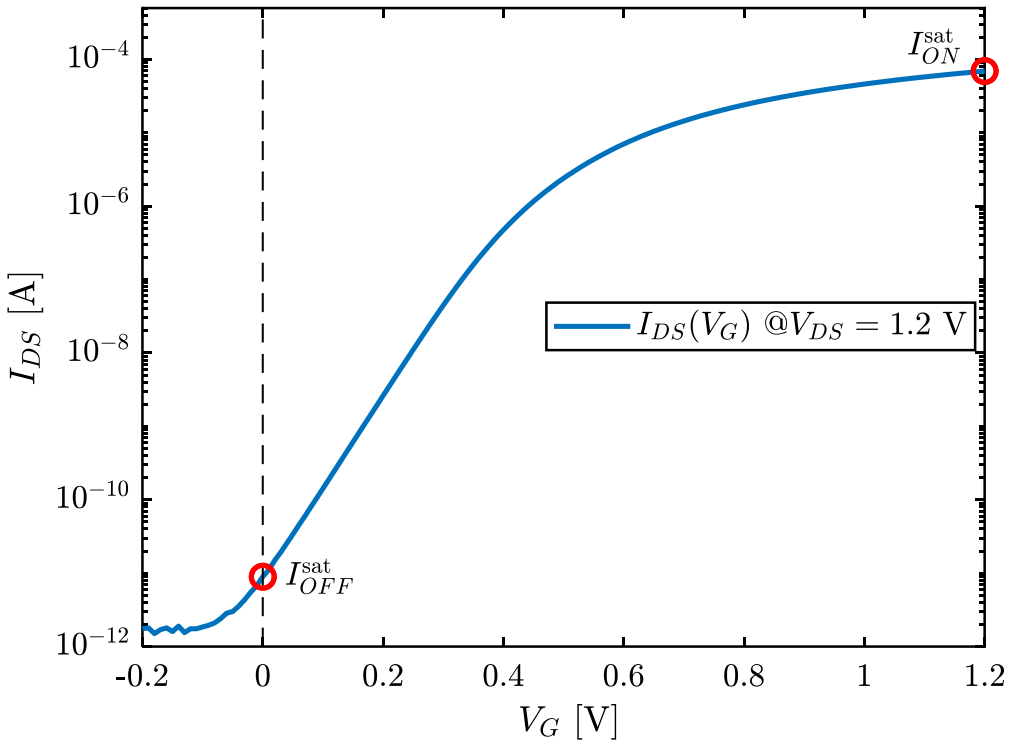
Fab 12 → 4 production runs
Fab 14 → 7 production runs

X-rays irradiations to TID ≥ 100 Mrad(SiO_2) (up to 1 Grad(SiO_2))

Two parameters:

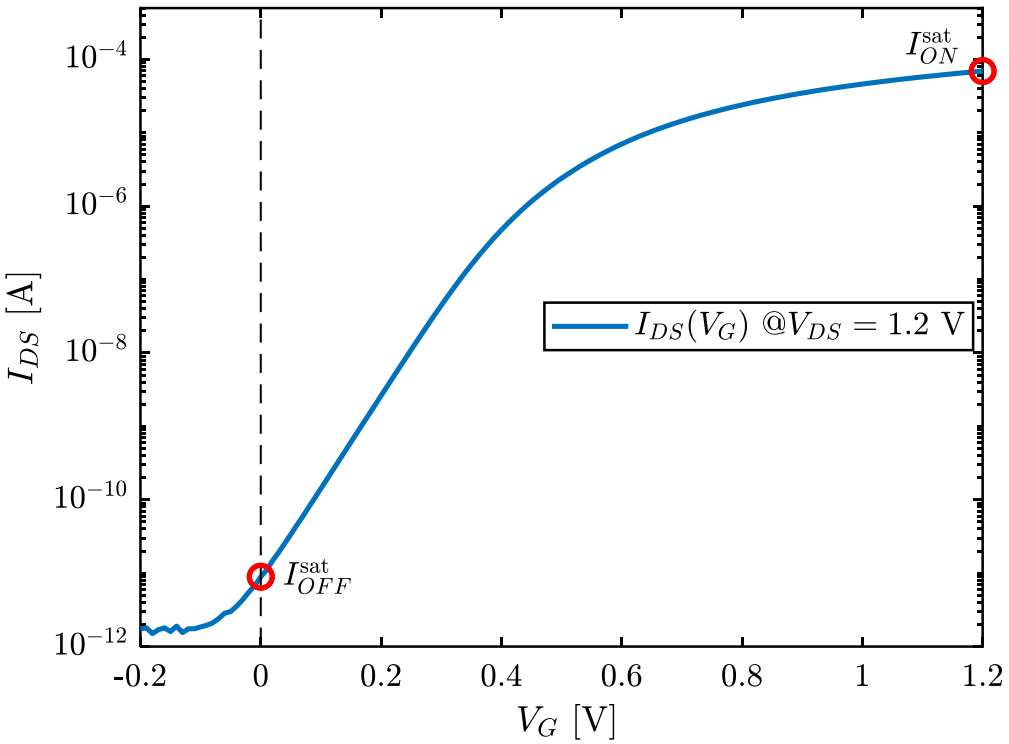
➡ IOFF

➡ ION



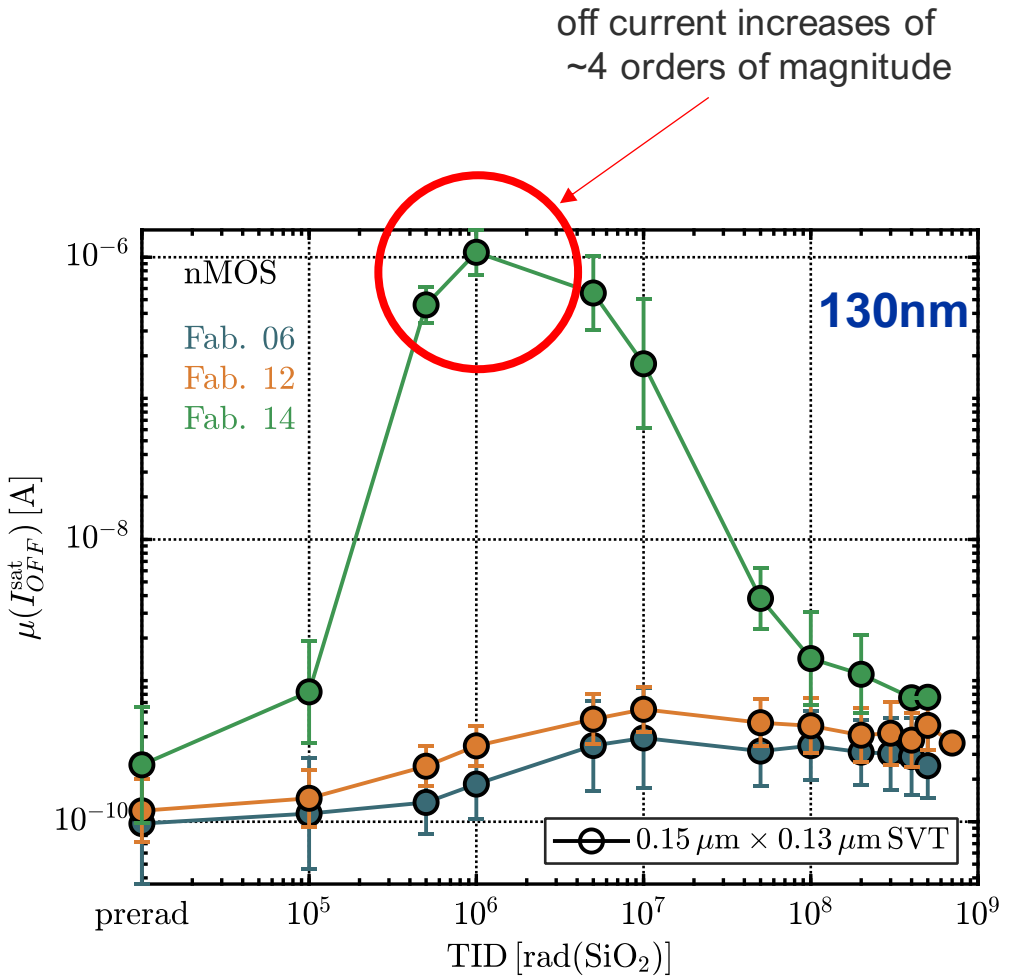
Two parameters:

- IOFF
- ION



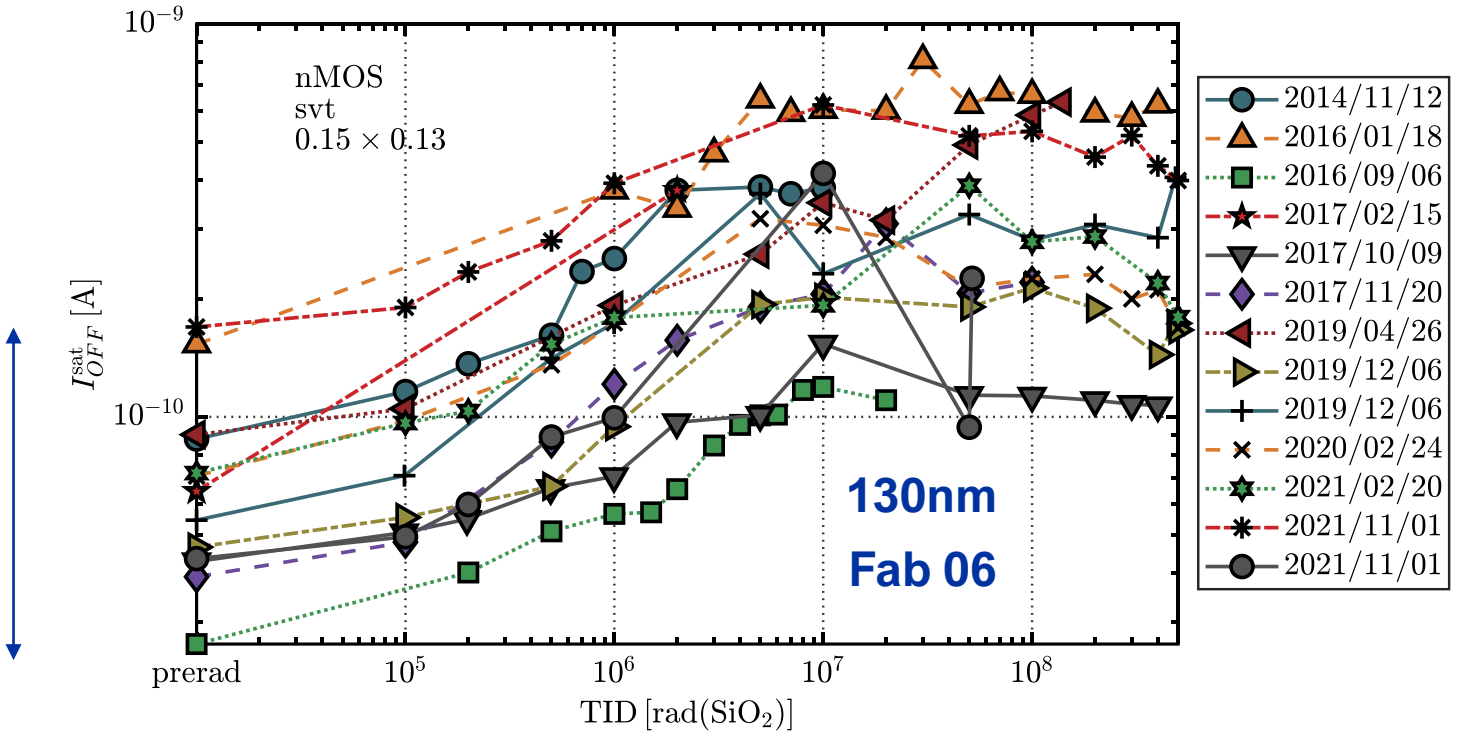
Fab-to-fab variability

mean value over all runs per fab

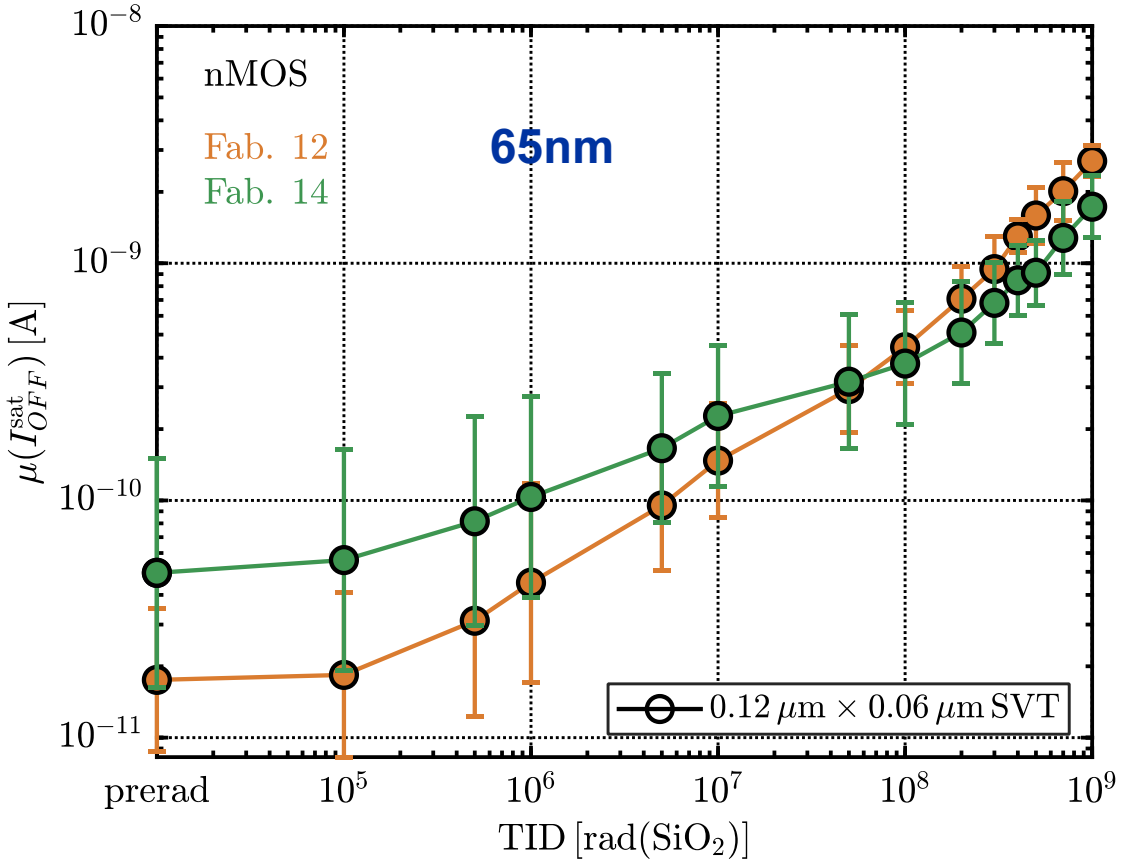


$\sigma(I_{OFF})$ ⟶ run-to-run variability

Run-to-run variability



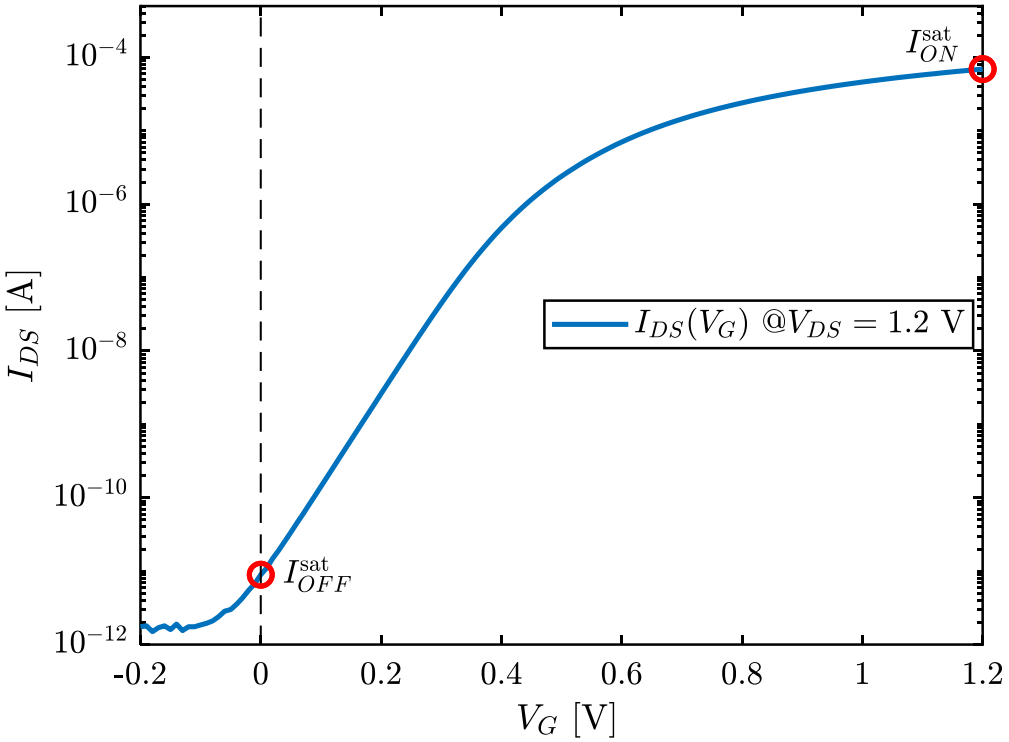
fab-to-fab variability
(less than in 130nm)



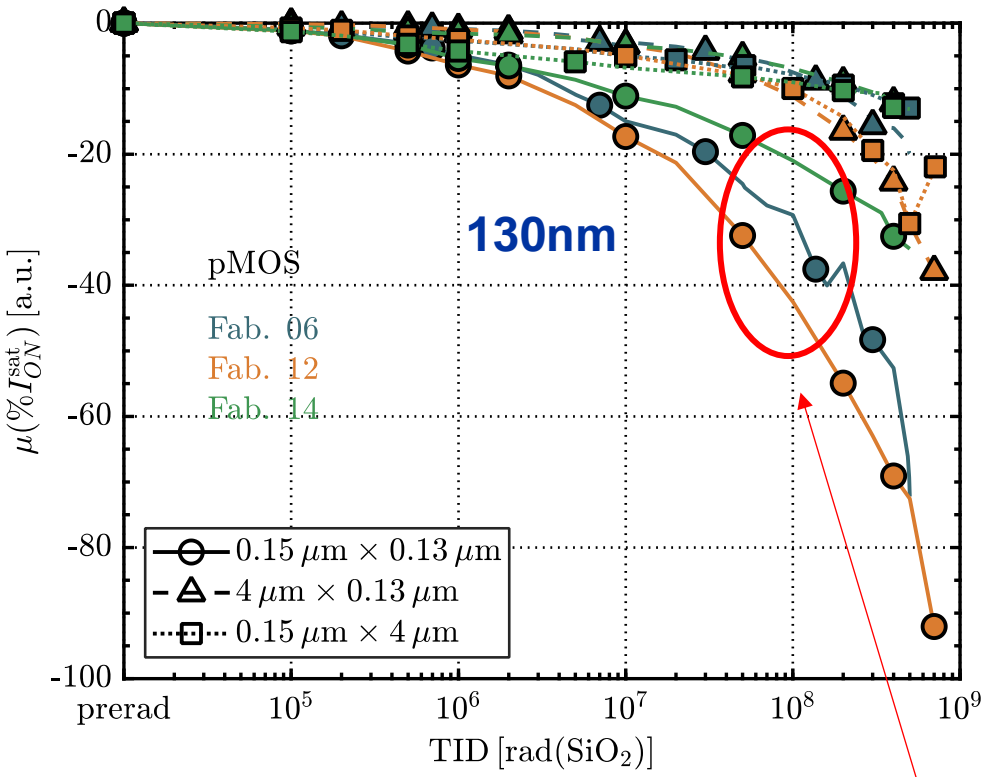
Two parameters:

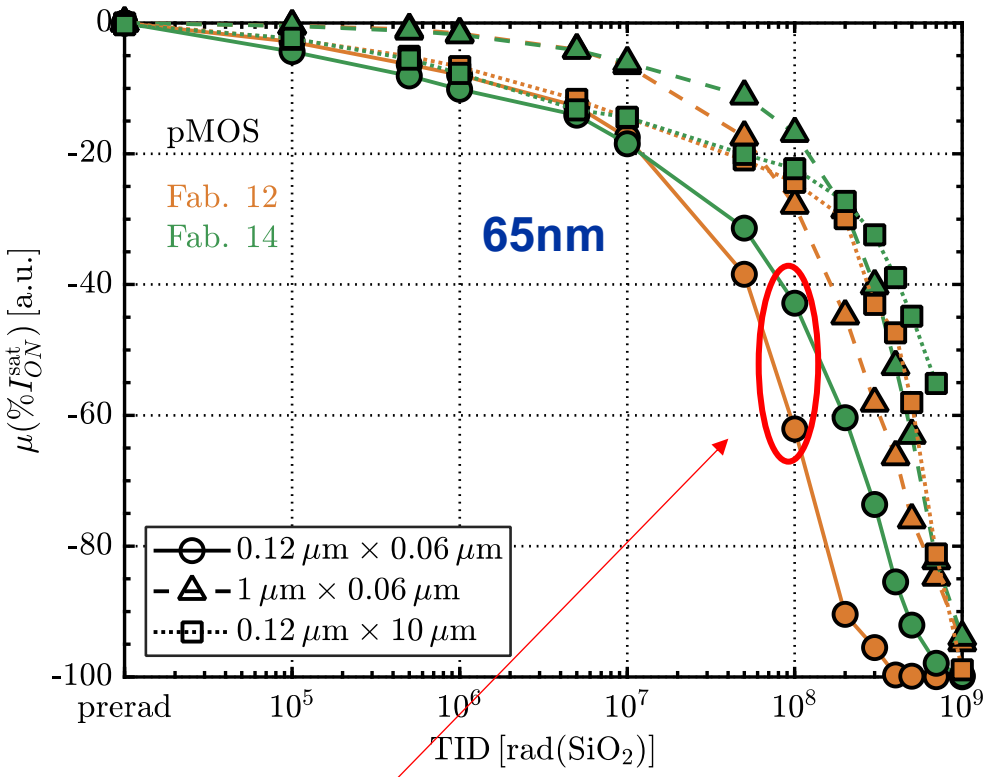
IOFF

ION



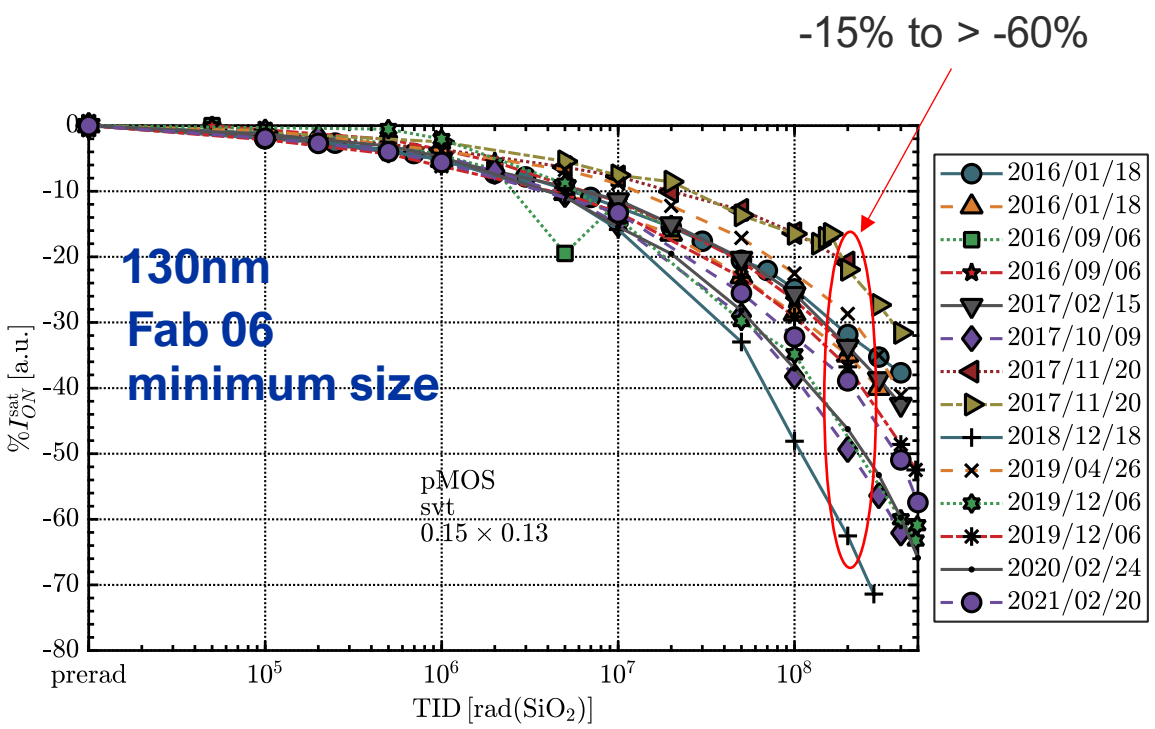
Fab-to-fab variability

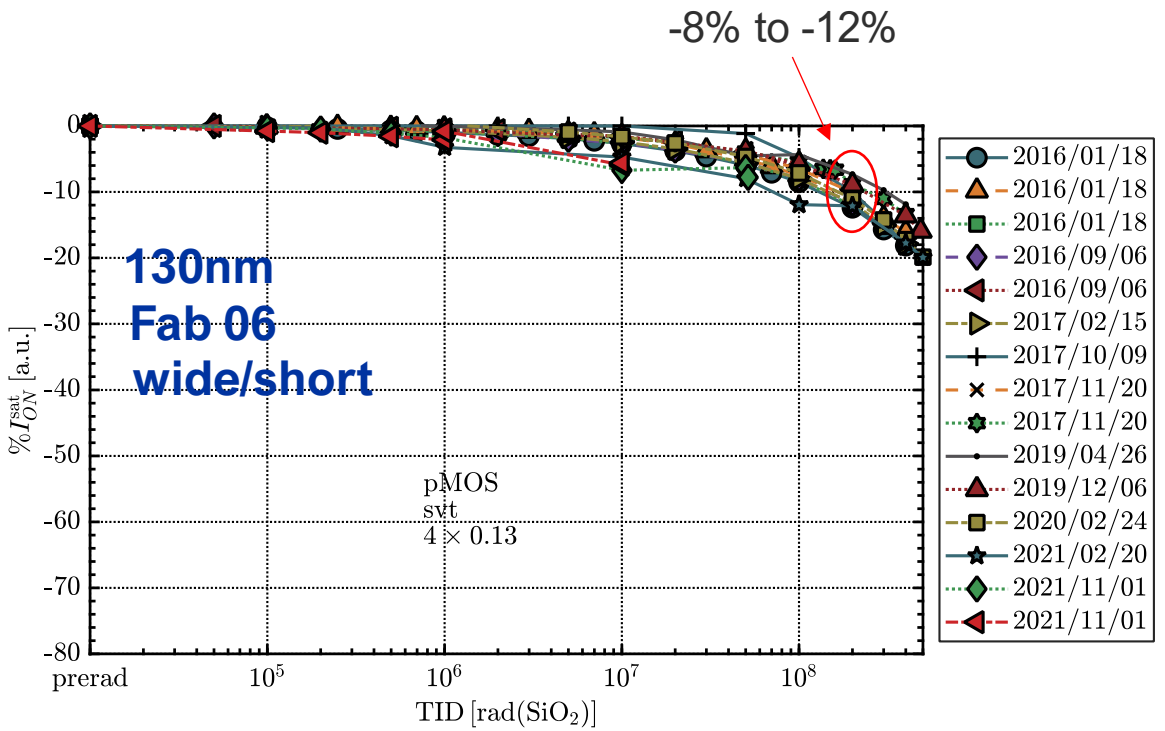




Minimum size devices exhibit the largest variability

Run-to-run variability





run-to-run variability depends on size

BSIM4 model to describe the behaviour of irradiated transistors in 65 nm CMOS technology (2018)
(in collaboration with the Technical University of Crete)
PDK available for CERN designers

radiation corners based on TID models

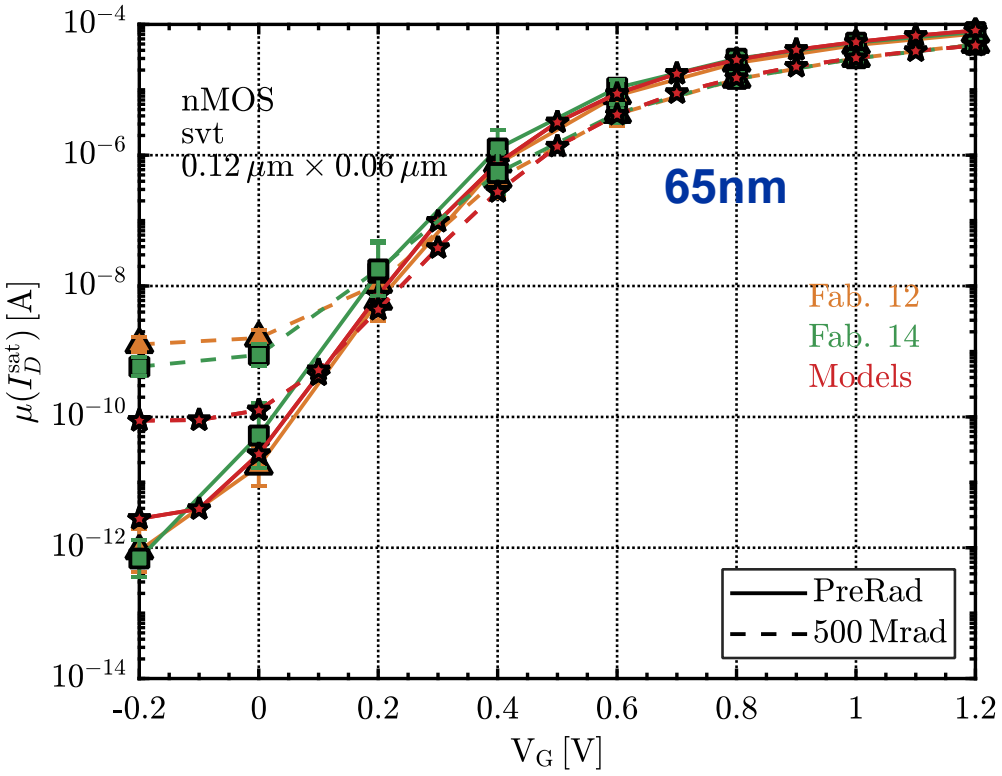
A. Nikolaou, M. Bucher, N. Makris, A. Papadopoulou, L. Chevas, G. Borghello, H. D. Koch, K. Kloukinas, T. S. Poikela, and F. Faccio. "Extending a 65nm CMOS process design kit for high total ionizing dose effects". In: *2018 7th International Conference on Modern Circuits and Systems Technologies (MOCAST)*. May 2018, pp. 1–4.

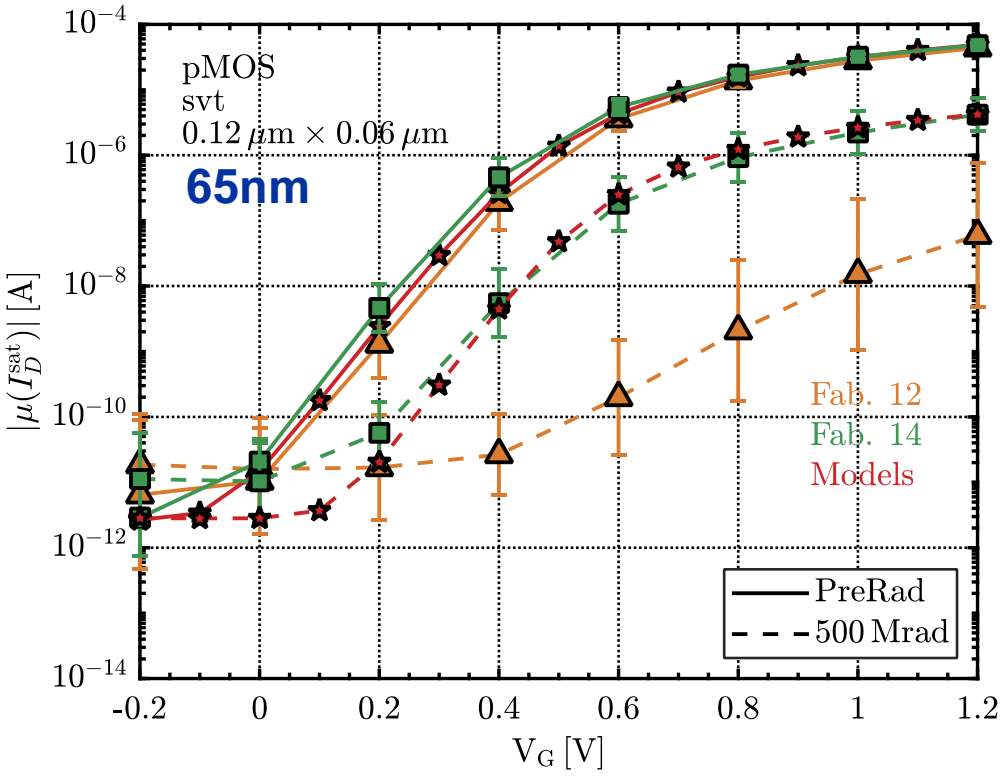
L. Chevas, A. Nikolaou, M. Bucher, N. Makris, A. Papadopoulou, A. Zografos, G. Borghello, H. Koch, and F. Faccio. "Investigation of Scaling and Temperature Effects in Total Ionizing Dose (TID) Experiments in 65 nm CMOS". In: *25th International Conference on Mixed Design of Integrated Circuits and System (MIXDES)*, Jun 2018, pp.313-318

M. Bucher, A. Nikolaou, A. Papadopoulou, N. Makris, L. Chevas, G. Borghello, H. D. Koch, and F. Faccio. "Total ionizing dose effects on analog performance of 65 nm bulk CMOS with enclosed-gate and standard layout". In: *2018 IEEE International Conference on Microelectronic Test Structures (ICMTS)*. Mar. 2018, pp. 166–170.

A. Nikolaou, M. Bucher, N. Makris, A. Papadopoulou, L. Chevas, G. Borghello, H. D. Koch, and F. Faccio. "Modeling of High Total Ionizing Dose (TID) Effects for Enclosed Layout Transistors in 65 nm Bulk CMOS". In: *2018 International Semiconductor Conference (CAS)*. Oct. 2018.

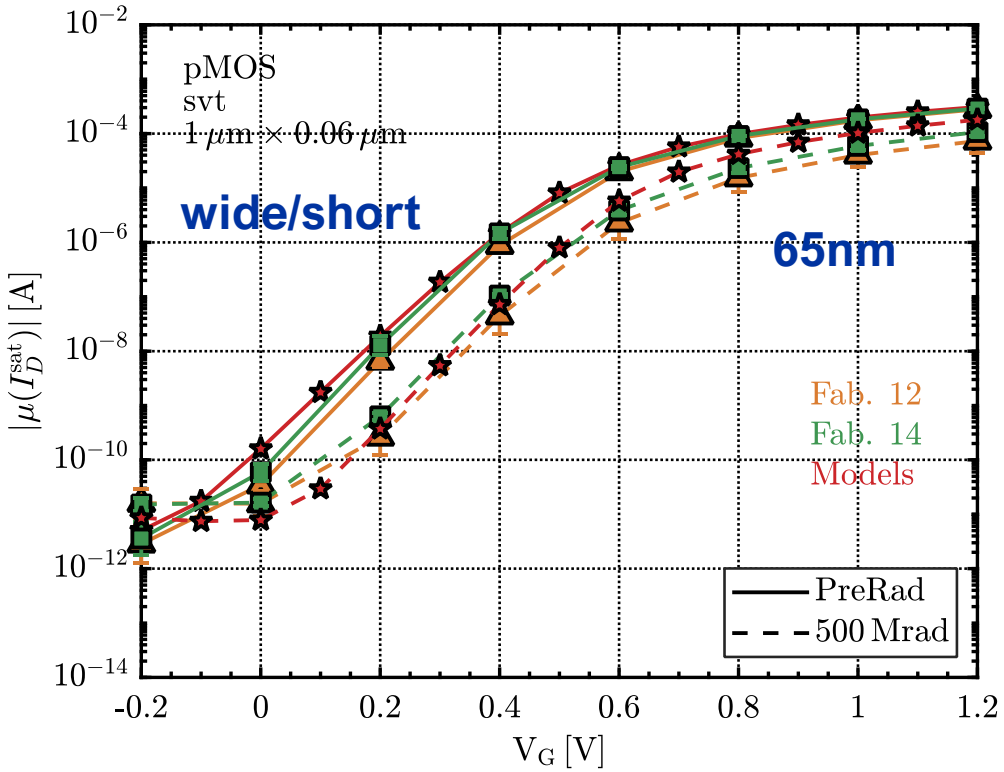
Measurements vs CERN radiation models (minimum size)

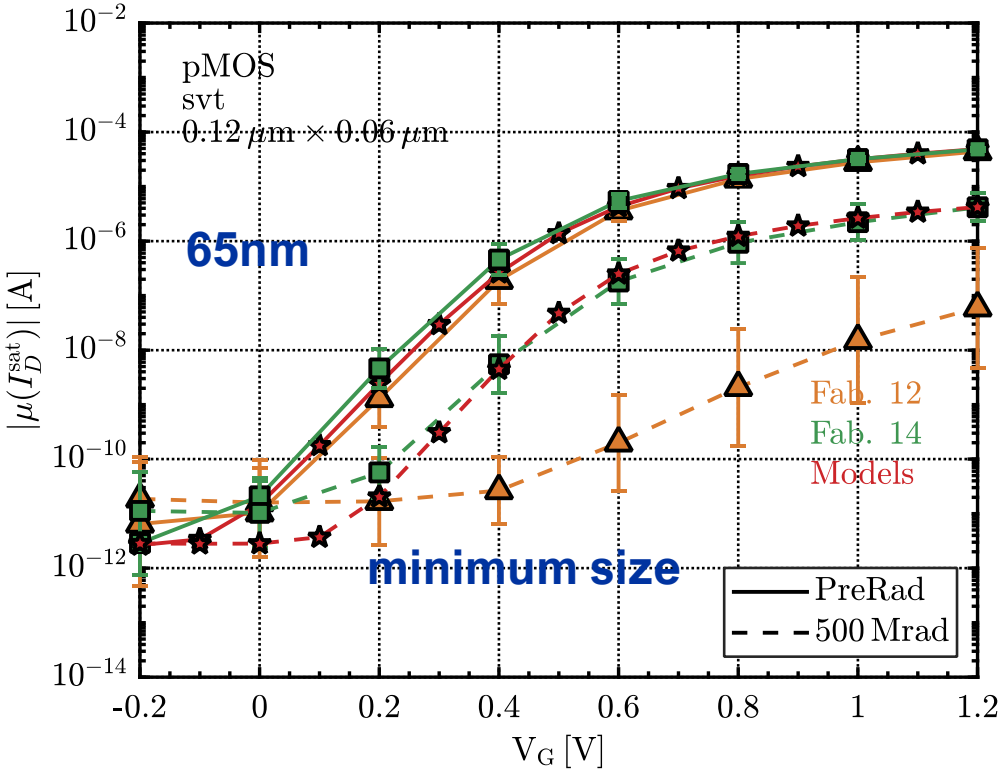




BSIM4 **typical-typical** corner

Measurements vs CERN radiation models (size dependency)





more accurate prediction even at 500 Mrad(SiO_2)
in wider devices

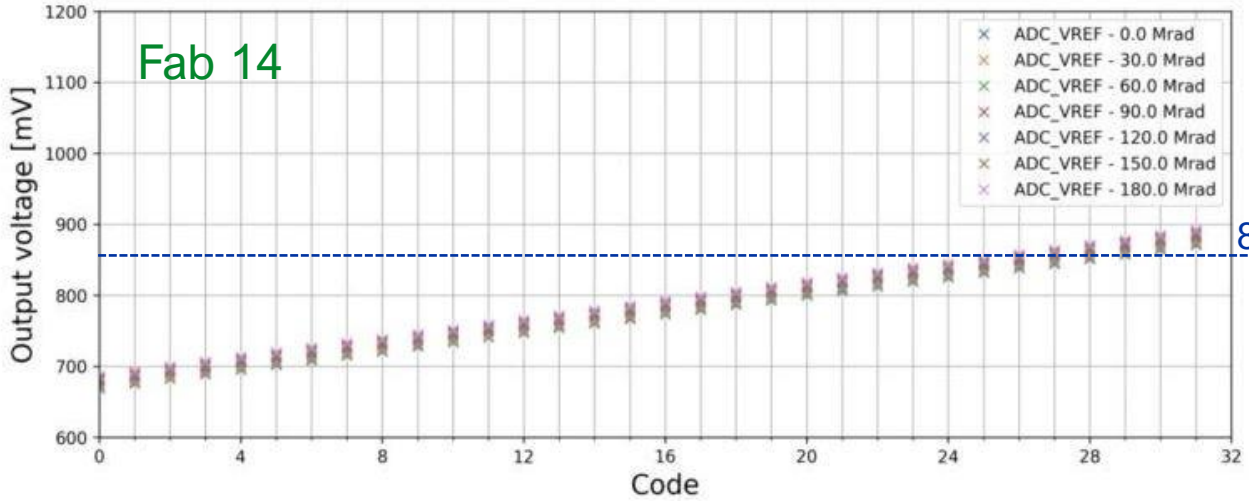
Case study : 5-bits DAC in Short Strip ASIC (SSA)

SSA: the front-end ASIC responsible of reading-out the Short-Strip silicon sensor

the DAC used to provide 850 mV as voltage reference for an ADC

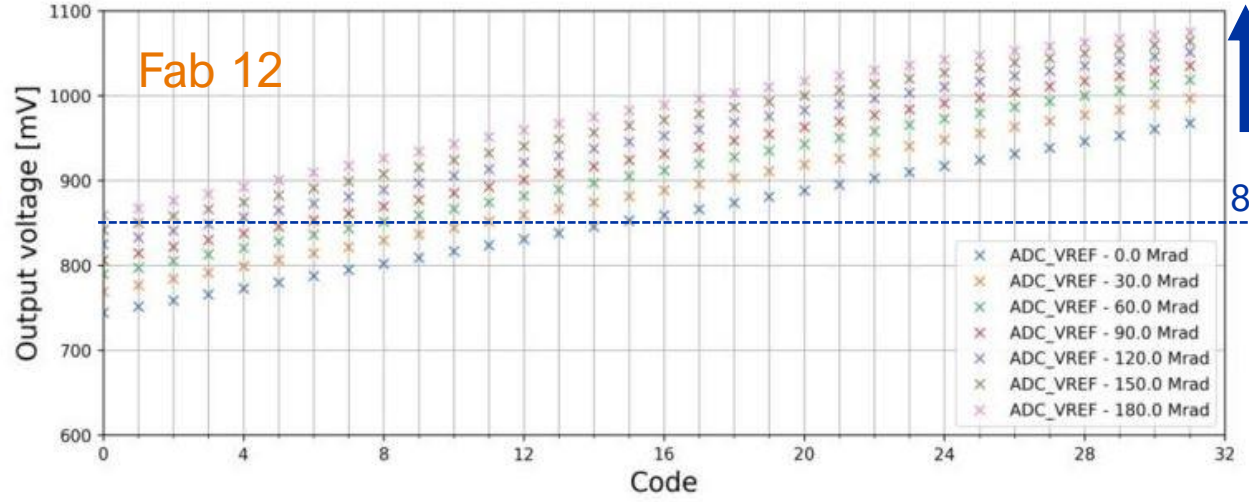
5-bits DAC output

SSA2
(MPW)



850 mV

SSA2.1
(production)



increasing TID

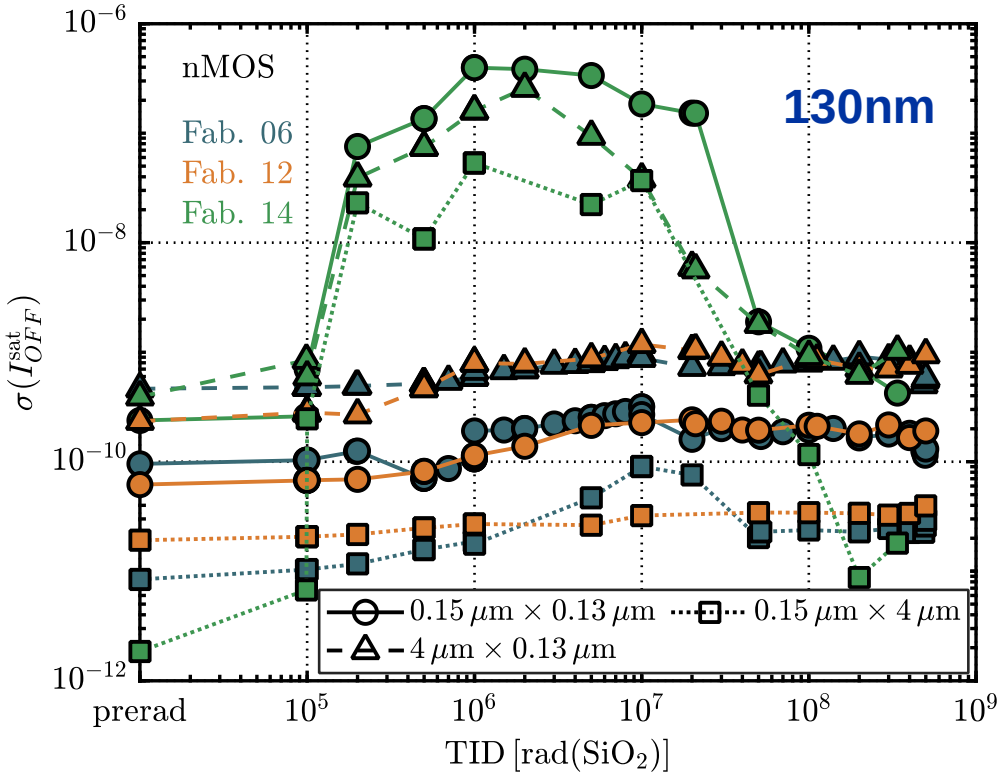
850 mV

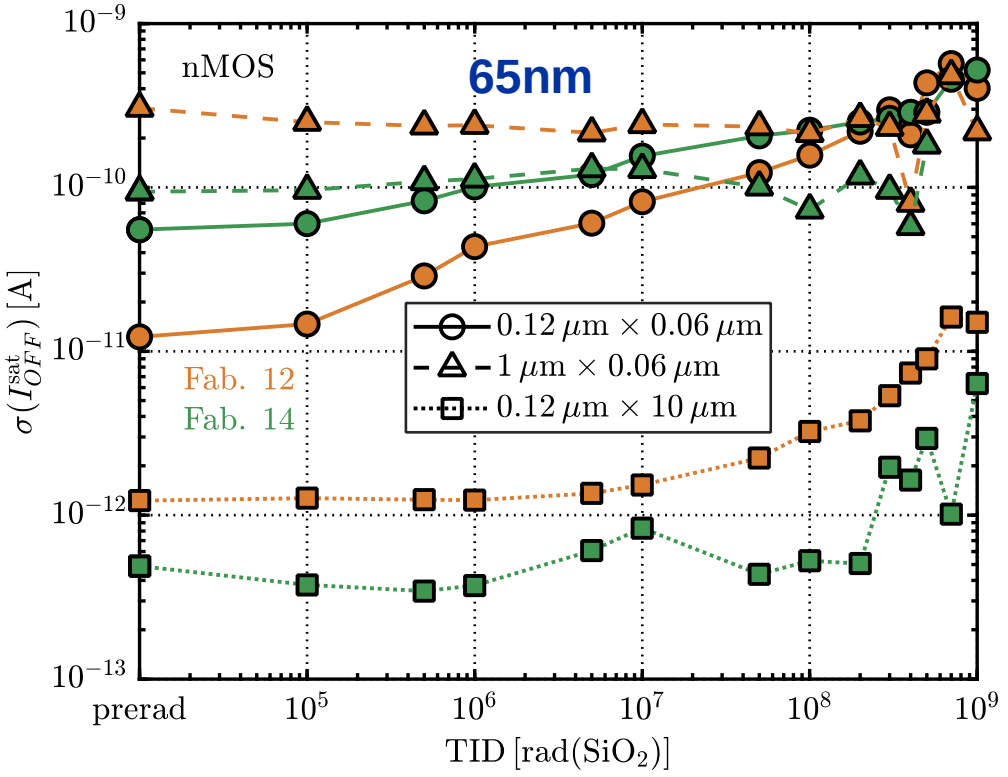
Conclusions

- 130,65nm are affected by fab-to-fab and run-to-run variability
- smaller variability in bigger devices
- accuracy of CERN radiation models depends on transistor's size
- variability may have a strong impact on ASICs performances

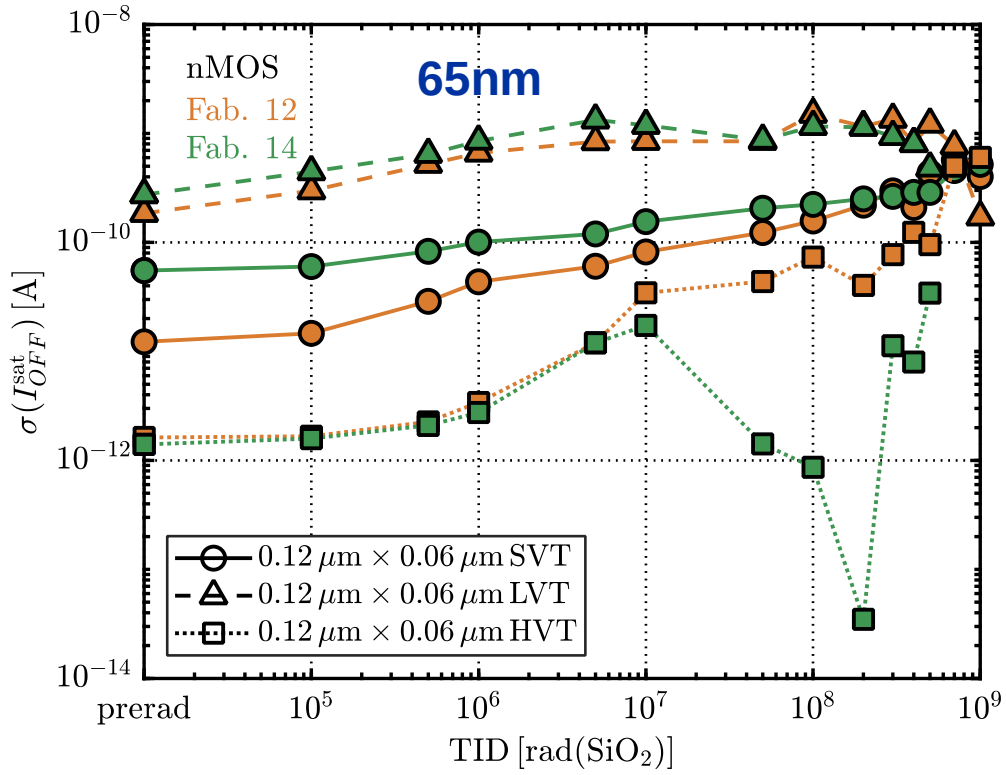
BACKUP SLIDES

$\sigma(I_{OFF})$ ⟶ run-to-run variability

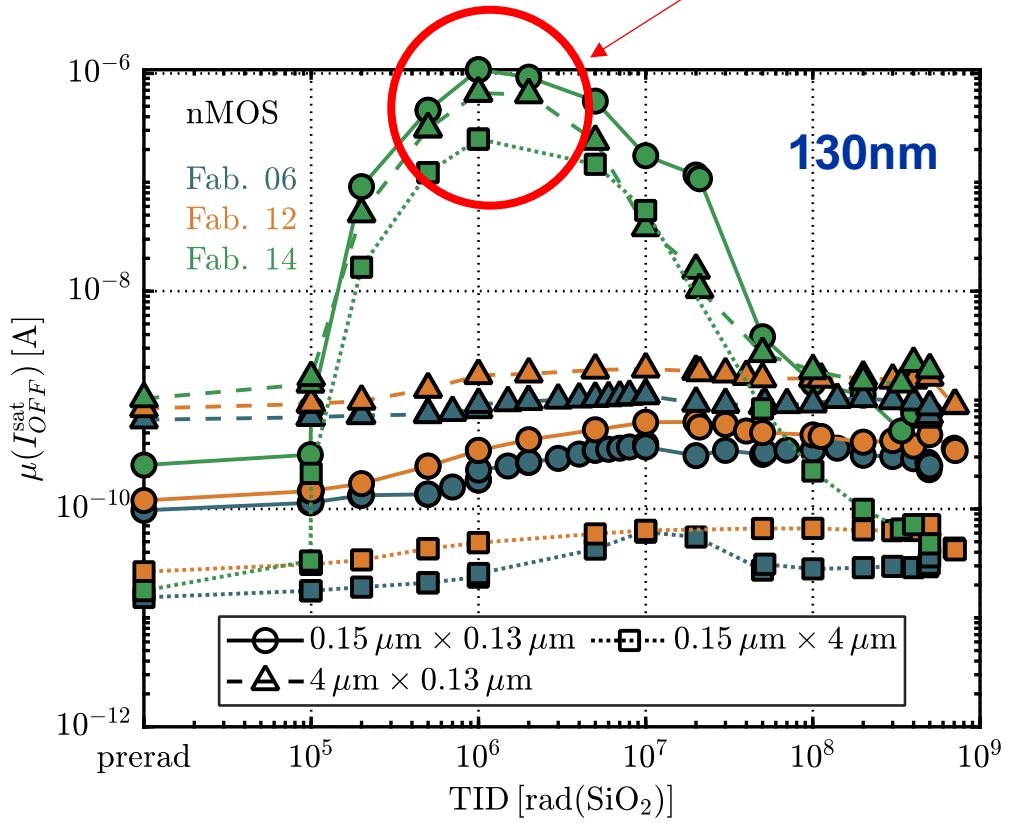


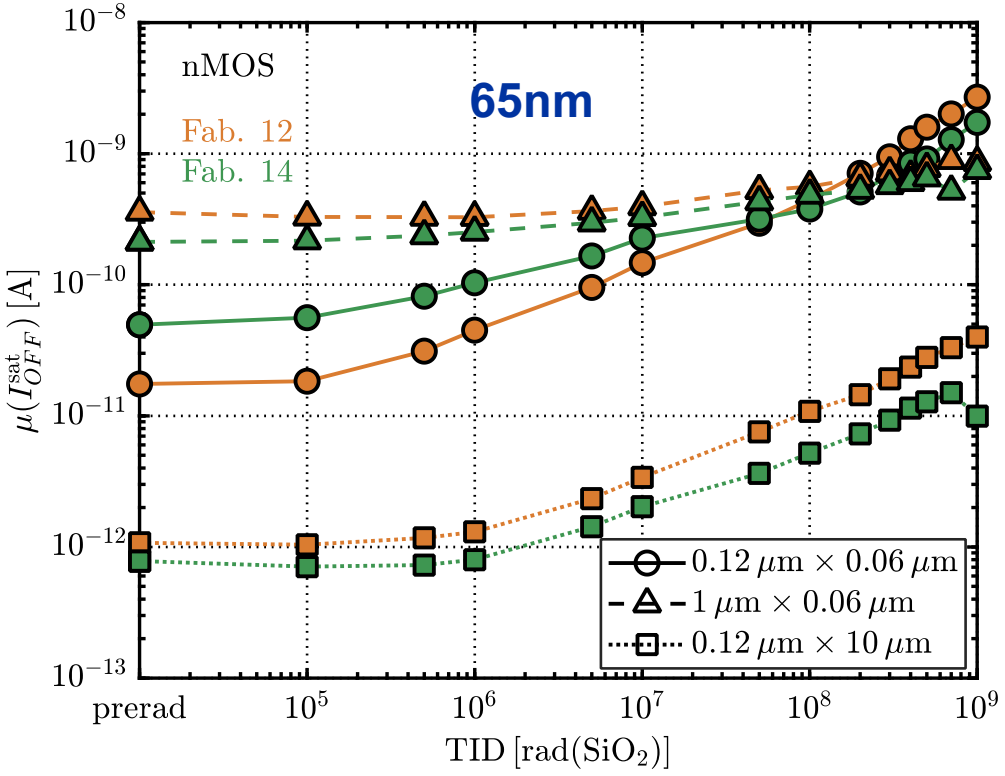


$\sigma(I_{OFF})$ ⟶ run-to-run variability

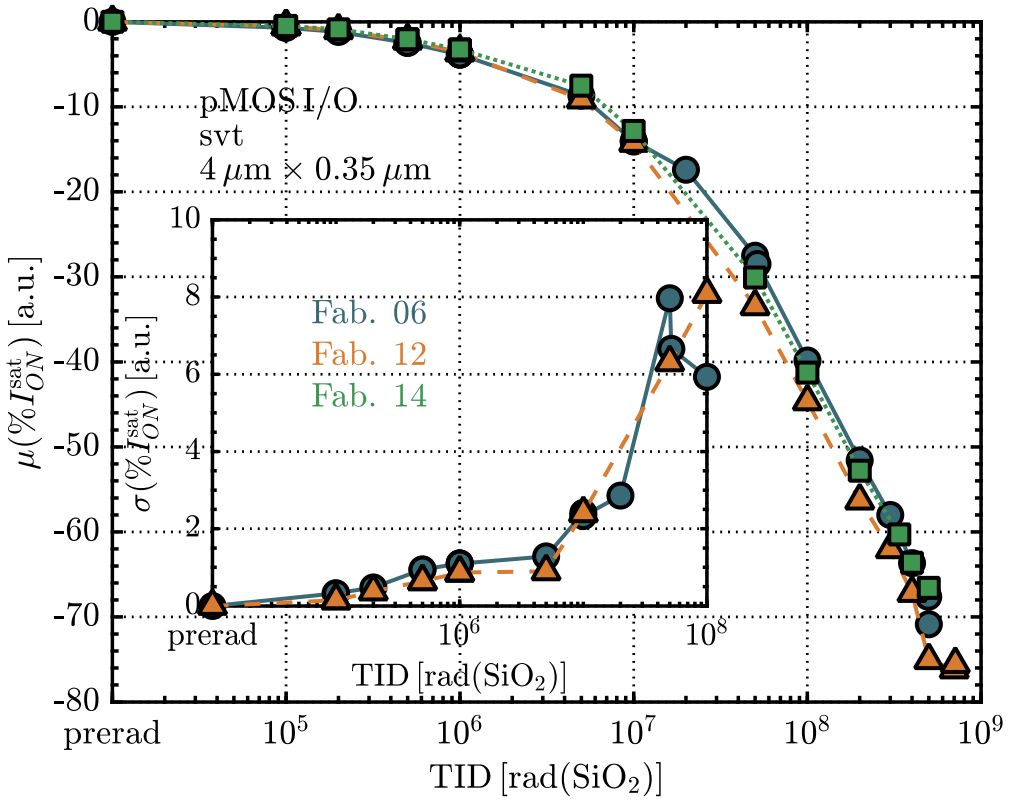


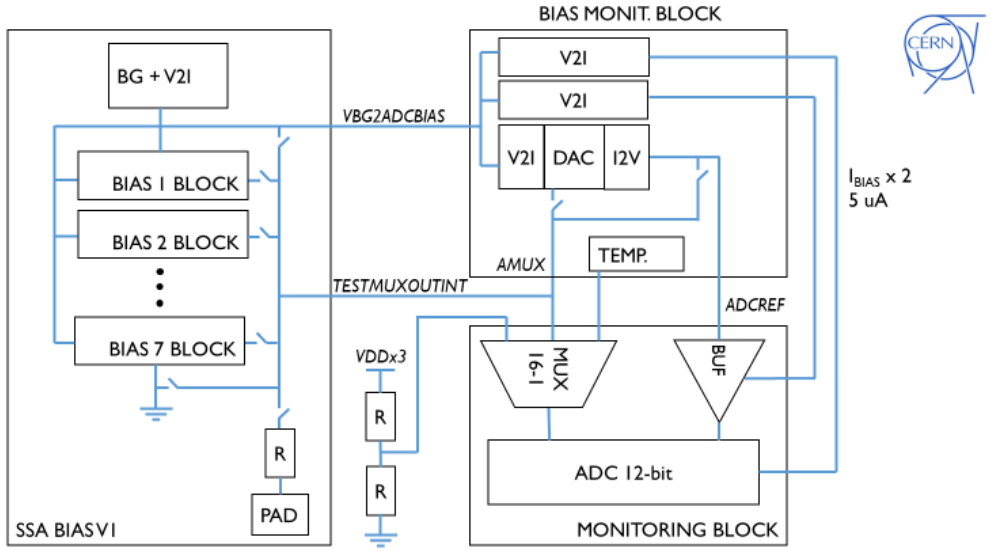
off current increases of
~4 orders of magnitude





I_{OFF} increases monotonically
with TID but no peak


pMOS I/O
svt
4 μm × 0.35 μm
Fab. 06
Fab. 12
Fab. 14
μ(%I_ON^sat) [a.u.]
σ(%I_ON^sat) [a.u.]
TID [rad(SiO2)]
prerad
10^5
10^6
10^7
10^8
10^9
0
-10
-20
-30
-40
-50
-60
-70
-80
10
8
6
4
2


BIAS MONIT. BLOCK
BG + V2I
VBG2ADCBIAS
V2I
V2I
V2I
DAC
I2V
BIAS 1 BLOCK
BIAS 2 BLOCK
BIAS 7 BLOCK
AMUX
TEMP.
TESTMUXOUTINT
ADCREF
VDDx3
MUX 16-1
BUF
R
R
R
PAD
ADC 12-bit
SSA BIASV1
MONITORING BLOCK
I_BIAS x 2
5 uA