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Fab-to-fab and run-to-run variability in 130nm and 65nm CMOS technologies exposed to ultra-high TID

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The discovery of a large fab-to-fab variability in the TID response of the CMOS technologies used in the design of ASICs for the particle detectors of the HL-LHC triggered a monitoring effort to verify the consistency of the CMOS production process over time. As of 2014, 22 chips from 3 different fabs in 130nm CMOS technology and 10 chips from 2 different fabs in 65nm CMOS technology have been irradiated to ultra-high doses, ranging from 100 $\mathrm{Mrad(SiO_2)}$ to 1 $\mathrm{Grad(SiO_2)}$. This unprecedented monitoring effort revealed significant fab-to-fab and run-to-run variability, both dependent on the characteristics of the MOS transistors.

Summary (500 words)

Total Ionizing Dose (TID) effects are a threat for all electronic circuits required to operate in radioactive environments. Among applications where radiation is a concern, the next upgrade of the Large-Hadron-Collider (LHC), the High-Luminosity-LHC (HL-LHC), represents a particularly hostile environment for electronics. It has been estimated that inner layers of the particle detectors of HL-LHC will accumulate a dose of 1 Grad(SiO2) over 10 years of operation. Designing Application Specific Integrated Circuits (ASICs) capable of withstanding these ultra-high radiation levels is an unprecedented challenge that requires a detailed study of the radiation response of the CMOS technologies used in the design of ASICs.
For the chips of the HL-LHC particle detectors, the 130nm CMOS and the 65nm CMOS technologies were selected. The study of the TID effects in these technologies revealed that all radiation-induced degradation phenomena are highly dependent on the manufacturing process. A prime example of this variability is the leakage current of nMOS transistors in 130nm technology. In two of the three facilities (fabs) monitored, TID has a very marginal effect on leakage, while devices produced in the third fab show an increase in leakage current that can exceed 4 orders of magnitude over the value measured before irradiation. The discovery of this extreme fab-to-fab variability mandated constant monitoring of the TID responses of 130nm and 65nm CMOS technologies to verify the consistency of the manufacturing process over time. To that end, technology monitoring chips have been added to each production run of ASICs for particle detectors.

As of 2014, 22 chips from 3 different fabs in 130nm and 10 chips from 2 different fabs in 65nm were measured, some of them in different conditions of temperature and bias. The chips were irradiated to ultra-high doses, ranging from 100 Mrad(SiO2) to 1 Grad(SiO2). This contribution presents the results of this unprecedented monitoring effort.

The relatively large statistics collected over the years will show how the TID response can vary both in devices produced in different fabs and in devices produced in the same fab but in different runs. As an example, the average percentage degradation of the maximum current (ION) of minimum size pMOS transistors in 130nm CMOS technology from the same fab measured at TID=100 Mrad(SiO2) averages at μ(%I_ON)=-30.1% with a standard deviation of σ(%I_ON)=9.1% over 8 chips measured in different runs. Similar results are measured in 65nm technology.

These results raise concerns about the radiation models used to simulate TID-induced degradation in MOS transistors. The radiation corners currently used in the design of ASICs in 65nm for the particle detectors of the HL-LHC have been realized using measurements made in a limited number of chips. In the final paper we will attempt to evaluate the impact of run-to-run variability on the reliability of the radiation models. In addition, it will also be shown how the variability of the radiation response depends on the characteristics

of the transistor such as polarity (nMOS, pMOS), size, threshold voltage (low-vth, high-vth, etc.) and voltage rating (core, I/O).

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