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Single Event Effects Testing and Verification of the RD53 Pixel Chip

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Single Event Effects (SEE) immunity is one of the major challenges that the RD53 chip is required to meet as being the next generation of the pixel readout chips for the High Luminosity LHC upgrade. Extensive proton and heavy ion beam testing was done to examine the overall chip reliability. The critical analog IP blocks are tested with a Two-Photon Absorption laser and gave an in-depth SET sensitivity analysis of the chip analog bottom. Besides the various testing methods, the substantial verification simulation done at the RTL and the gate level was the essential part of the SEU robustness validation.

Summary (500 words)

The RD53 collaboration makes the pixel readout chips for the ATLAS and CMS phase II upgrades. The final ATLAS chip is currently under sign-off verification and testing and will be submitted for production by mid-2022 and followed by the CMS chip submission by the end of the year. In this stage, it is vital to have extensive Single Event Transient (SET) and Single Event Upset (SEU) testing and verification to determine and fix any possible remaining issues. The RD53 pixel chip protects all critical data (configuration memory, state machines, critical event data, look-up tables) against SEEs, but no protection is implemented in trigger latency storage, and event and hit buffering to avoid excessive power consumption and to be inside the area budget. Critical IP blocks (PLL, driver, differential receiver, biasing etc.) are also optimized for SEE immunity. The goal of the SEU simulations is to ensure that the Triple Modular Redundancy (TMR) is implemented correctly and that no critical parts (registers), that should be protected, are overlooked. This is done both at the RTL and the gate level. The paper will cover the concept behind these simulations and the obtained results. Extensive proton and heavy-ion beam testing have measured the effectiveness of the different TMR protections inside the chip, but also fake and corrupted hit rates due to unprotected registers in hit detection and data storage. Test beam testing has also shown that the chip can get into a state of blocked hit readout, while having the command link still functional. A cross-section of this state has been measured in several chip configurations, hit rates, and beam parameters. It has been seen that a fast clear command of data buffers and state machines resolves this and recovers full-chip functionality. The test procedure and the measured cross-sections will be presented. To characterize and improve SET sensitivity of critical analog blocks, a two-photon absorption laser injection system was used. This testing method was very effective in determining and locating sensitive nodes. The testing setup and procedure will be covered in the paper. This found the cause of SET sensitivity of a bandgap reference circuit and lead to a revision of its design. Other blocks such as a Clock and Data Recovery (CDR) and a CML driver showed minor SET sensitivity causing small phase jumps and shifts in the readout link. The effects of these small phase jumps on the readout data are discussed.

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