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Measurements of Total Ionizing Dose Effects and Influence of NMOS Bulk Bias on a CMOS Image Sensor process

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The CERN EP R&D WP 1.2 aims to develop state-of-art monolithic pixel detectors using accessible modern CMOS processes. The TPSCo 65nm process is a suitable candidate and its radiation tolerance and sensor performance are therefore being studied. The impact of the back bias on the transistor behavior has also been measured to provide the designers with accurate models. This process shows sensitivity to radiation and degradation mechanisms similar to previously studied 65nm CMOS technologies, strongly dependent on geometry. In this paper, we offer a qualitative characterization of this node that can serve as a guideline for designers of this technology.

Summary (500 words)

The main objective of the EP R&D Work Package (WP) 1.2 is to develop monolithic CMOS pixel sensors for two principal applications: (i) very high-resolution vertex measurements and (ii) vertex measurements at a high rate and hostile environments at the HL-LHC (High Luminosity). The higher luminosity leads to a maximum expected Total Ionizing Dose (TID) of up to 1 Grad. The move to more advanced nodes with smaller feature sizes should allow for reducing power consumption while increasing the intelligence of the sensor. Moreover, the thinner gate oxide, which comes with the downscaling of the transistor size, increases the tolerance to TID. During phase 1, WP1.2 intends to evaluate different nodes and their performance for radiation tolerance and sensor performance, and the TPSCo 65nm process has become the principal candidate.

Several transistor test structures (TTS) including both pMOS and nMOS have been designed and tested. These TTS include core CMOS devices (rated at 1.2 V), with several threshold voltages (VTH) as well as 3.3 V I/O devices. The TTS contain two arrays of transistors, where either the width or the length varies, allowing to test the radiation response on different transistor dimensions. Another topic of study was the effect of bulk bias on the transistor performance, which is of interest for pixel designs where the nMOS on the pixel matrix are biased with their bulk at voltages down to -6 V. This study aims to analyze the behavior of nMOS transistors at an operating point which is not accurately modelled, as a bias of -6V at the pwell is beyond what is foreseen as a standard way of using the technology. Measurements of nMOS transistors with a pwell biasing of -6 V shows an increase of the nominal VTH of ˜200 mV. For bulk biases down to -1.2 V, the measured VTH matches the simulation. However, this is not the case for a bias of -6 V, where the error concerning the simulation reaches ˜160 mV. This error can lead to a degradation of the analog performance due to improper biasing.

TID tests up to 1 Grad (SiO2) on core 1.2 V devices confirm the reliability of these transistors under irradiation, showing similar radiation response to other 65 nm technologies. Post-irradiation high temperature annealing revealed the presence of two well-known radiation effects: RISCE and RINCE, that affect short and narrow transistors, respectively. These are directly related to the radiation-induced charge trapped on the spacers and the shallow trench isolation oxide (STI). Threshold voltage shifts up to ˜200 mV have been measured. However, fast recovery of the transconductance and VTH after annealing was observed. An increase of radiation-induced leakage current of less than one order of magnitude was detected on nMOS transistors with W > 600 nm.

This paper offers a preliminary characterization of this technology under irradiation and different bulk biases, which will be beneficial for providing designers and detector groups with accurate models to produce circuits that withstand the specifications.

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