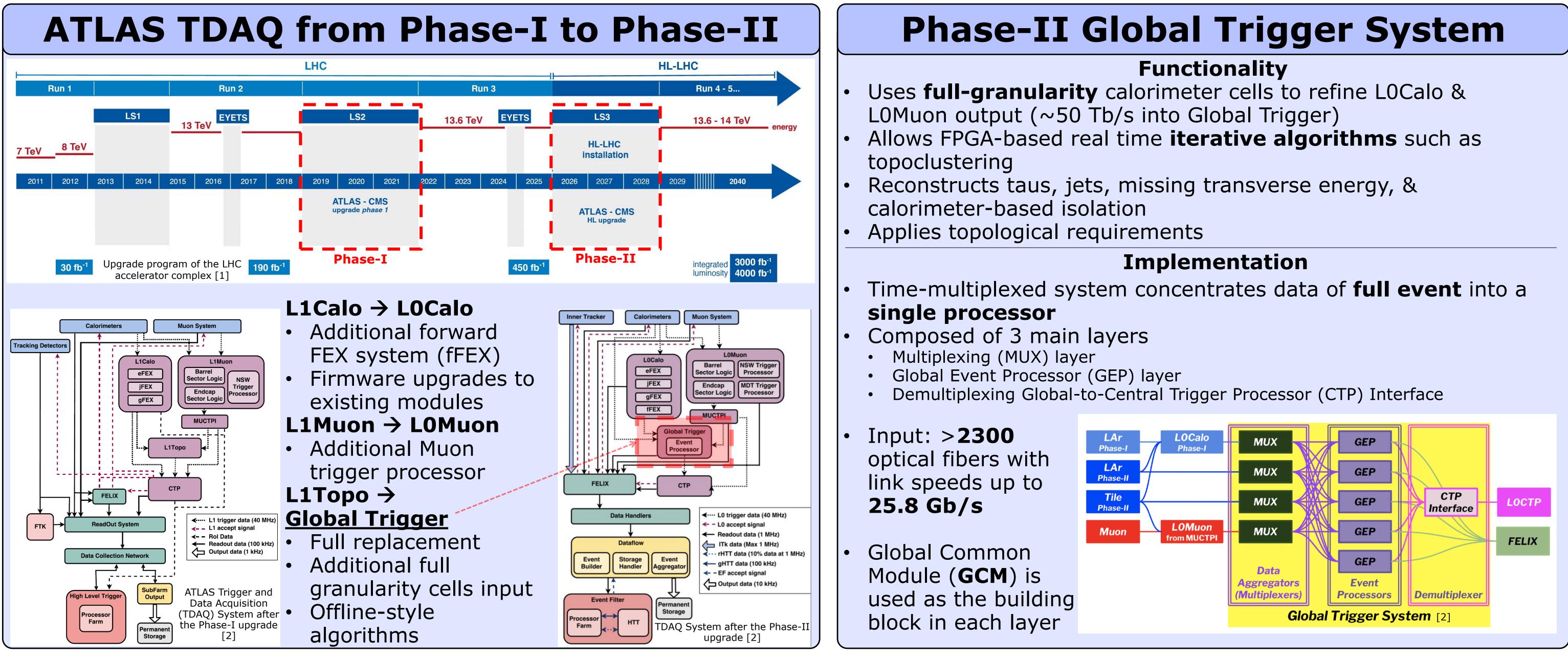


Global Trigger Versatile Module for ATLAS Phase-II upgrade

Experimentelle **Teilchen- und Astroteilchen-**Physik

Viacheslav Filimonov, Bruno Bauss, Volker Büscher, Ulrich Schäfer, Duc Bao Ta TWEPP 2022 Topical Workshop on Electronics for Particle Physics



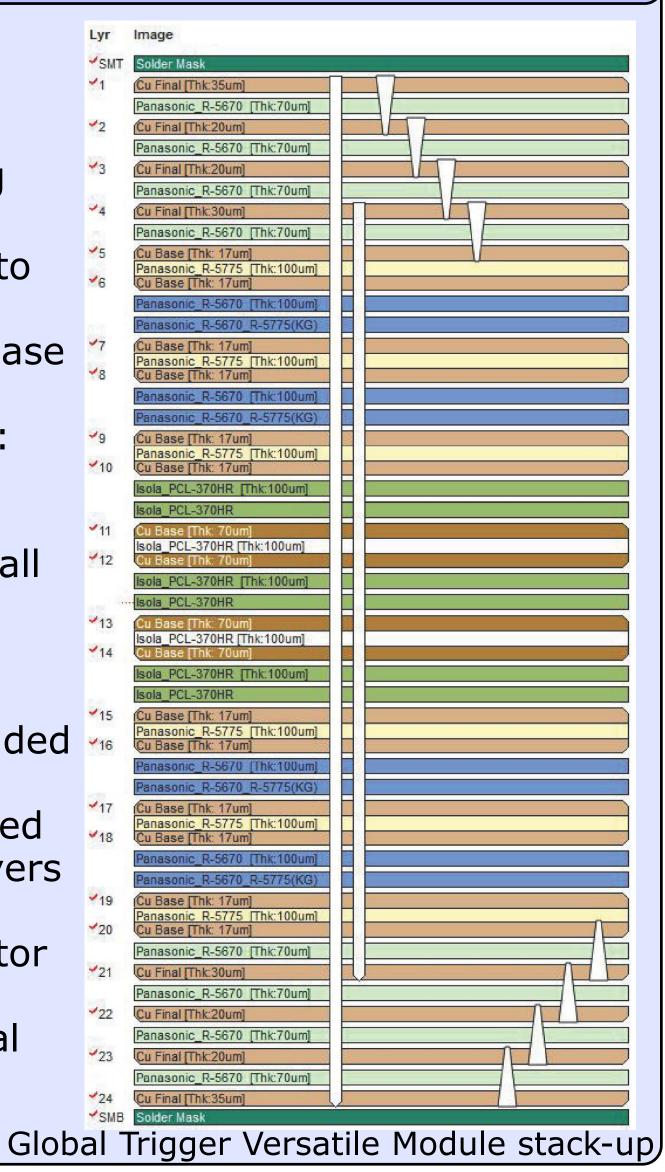
Global Trigger Versatile Module

Key considerations

- An auxiliary hardware component used for development, testing and operational purposes within and beyond the Global Trigger
- Hosts the new generation of optical modules and FPGAs running at high data rates (up to 28 Gb/s) as well as other hardware resources needed for the Global Trigger
- Designed according to the Global Trigger hardware specifications

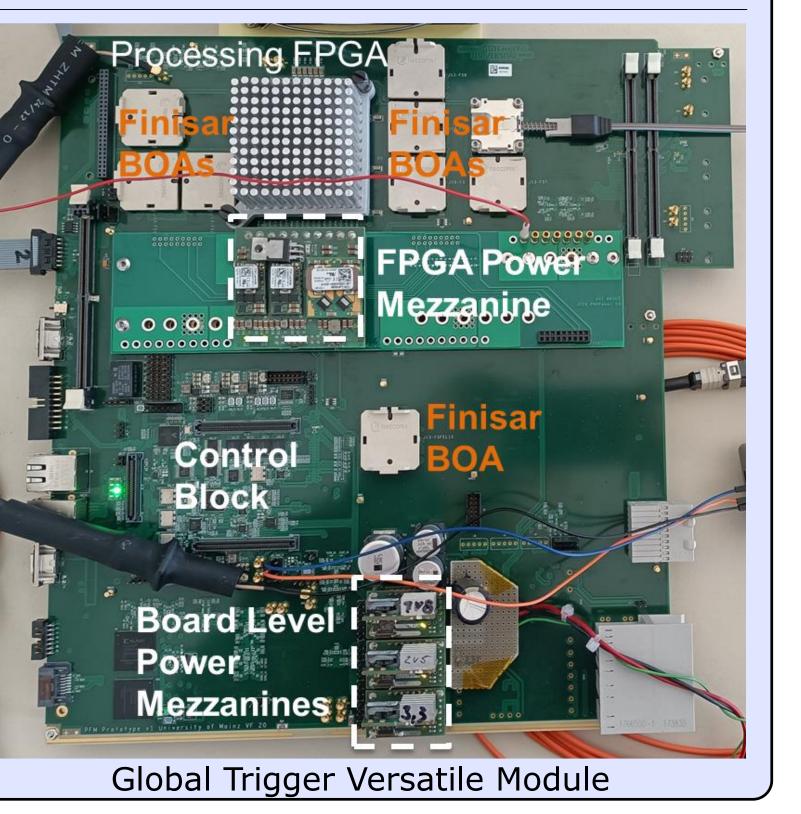
High-Speed PCB Design Considerations

- Optimizing the "high speed" signal integrity
- > Dedicated high-speed PCB design routing techniques
- ✓ All the high-speed differential pairs adhere to strict physical and spacing constraints
- ✓ Staying within the phase tolerance limit: phase tuning performed \checkmark Achieving a required differential impedance: in-pair spacing and trace width controlled ✓ Minimizing the crosstalk: spacing 4 times larger than the in-pair spacing used across all pairs



Hardware overview

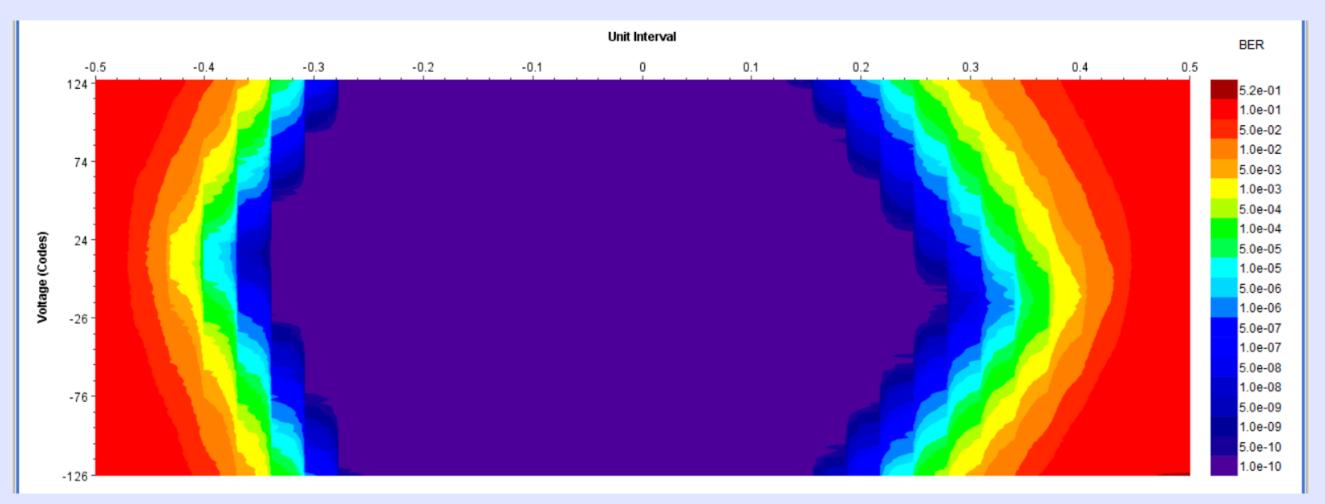
- Designed in a custom **ATCA** form factor
- Standalone operation possible
- Xilinx Virtex **UltraScale+ 13P** FPGA
- 1.7M LUTs, 12K DSPs, 128 MGTs
- 9 Finisar BOA modules
- 218 high-speed tracks
- UltraZed board with **Zynq UltraScale+**
- Control Block
- 2 DDR4 RAMs
- IPM Controller (IPMC)
- Power mezzanines



- > The high speed **stack-up** design
 - Minimizing the crosstalk: signal planes shielded by the ground planes
- ✓ Avoiding stubs on the signal lines: high-speed signals occupy the top and bottom inner layers and use microvias
- ✓ Good dielectric constant and dissipation factor for high frequencies: ultra-low transmission loss and highly "heat resistant" PCB material (MEGTRON6) used

High-speed performance evaluation and current status

- Long-run Integrated Bit Error Ratio Test (IBERT) at 25.78125 Gb/s with a 31-bit PRBS pattern for the high-speed Finisar BOA optical modules and the FPGA
- 12 transmitter links of the optical module were looped back to 12 receiver links of the same module with a help of a "24 to 2x12-fiber" Y-cable and a 12-fiber trunk cable
- All 12 links are functional, and no bit errors detected, measuring the bit error



rate (BER) down to $4.9 \cdot 10^{-15}$

A typical eye diagram, obtained using a low power mode of the GTY receiver, with an open area of 8712, shows a good performance of the Finisar BOA optical module

Finisar BOA IBERT loopback test: a typical eye diagram

- A Global Trigger Versatile Module designed according to the Global Trigger hardware specifications Performance of the high-speed optical modules and the FPGA successfully evaluated with long-run link tests
- The Global Trigger Versatile Module plays an important role in the firmware development for the Global trigger system
- Currently provides a development platform for a Topoclustering algorithm integrated into a Global Trigger firmware framework
- Advanced hardware resources and adherence to the Global Trigger hardware specifications make the Global Trigger Versatile Module a valuable hardware component that can be used for development, testing and operational purposes within and beyond the Global Trigger in projects requiring high bandwidth and processing capabilities



http://www.etap.physik.uni-mainz.de/atlas

http://atlas.ch

LHC / HL-LHC Plan (last update February 2022), https://hilumilhc.web.cern.ch/content/hl-lhc-project
ATLAS Collaboration, "Technical Design Report for the Phase II Upgrade of the ATLAS TDAQ System", CERN-LHCC-2017-020.

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