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Global Trigger Versatile Module for ATLAS Phase-II upgrade

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ATLAS detector Phase-II upgrade for the High Luminosity Large Hadron Collider (HL-LHC) affects all major ATLAS systems including the Trigger and Data Acquisition. As part of the Level-0 Trigger System, the Global Trigger uses the most advanced FPGAs and optical modules to provide high input and output bandwidth and substantial processing power. The Global Trigger Versatile Module (GVM) hosts the new generation of optical modules and FPGAs running at high data rates and other hardware resources needed for the Global Trigger, acting as an auxiliary hardware component used for development, testing and operational purposes within and beyond the Global Trigger.

Summary (500 words)

ATLAS detector at the Large Hadron Collider (LHC) will undergo a major Phase-II upgrade for the High Luminosity LHC (HL-LHC). The upgrade affects all the main ATLAS systems including the Trigger and Data Acquisition.

As part of the Level-0 Trigger System, the Global Trigger uses full-granularity calorimeter cells to perform algorithms, refines the L0Calo trigger objects and applies topological requirements.

A building block of the Global Trigger is the Global Common Module (GCM), which has to provide significant processing resources along with a high input and output bandwidth. Various link speeds, including high-speed links up to 28 Gb/s, should be supported. The high-speed link support is essential in order to cope with the transmission of high-granularity calorimeter data which drives the bandwidth requirement for the upgraded TDAQ system.

An additional Global Trigger Versatile Module (GVM) has been designed according to the Global Trigger hardware specifications. The GVM hosts the new generation of optical modules and FPGAs running at high data rates (up to 28 Gb/s) as well as other hardware resources needed for the Global Trigger and acts as an auxiliary hardware component that can be used for development, testing and operational purposes within and beyond the Global Trigger.

The GVM is designed in an ATCA form factor with the possibility of a standalone operation. The main building blocks are the following: one large processing FPGA (Xilinx Ultrascale+ VU13P), up to eight Finisar BOA modules for real-time data path, one Finisar BOA module for interface to Front-End Link eXchange (FELIX) system, one UltraZed board with Zynq UltraScale+, one IPM Controller (IPMC), one FPGA power mezzanine and two DDR4 RAMs. Dedicated clock distribution circuits are implemented as well in order to provide reference clocks for the multi-gigabit transceivers of the FPGA.

In order to optimize the signal integrity for the high-speed signals between the FPGA and optical modules as well as other high-speed components, dedicated high-speed PCB design techniques were used. Thus, all the high-speed differential pairs adhere to strict physical and spacing constraints. Phase tuning is performed. Appropriate in-pair spacing and trace width provide the required differential impedance, while sufficient spacing across all pairs minimizes the crosstalk.

Moreover, the stack-up is designed in such a way as to provide good signal integrity for high-speed signals. Signal planes are shielded by the ground planes, thus minimizing the crosstalk. High-speed signals occupy the top and bottom inner layers, and use microvias in order to avoid stubs on the signal lines.

Ultra-low transmission loss and highly heat resistant PCB material (MEGTRON6) is used for the PCB due to its good dielectric constant and dissipation factor for high frequencies.

The main hardware functionality of the module including power, clock trees, JTAG chain, main processing FPGA and control block has been verified. Performance of the high-speed optical modules and the FPGA has been evaluated with long-run link tests.

Successful results demonstrating a good performance of the on-board components have been obtained. The presentation will provide a hardware overview and measurement results of the GVM.

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