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Irradiation testing of ASICs for the ATLAS HL-LHC Upgrade

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For the high luminosity upgrade to the LHC, the ATLAS inner detector will be replaced by an all-silicon tracker (ITk) consisting of two systems: pixels and strips. The HCCStar and AMACStar are ITk strips ASICs vital for performing the system readout, and monitoring and control.To ensure these ASICs will successfully operate in the high-radiation environment of the HL-LHC, these ASICs need to be tested for radiation tolerance, and this has been tested using both heavy ions and protons. The ASIC designs were shown to be protected against radiation related effects.

Summary (500 words)

The HCCStar and AMACStar are ASICs on the ITk strips for the HL-LHC. Since these ASICs will be used in a high radiation environment, we need to make sure these chips function properly when high energy particles pass through them. When high energy particles pass through materials, they can ionize the material and leave behind electron-hole pairs, which can cause logic states to flip in the configuration registers or in the data as it is being processed. Radiation can also create short voltage pulses on wires. The ASIC designs use voted triplication of registers, deglitchers on wires, and encoding of states and signals to protect against single event effects (SEEs). SEEs occur more frequently as linear energy transfer (LET) increases, so testing with ions with different LETs can help us make predictions for future scenarios.

We tested the HCC and AMAC using heavy ions at UCLouvain on a cold plate inside a vacuum chamber. We used 8 ions for each chip ranging in LET from 1.3 to 62.5 MeV*cmˆ2/mg. The average fluence was 5.5E7 ions/cmˆ2, with the amount of beam time for each ion adjusted based on LET.

Both chips performed extremely well operationally. Multiple SEEs occurred in the configuration registers during the different ion beam runs, and they were automatically corrected by the ASICs voted-triplication mechanism. For the lightest LET, we saw fewer than 10 corrected bit flips for both chips. For the ions tested with LETs of 5.7 and higher, we saw on the order of 1000 corrected bit flips for each chip. For the three highest-LET ions, instances of non-corrected SEEs were unsurprisingly observed for the HCC. AMAC experienced communication issues for the highest LETs, but control of the ASIC was recovered with communication resets. The cross-sections were measured for each chip, and system resets were shown to quickly recover operation. These are likely caused by large amounts of deposited charge across a larger area of the chip, and their extremely rare expected rate can be calculated for the HL-LHC.

Using the calculated cross-sections, we produced Weibull curves for each chip, which allows us to calculate the rate of SEEs expected at the HL-LHC. These results are relevant to both the ASIC track and the Radiation Tolerant Component and Systems track. By the time of the conference, we will have performed proton irradiation at TRIUMF, so those results would be included as well. Proton irradiation will give us a higher fluence of high energy protons, which can create high LET ions through nuclear interactions within the chip. Because this is similar to what will happen in HL-LHC conditions, this test is important to further validate the ASIC designs. Figures showing rates and results will be prepared and shown in the poster after a standard approval process by the ATLAS collaboration.

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