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Performance evaluation of the prototype pixel readout chip (CROCv1) for the CMS Inner Tracker Upgrade

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Following the RD53A demonstrator, the ItkPix (ATLAS) and CROC (CMS) pixel readout chips are being developed within the RD53 collaboration for the HL-LHC pixel detector upgrades of the two experiments. The two chips are based on a common design, called RD53B, in 65nm CMOS technology and are optimized for very high rate (3GHz/cm2) and radiation levels (>500Mrad). The CMS pre-production chip CROCv1 was submitted in June 2021 and an extensive characterization campaign has been running since its arrival in October 2021. This contribution gives a general overview of the chip architecture and discusses the characterization and testing of CROCv1.

Summary (500 words)

The High Luminosity Large Hadron Collider (HL-LHC), starting its operation in 2029, will constitute a new frontier for particle physics. Major experimental challenge resides in the design of the inner tracking detectors: the harsh environment in the innermost layers of the detectors is setting stringent requirements on the pixel chip design. The readout chip has to be capable to cope with high hit rates of 3 GHz/cm2 and trigger rates of 1 MHz in combination with a trigger latency of 12.5 us. A very high radiation tolerance of over 500 Mrad and 2x10^16 neq/cm2 is required as well as the support for a serial powering scheme of the pixel modules. The new generation pixel readout chips that will have to meet these challenging specifications, are designed by the RD53 collaboration, which is a joint effort between ATLAS and CMS.

Following the RD53A demonstrator chip, the next generation of RD53 chips, called RD53B, are designed as full-sized pre-production chips and incorporate the production requirements defined by the experiments. There are two experiment specific versions of RD53B: the ATLAS version, called ItkPixV1 and the CMS version, called CROCv1. The two chips are two separate instances of the common RD53B design framework. The main difference between them is the pixel matrix size and the pixel analog front end. There are other differences partly stemming for the sequential fabrication: RD53B-ATLAS in 2020 and RD53B-CMS in 2021.

The RD53B generation is designed in 65nm CMOS technology and features 50um x 50um sized pixels. Among the many added features with respect to the RD53A chip are data-merging between neighboring chips, data compression to reduce the data rate by a factor of 2 and a self-trigger capability. The critical IP blocks of PLL/CDR and the Shunt-LDO power regulator circuits have improved greatly allowing for a reliable operation. Protection features against overvoltage and overload have been added together with an optional low-power mode. To mitigate Single Event Effects (SEE) a Triple Modular Redundancy (TMR) strategy was adopted including self-correction and a triplicated clock tree with skew for critical parts.

The CMS pre-production chip CROCv1 was submitted in June 2021 and incorporates bug fixes and few additional monitoring and diagnostic features relative to ItkPixV1.

An extensive characterization campaign has been running since, based on a versatile DAQ system which is comprised of firmware, software and hardware layers, developed to support characterization, production and integration tests of the upgraded CMS Tracker. The CROCv1 characterization campaign includes validation, evaluation and benchmarking of the performance of the main building blocks and the newly introduced features of the chip at single chip level, wafer level as well as at pixel module level. The performance of the chip

was evaluated over different corners covering temperature, irradiation and powering conditions.
In this contribution, a general overview of the chip architecture and the measurement setups will be introduced followed by the results from the characterization campaign of CROCv1 including bugs and improvements that were proposed for the final chip submission planned for end of 2022.

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