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Analog performance of the CROC-V1 pixel readout chip for the CMS Phase-2 Tracker Upgrade

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The CROC-V1 readout front-end (FE) chip was designed by the RD53 collaboration for the CMS Phase-2 Inner Tracker Upgrade. It is designed to cope with the extreme radiation and hit rates of the HL-LHC and it is based on the 65 nm CMOS technology and a novel analog FE design featuring linear charge to Time-over-Threshold (ToT) conversion. In this contribution, the characterization measurements of the analog part of the chip are presented with a special focus on the linear analog FE, including Total Ionizing Dose (TID) radiation damage studies.

Summary (500 words)

The High Luminosity Large Hadron Collider (HL-LHC) project aims to increase the integrated luminosity by a factor of 10 beyond the LHC's design value, thus placing challenging requirements on the performance of the detectors. The readout electronics of the CMS Inner Tracker, located at the innermost layer of the detector, must be able to operate at hit rates of 3 GHz/cm2 and trigger rates of 1 MHz under extreme radiation conditions with fluences of up to 2x10ˆ16 neq/cm2 and resist a TID larger than 500 Mrad. The RD53 collaboration is a joint effort between ATLAS and CMS to design readout chips based on 65 nm CMOS technology to meet the requirements of HL-LHC.

The RD53A readout chip, submitted in 2017, was the demonstrator chip designed by the RD53 collaboration featuring a 192 x 400 matrix of 50 um x 50 um pixels split into three regions, each with a distinct analog FE design. After extensive testing, the design of RD53A was evolved and led to the next generation of pre-production chips, ITkPix-v1 for ATLAS and CROC-v1 for CMS, collectively known as RD53B, with final size pixel matrices (384 x 400 and 336 x 432 respectively). RD53B chips introduced new features in many areas such as event encoding, data transmission, monitoring and diagnostics while also incorporating various bug fixes.

The CROC-v1 was submitted in June 2021 and improves upon the Linear FE design. The Linear FE design consists of a charge sensitive amplifier feeding a low noise comparator. The ToT of the amplifier's response is measured to estimate the input charge. The FE can receive charge either from a sensor or from a special injection circuit which is being used to tune various parameters of the front-end.

A dedicated DAQ system consisting of hardware, firmware and software components, has been developed to enable the operation and testing of RD53 chips. It is being used in the characterization campaign of the CROC-v1 to evaluate, validate and benchmark the performance of the chip in various configurations such as single-chip cards, multi-chip modules and wafer probing.

During the ongoing characterization campaign, the Linear AFE has shown promising results. It is able to reach low thresholds with a high signal to noise ratio, a low threshold dispersion among different pixels and a less pronounced time-walk effect compared to RD53A. More specifically, most of the tested samples were able to reach thresholds lower than 1000 electrons with a threshold dispersion of 70 electrons or fewer and a percentage of noisy pixels lower than 1%. Multiple irradiation campaigns, using x-ray and gamma-ray sources, were able to validate the performance of the FE after a TID of up to 1 Grad.

This contribution will focus on the characterization of the Analog FE of CROC-v1 and will present results of various tests including irradiation tests and first test beam results.

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