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RD53 pixel chips for ATLAS and CMS

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RD53 Collaboration is a joint effort between ATLAS and CMS that was established in 2013, and extended in 2018, to develop readout chips for the HL-LHC pixel detectors in 65nm technology.
Main operational constraints for the readout electronics are: the extremely harsh radiation environment (1 Grad), high hit (3GHz/cm2) and Trigger rates (4 MHz), high data rate readout (5 Gb/s).
This work will describe all architectural choices that have been performed in order to cope with these extreme operating conditions.
Measurements results showing that ATLAS and CMS experiment specifications are met will be presented.

Summary (500 words)

With the planned upgrade for the Large Hadron Collider (LHC) at CERN also sub-detectors of both ATLAS and CMS will be upgraded in order to be able to cope with these extremely harsh environment.
The new pixel detector of both experiments will have silicon sensors with a pitch of 50 um x 50 um and 100 um x 25 um.
In order to develop the readout chips of both experiments the RD53 collaboration was established in 2013, to be able to aggregate enough people to overcome the challenges posed by this project.
A first full scale prototype chip was fabricated in Aug. 2017 that allowed the community to verify the basic architectural choices and the final version of the Analog Front-End circuit.
This submission was followed in Mar. 2020 and Jun. 2021 by the pre-production version of the ATLAS and CMS chips.
These chips are now heavily under test and have so far shown that all ATLAS and CMS experiment specifications are met.
The collaboration is currently finalizing the production version of both chips which will be submitted by the end of the year.
This work will mainly focus on architectural choices and developments that have been made in order to cope with system requirements.
These chips have to be able to operate in an extremely harsh radiation environment (1 Grad) with very high hit (3 GHz/cm2) and Trigger rates (4 MHz) and a high data rate readout (5 Gb/s).
Both ATLAS and CMS will adopt a serial powering scheme that relies on two on-chip ShuntLDO regulators that generate all needed on-chip voltages using a constant current input.
In order to be able to operate the chip a novel input protocol was developed. This protocol, which runs at 160Mb/s, allows the chip to fully operate using a single LVDS input line that provides configuration and data. It allows the chip to be continuously reconfigured, in order to minimize unavoidable SEU/SET effects, while being able to accept Trigger commands.
Internally there is a CDR/PLL circuitry to generate all needed on-chip clocks and data from the input data line.
Hits arriving from the sensor to the pixels are stored internally using a 4-bit ToT mechanism and read out upon Trigger arrival.

Triggered hits are compressed and merged forming single/multiple events that are then readout via up to four serial links that use the Aurora64/66 protocol and allow a total output bandwidth of 5.12Gb/s.
Multi-chip data merging, allowing to merge data coming from four different chips, is built in in order to minimize the number of optical links needed to read out the outer pixel layers of the
detector.
Measurements of the main implemented features will be presented to show that pre-production chips meet desired specifications of both experiments.

Author: BECCHERLE, Roberto (INFN, Pisa (IT))

Presenter: BECCHERLE, Roberto (INFN, Pisa (IT))

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