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Design of an analog monolithic pixel sensor prototype in TPSCo 65 nm ISC CMOS imaging technology

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A series of monolithic active pixel sensor prototypes were manufactured in the TPSCo 65 nm ISC imaging process in the framework of the CERN-EP R&D on monolithic sensors and the ALICE ITS3 upgrade project. Each APTS chip contains a 4x4 pixel matrix with fast analog outputs buffered to individual pads. To explore the process and sensor characteristics, various pixel sizes (10um - 25um), geometries and reverse biasing schemes were included. Prototypes are fully functional with detailed sensor characterization ongoing. The design will be presented with some experimental results also correlating to some transistor measurements.

Summary (500 words)

Monolithic active pixel sensors (MAPS) receive more and more interest for tracking detectors in high energy physics, and have shown significant progress in recent years. They are fabricated in commercial CMOS technology, normally with some process modifications optimized for sensor performance, offering advantages of detector capacitance, material budget, assembling effort and total cost comparing to conventional hybrid structures. Similar to commercial ASICs, the process feature size tends to decrease to improve timing and spatial detection resolution, readout and computing speed and power consumption in high energy physics applications.

A series of monolithic sensor prototypes have been fabricated in the TowerJazz Panasonic Semiconductor 65nm CMOS Image Sensor Process (TPS65ISC) in the framework of the CERN-EP R\&D on monolithic sensors (Work package 1.2) to explore this technology as a potential candidate for future high energy physics detectors and related applications, and in particular for the ALICE ITS3 upgrade. The Analog Pixel Test Structure or APTS contains a small 4x4 pixel matrix with very fast (rise and fall times of a few 100 ps) analog outputs directly buffered to output pads for off-chip real-time observation of all pixels in parallel. The primary aim is to explore this process and characterize sensor performance with process modifications. Prototypes are proven fully functional with detailed sensor characterization ongoing. This paper will mainly focus on the design of APTS.

The APTS measures 1.5 x 1.5 mm2. In the first submission in this technology 35 different APTS variants were implemented with varying pixel size (10um - 25um), sensor geometry and reverse biasing scheme. In general the fast buffer chain is composed of four source followers, but in some chips the two source followers in the matrix periphery are replaced by a high speed operational amplifier circuit capable of driving a 50 ohm load to allow signal termination on board or on the scope and maximize speed capability to characterize charge collection time.

Source followers are commonly used in conventional MAPS readout to compensate part of the parasitic capacitance on the input node, and therefore increase conversion gain or the voltage excursion of the output signal per electron charge collected by the sensor. Reverse sensor bias further helps to reduce the sensor capacitance due to an increased depletion around the collection electrode. However, increasing reverse substrate bias also significantly affects the operating point through the bulk effect on the transistors, in particular the input transistor of the NMOS follower within the pixel matrix of which the source cannot be connected to its substrate. This effect appears to be underestimated in the simulation for significant reverse substrate bias outside of

the standard supply voltage, and this is now further being studied by correlating back to measurements of individual transistors.

APTS features various pixel flavors and fast analog readout, designed to optimize the pixel sensor performance and now allows an in-depth study of the charge collection properties and the effect of reverse bias and other parameters. Its design will be presented with some experimental results and correlation to transistor measurements.

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