Bandgap Reference, Temperature Sensor and Low Drop-out Regulator Circuits for Monolithic Sensors in TPSCo 65 nm Technology

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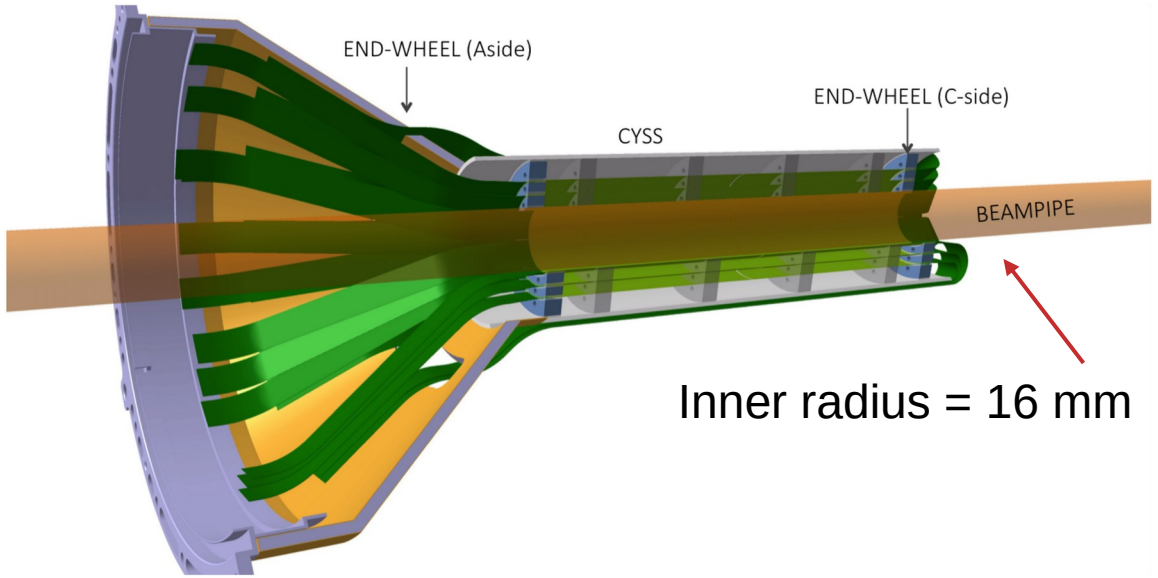
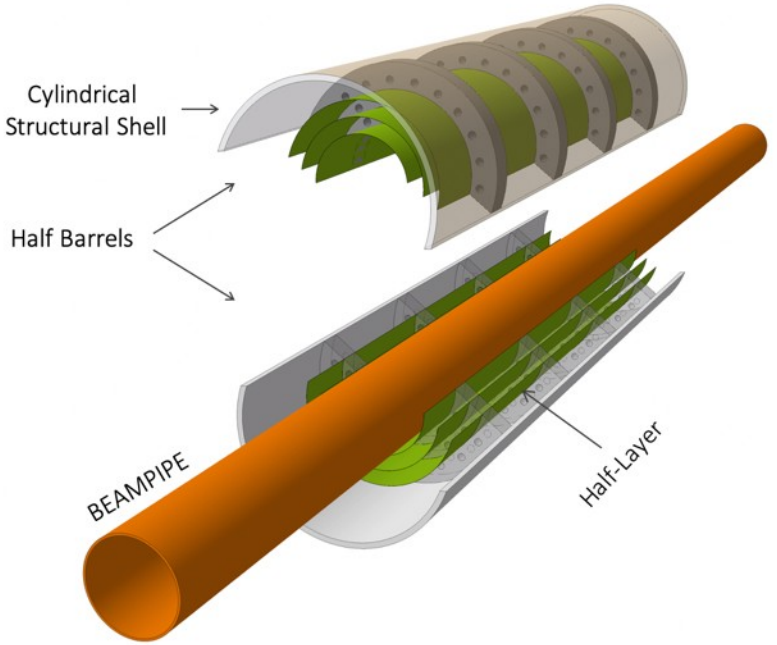
ALICE ITS3 Upgrade





- Wafer-scaled monolithic stitched sensors
- Very low material budget ⟹ Improved tracking precision
- Low power consumption (no active cooling)
- Operation temperature is at 20 ºC

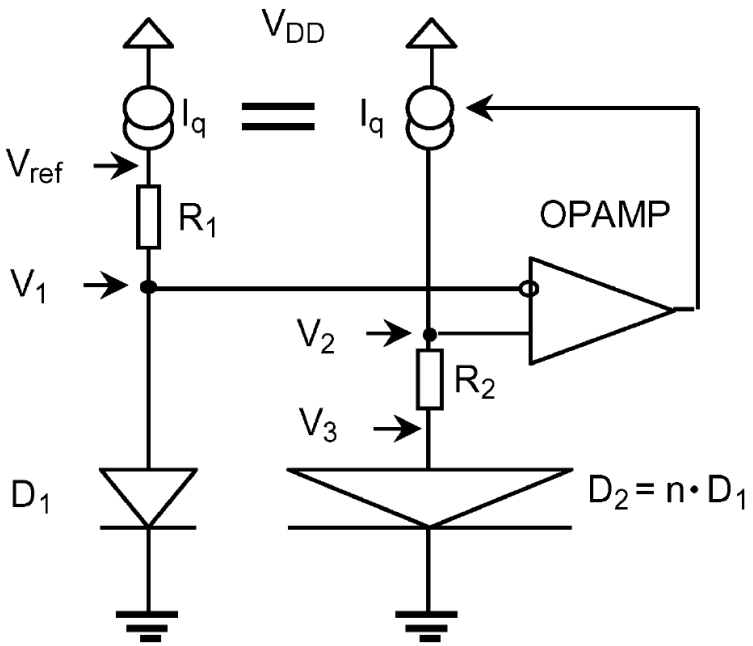
Outline

- Bandgap Reference (BGR) (Submitted and measured within TPSCo MLR1)
- Temperature Sensor (TS) (Submitted and measured within TPSCo MLR1)
- Low Drop-Out Regulator (LDO) (Submitted within TPSCo ER1)
- Conclusion

Bandgap Reference (BGR) Circuit

- Bandgap Reference (BGR) circuits provide **reference voltage (V_{ref})** which is ideally **insensitive** to **variations** of
  - **Process**
  - **Temperature**
  - **Power supply**
- Additionally, BGR circuit must be **tolerant** to **Total Ionizing Dose** (TID).

- **BGR**
- TS
- LDO
- Conclusion



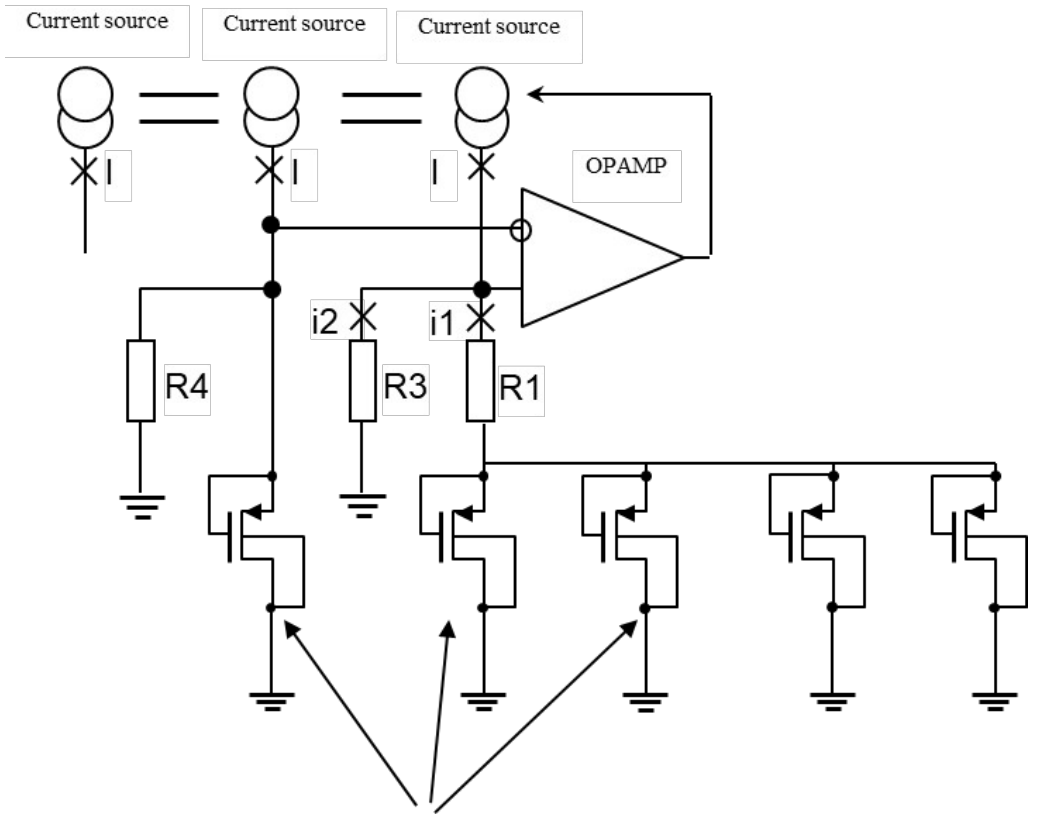
BGR featuring **conventional diodes** relies on forward-biased p-n junction.

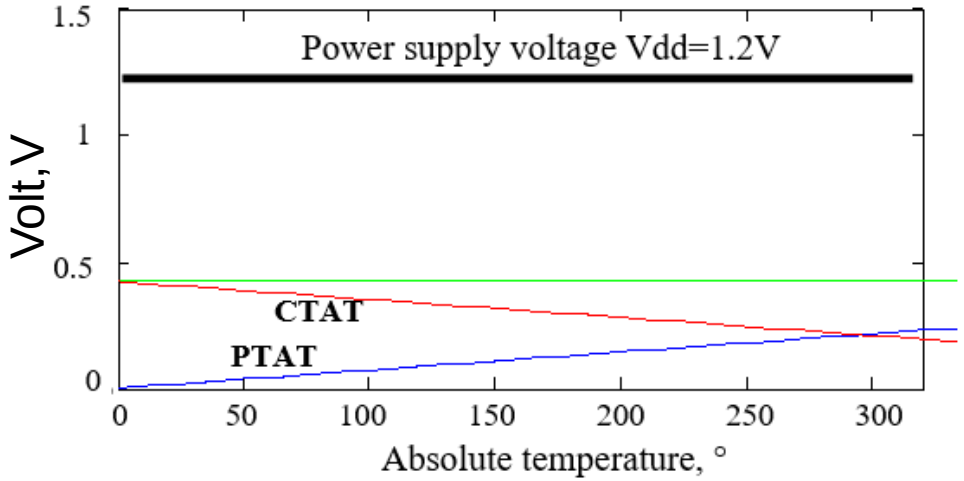
× Low power supply ⟹ Complication of design (V_{ref} ≈ 1.22V)

× Conventional diodes are **vulnerable** to **TID effect**.

Implemented BGR Circuit

- **BGR**
- TS
- LDO
- Conclusion



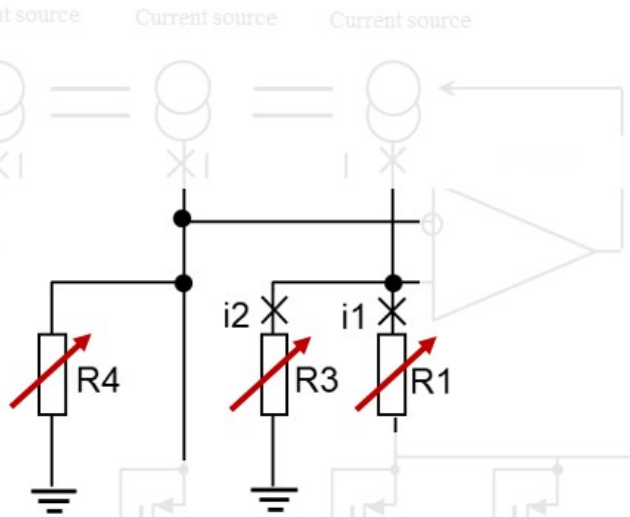


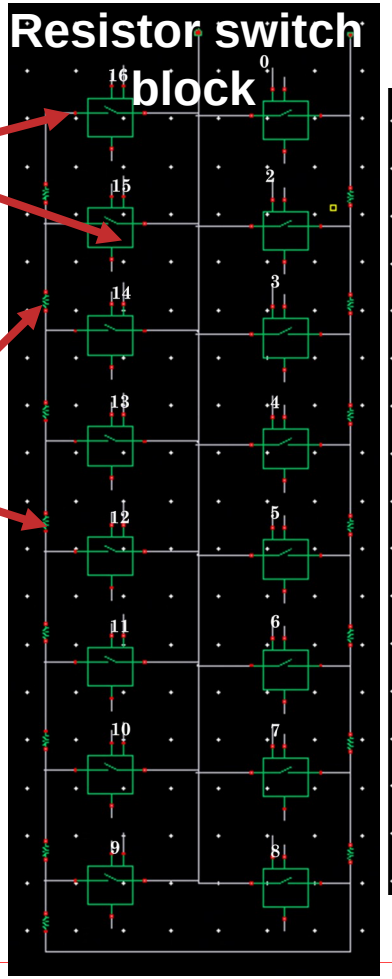
Reference elements: Diode, BJT, gated-diode, DTMOST

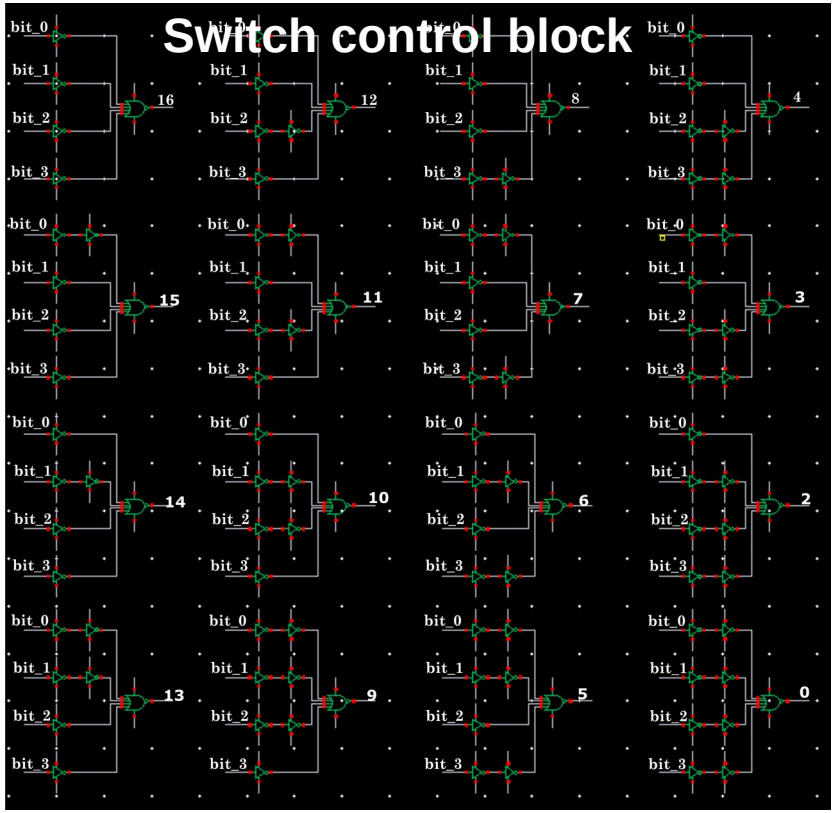
- Resistors R1, R3, and R4 can be **controlled** for **different process variations**.

Implemented BGR Circuit (2)

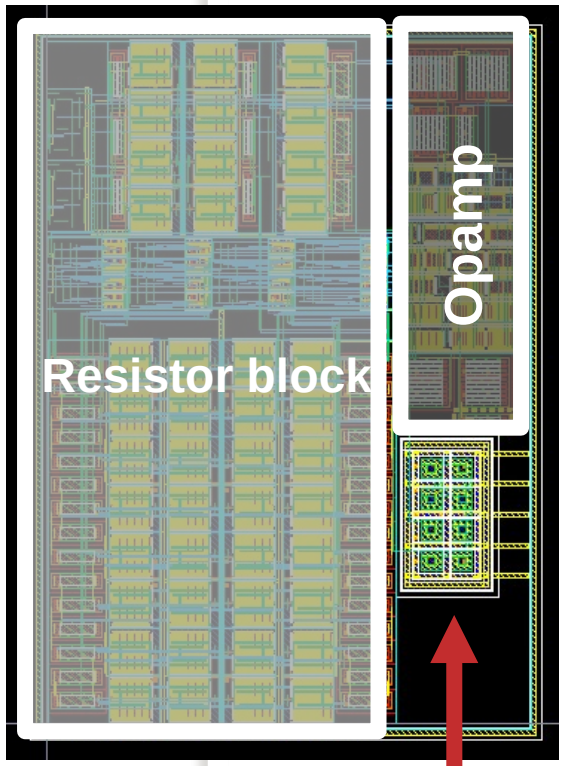
- **BGR**
- TS
- LDO
- Conclusion



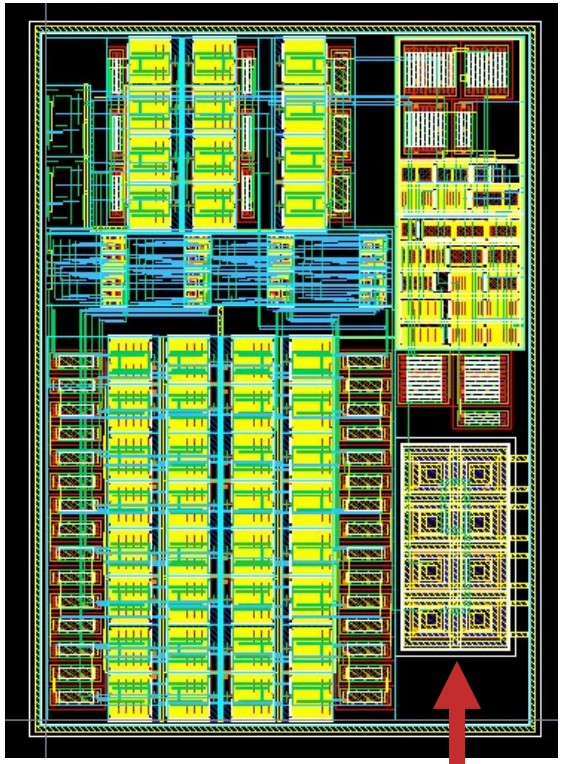




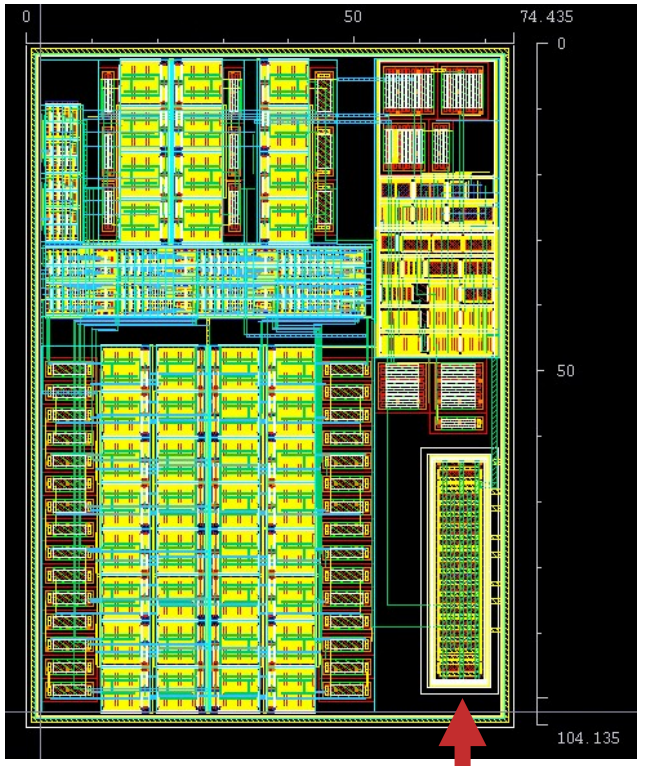
Layouts of Implemented BGR Circuits



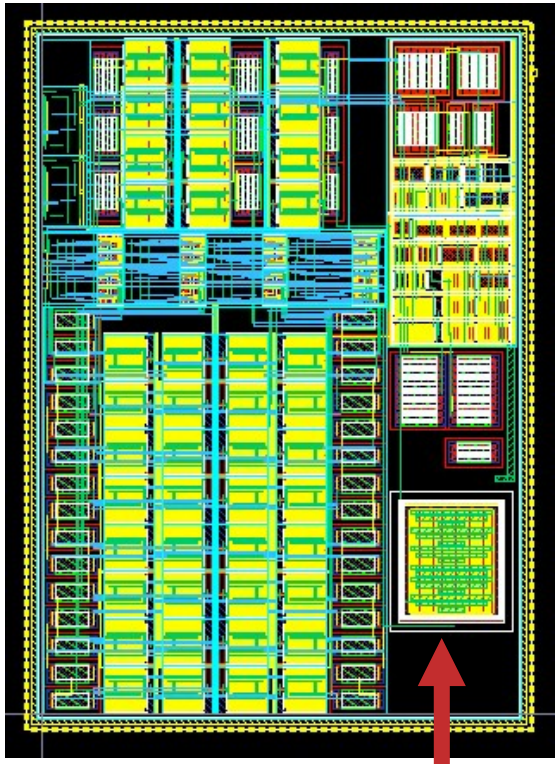
Diode



BJT_VPNP



Gated-diode

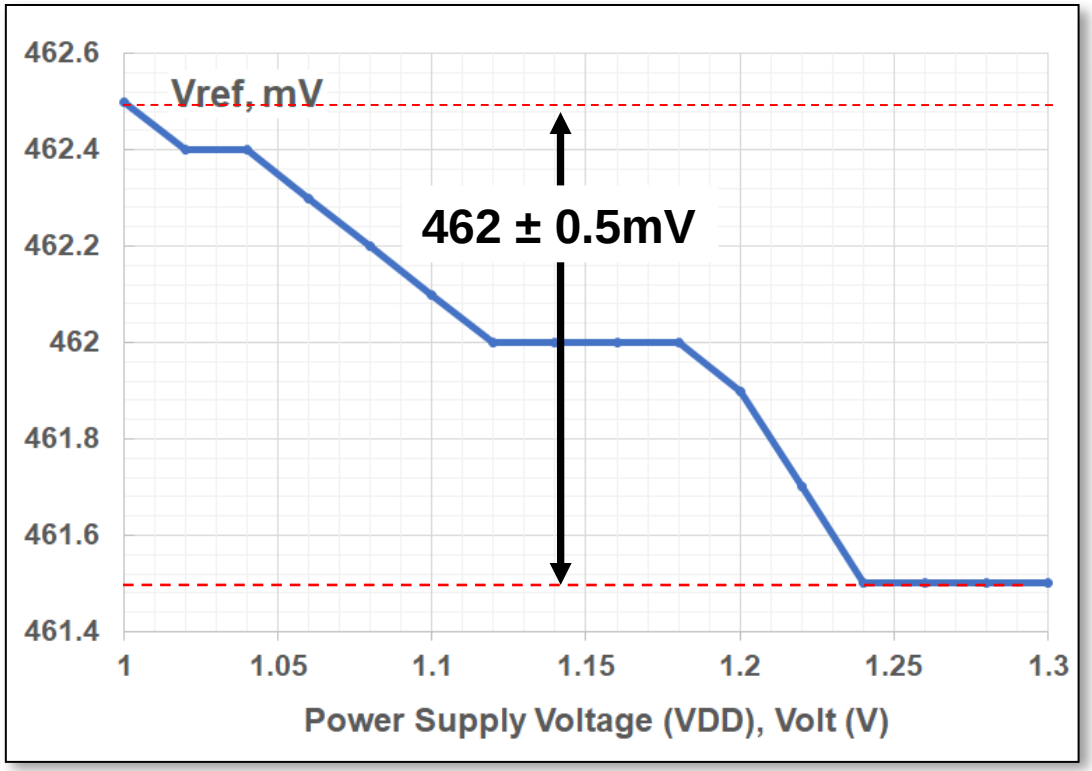


DTMOST

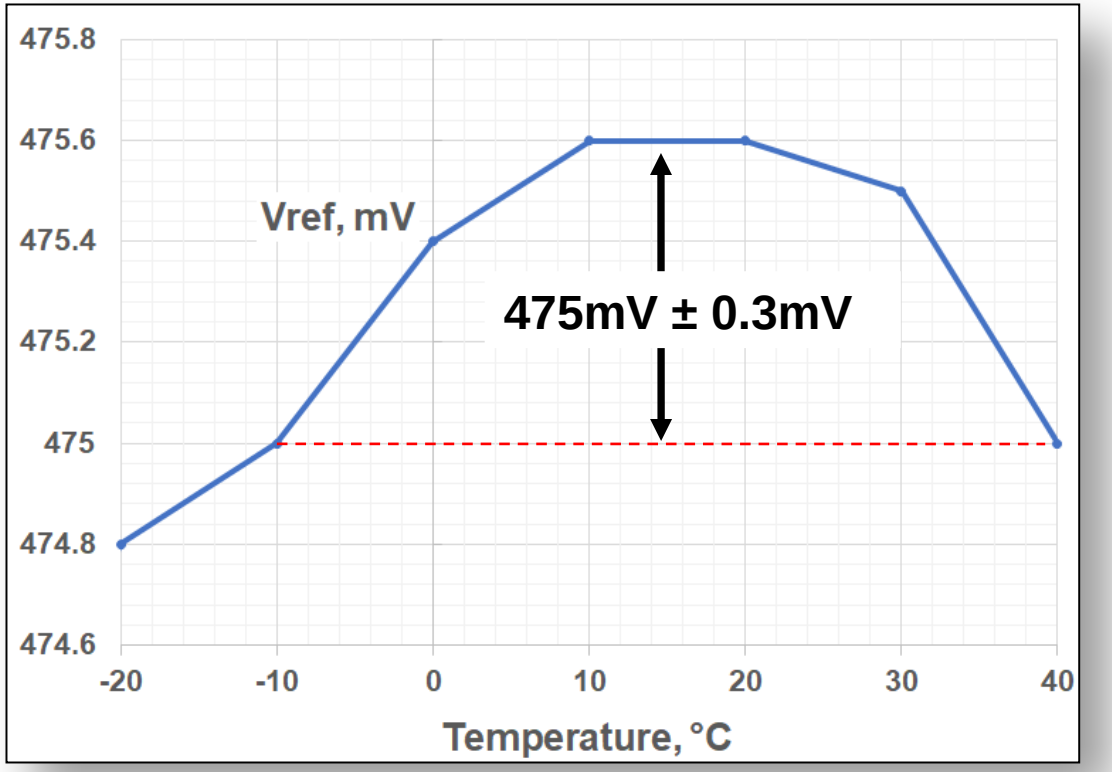
- Each flavour covers 74.4µm × 104.1µm on wafer.

Measurement Results of DTMOST-based BGR

- **BGR**
- TS
- LDO
- Conclusion



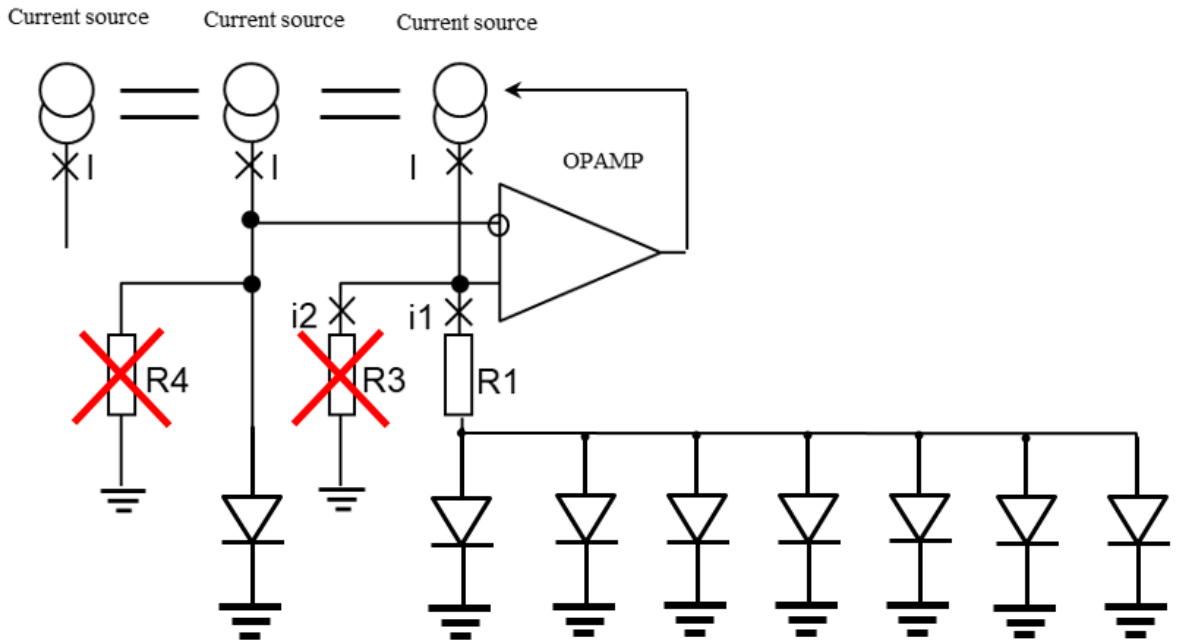
The resulting V_{REF} is equal to **462 ± 0.5 mV** when **VDD** is swept from **1V** to **1.3 V**.

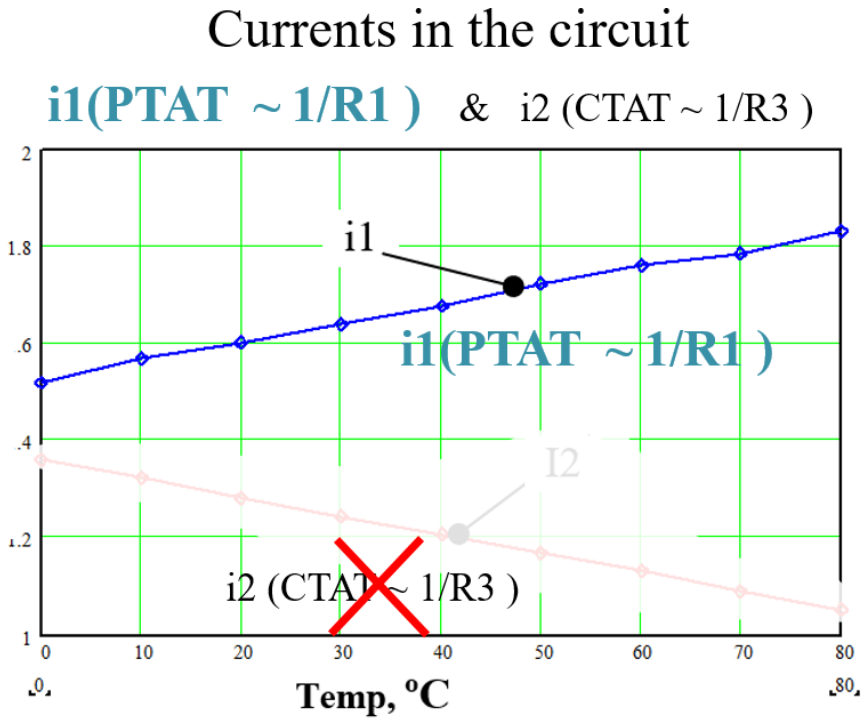


The resulting V_{REF} is equal to **475 ± 0.3 mV** when **temperature** is swept from **-20 ºC** to **40 ºC**.

Temperature Sensor (TS) Circuit

- TS is an essential circuit for **thermal management** of ALICE ITS3 chip.
- **BJT transistors** (NPN or PNP) are mainly used as the sensing element due to their **well-defined I-V** temperature characteristics.



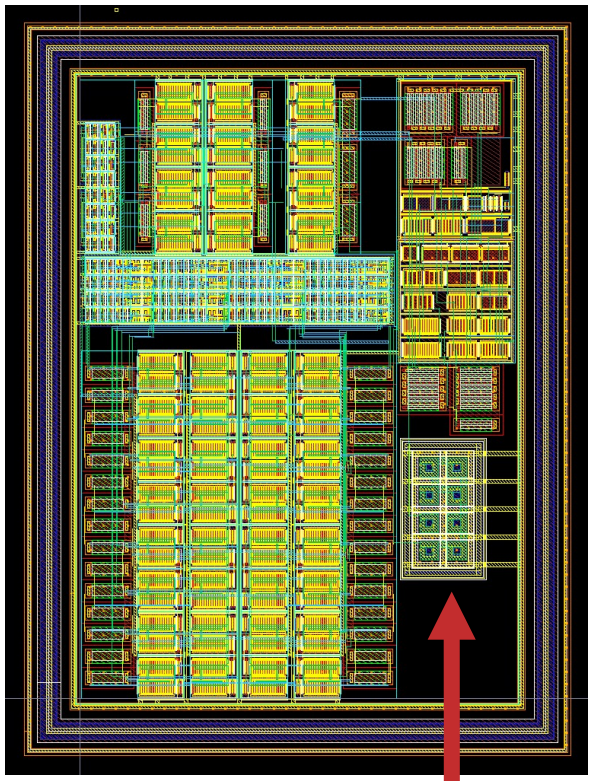


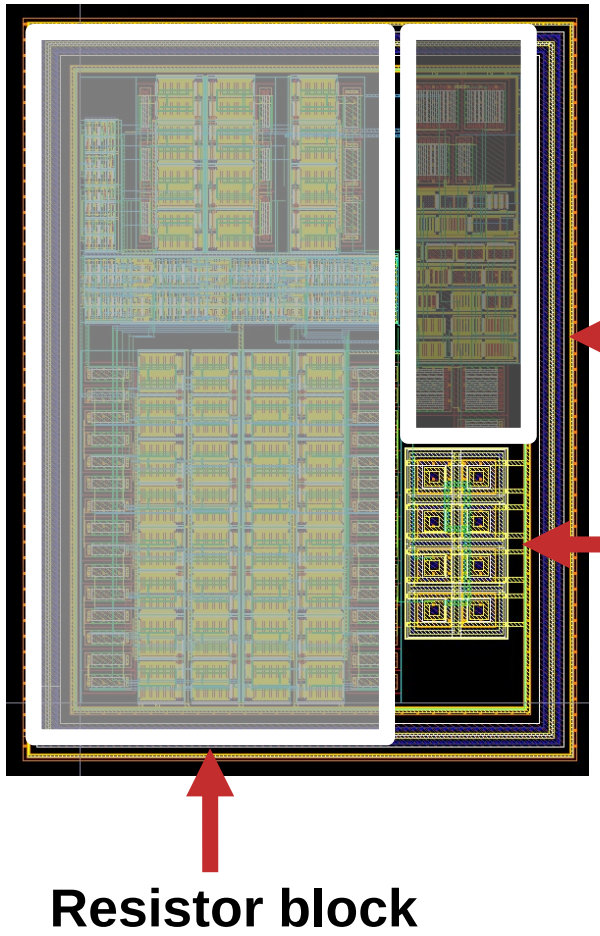
Sensing elements: Diode, BJT

- BGR
- **TS**
- LDO
- Conclusion

Layouts of Implemented TS Circuits

- BGR
- **TS**
- LDO
- Conclusion

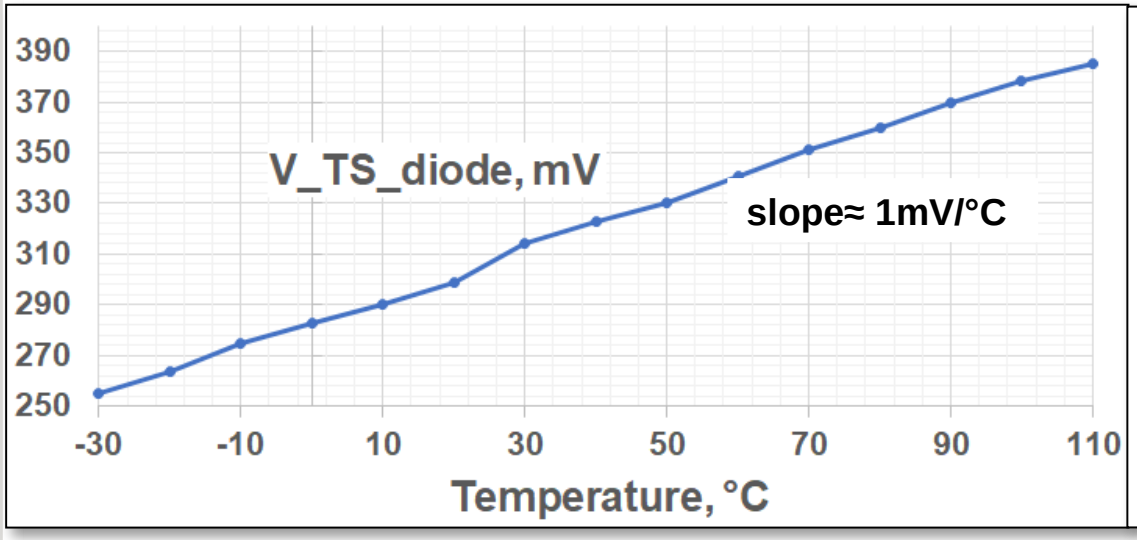


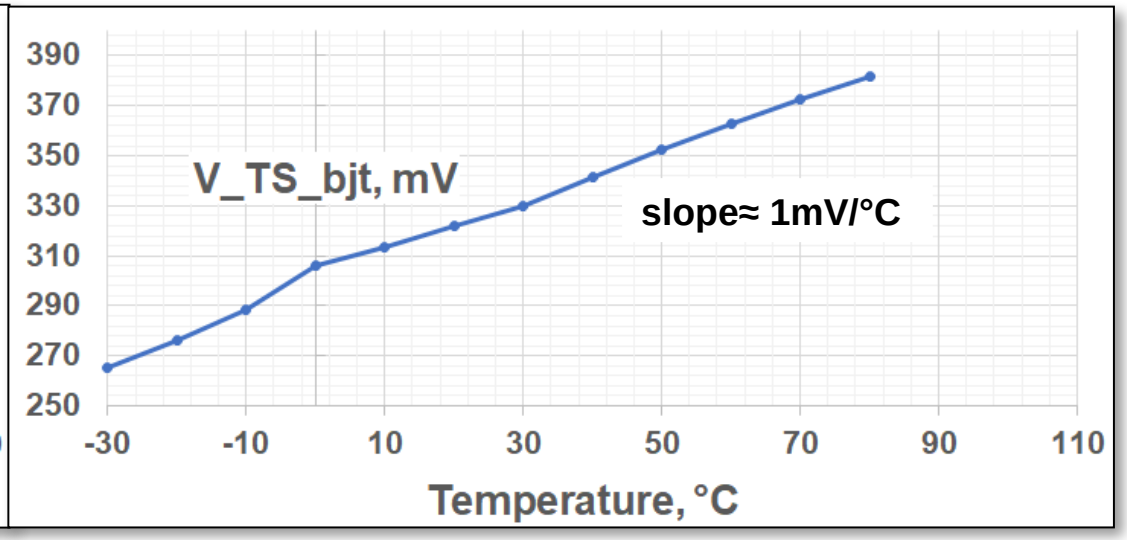


- Each flavour covers 74.4μm × 104.1μm on wafer.

Measurement Results Diode- and BJT-based TS

- BGR
- **TS**
- LDO
- Conclusion

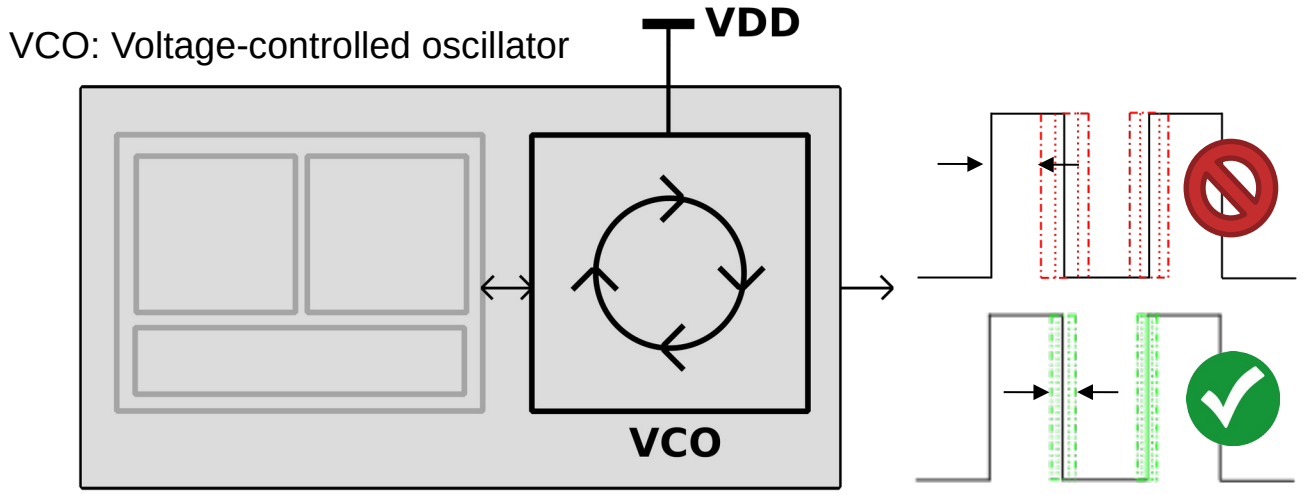




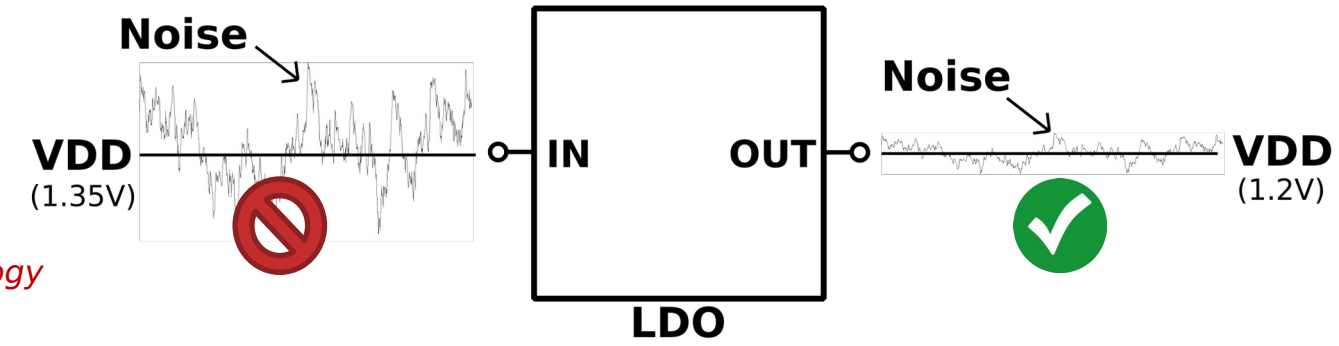
- The **linear operation region** of TS is starting from **-30 ºC** to **110 ºC**.
- TS provides a **1 mV/ºC gradient** within the **specified temperature range**.

Motivation of Design of Low Drop-out Regulator

- BGR
- TS
- **LDO**
- Conclusion



Reference Phase-Locked Loop (PLL)



LDO: Low Drop-Out Regulator

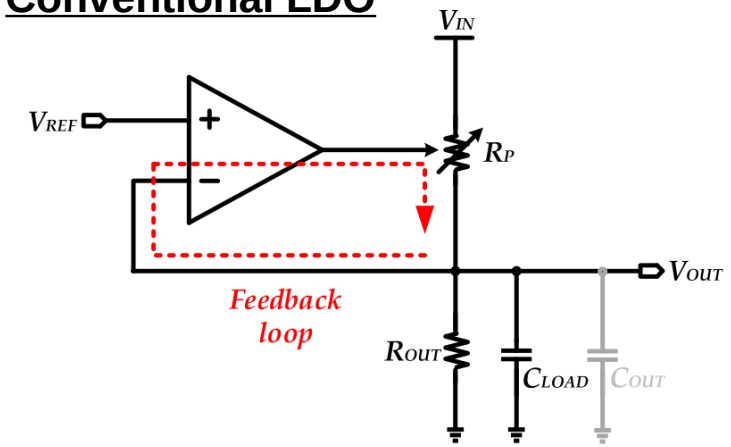
✔ **Clean DC output** voltage for **VDD**

Clean and **more precise clock** generation

Design Considerations of LDO

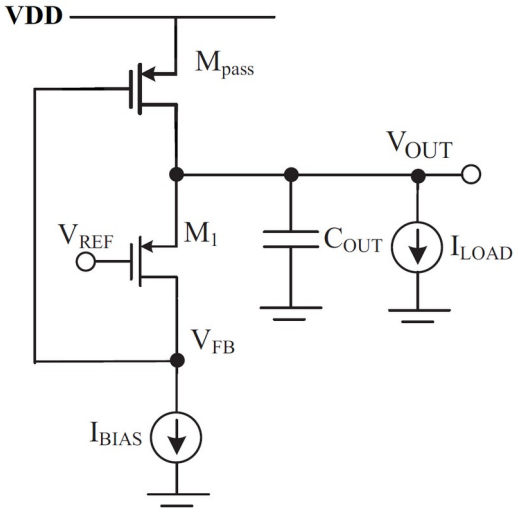
- BGR
- TS
- **LDO**
- Conclusion

Conventional LDO



- **Clean V_{out}** is maintained through the feedback loop.
- Frequency compensation is needed. → **C_{OUT}** implemented **(in µF range)**
- **Extra pad/pin** to outside world.
- **Not suitable** for on-chip LDO implementations.

Flipped Voltage Follower (FVF) Based LDO



- Gate voltage of M_{pass} is adjusted through the feedback.
- **I_{load}** is defined by the **PLL**.
- ✔ **C_{OUT}** is in the range of **pFs**.
- ✔ **Suitable** for **on-chip** LDO implemantations.

Implemented Design of LDO

- BGR
- TS
- **LDO**
- Conclusion

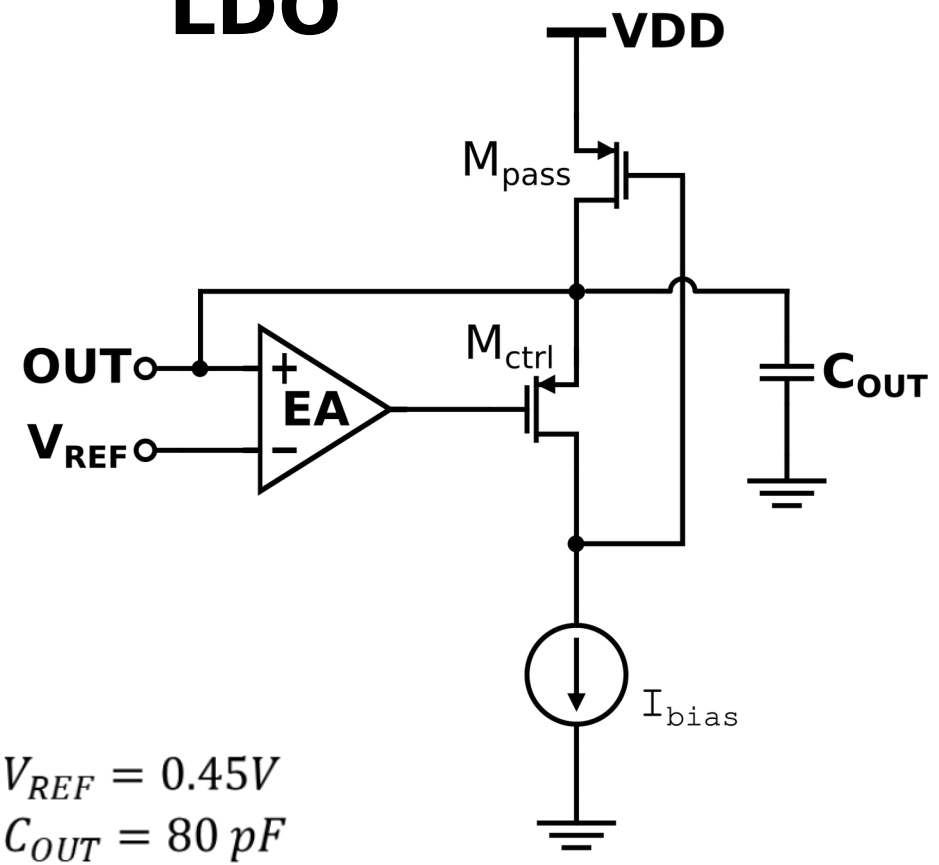
Desired characteristics from LDO:

- **Less sensitive** to power supply noise (good PSRR)
- **Low output impedance**

EA: Error Amplifier is implemented for better low frequency response:

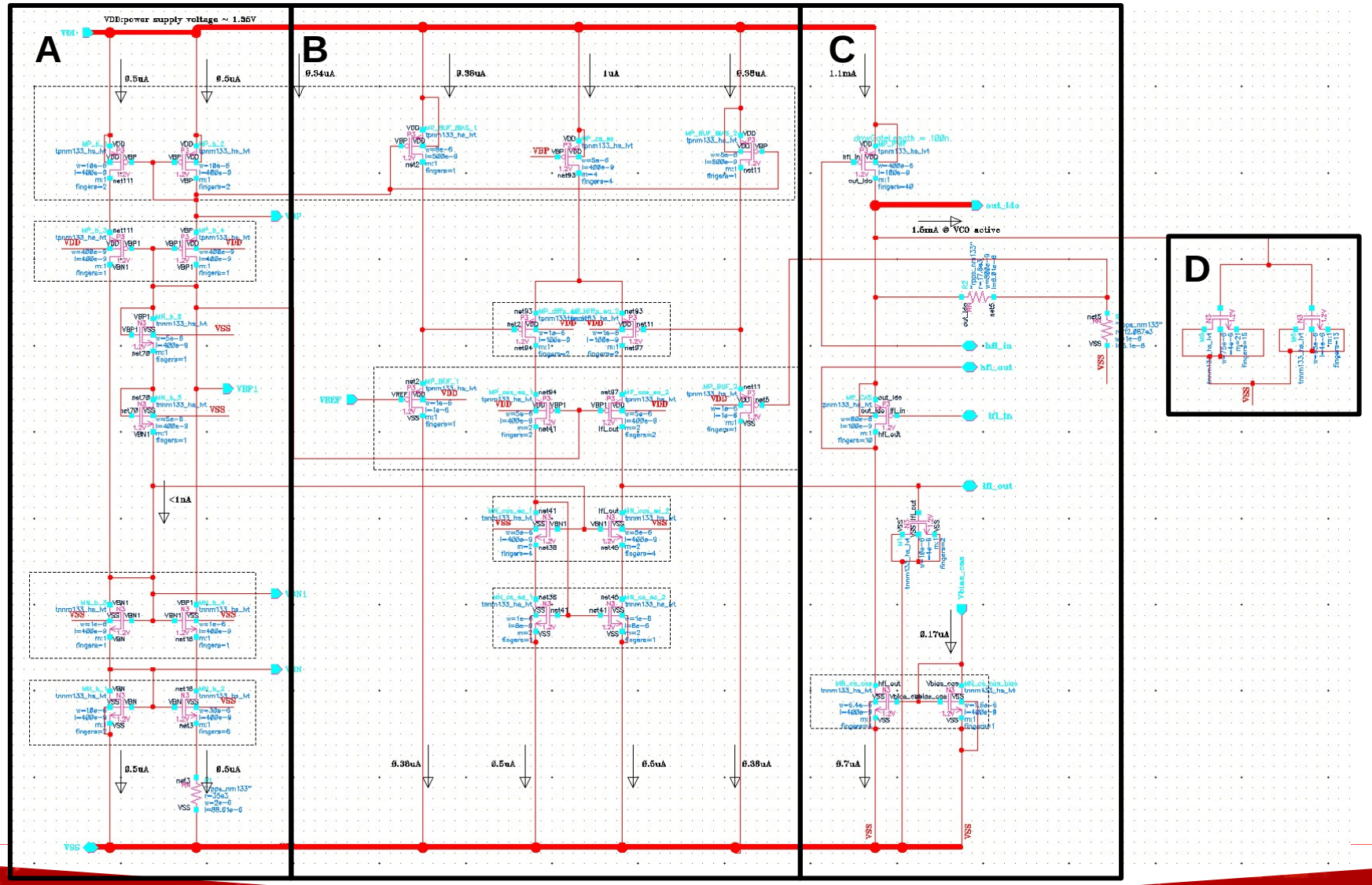
- ✔ To **decrease** the **output impedance** of LDO
- ✔ To **increase** the **loop gain** and **PSRR**

Implemented LDO



Schematic of Implemented LDO

- BGR
- TS
- **LDO**
- Conclusion



A: Biasing circuit
B: Error amplifier
C: FVF-based regulator
D: C_{OUT}

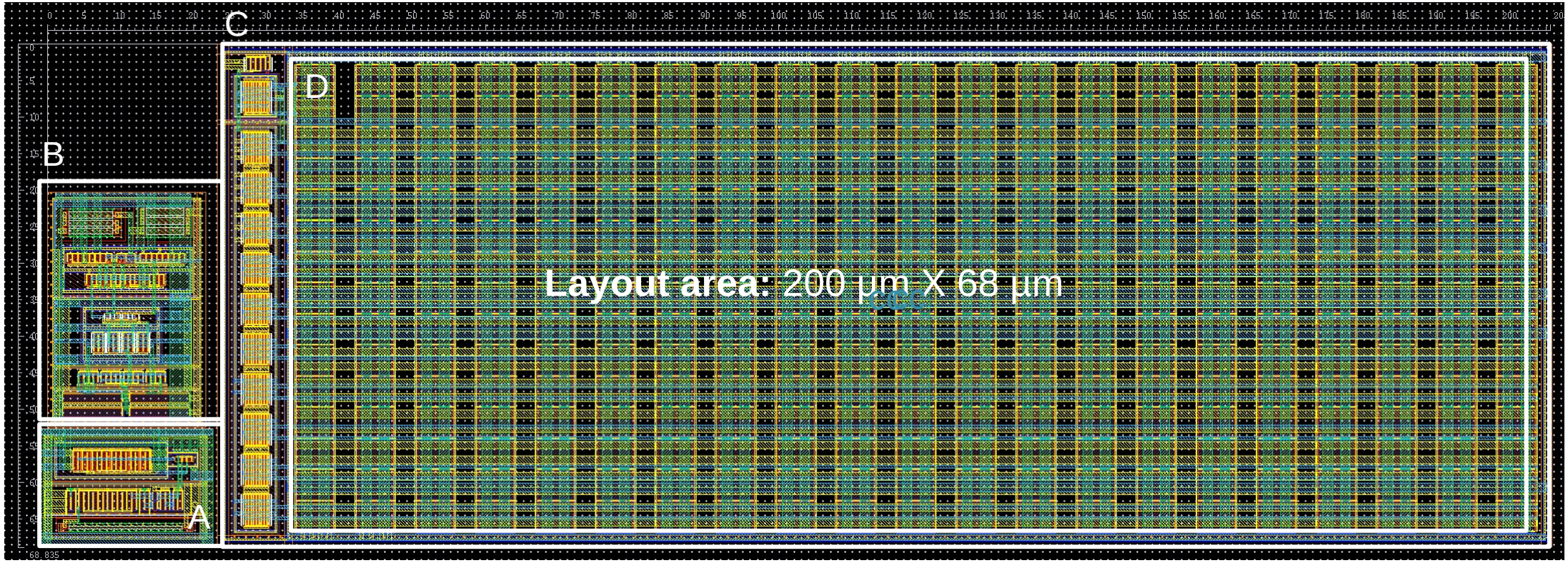
Electronics Technology

ALICE ITS3

Nikhef

Overview of Layout

- BGR
- TS
- **LDO**
- Conclusion

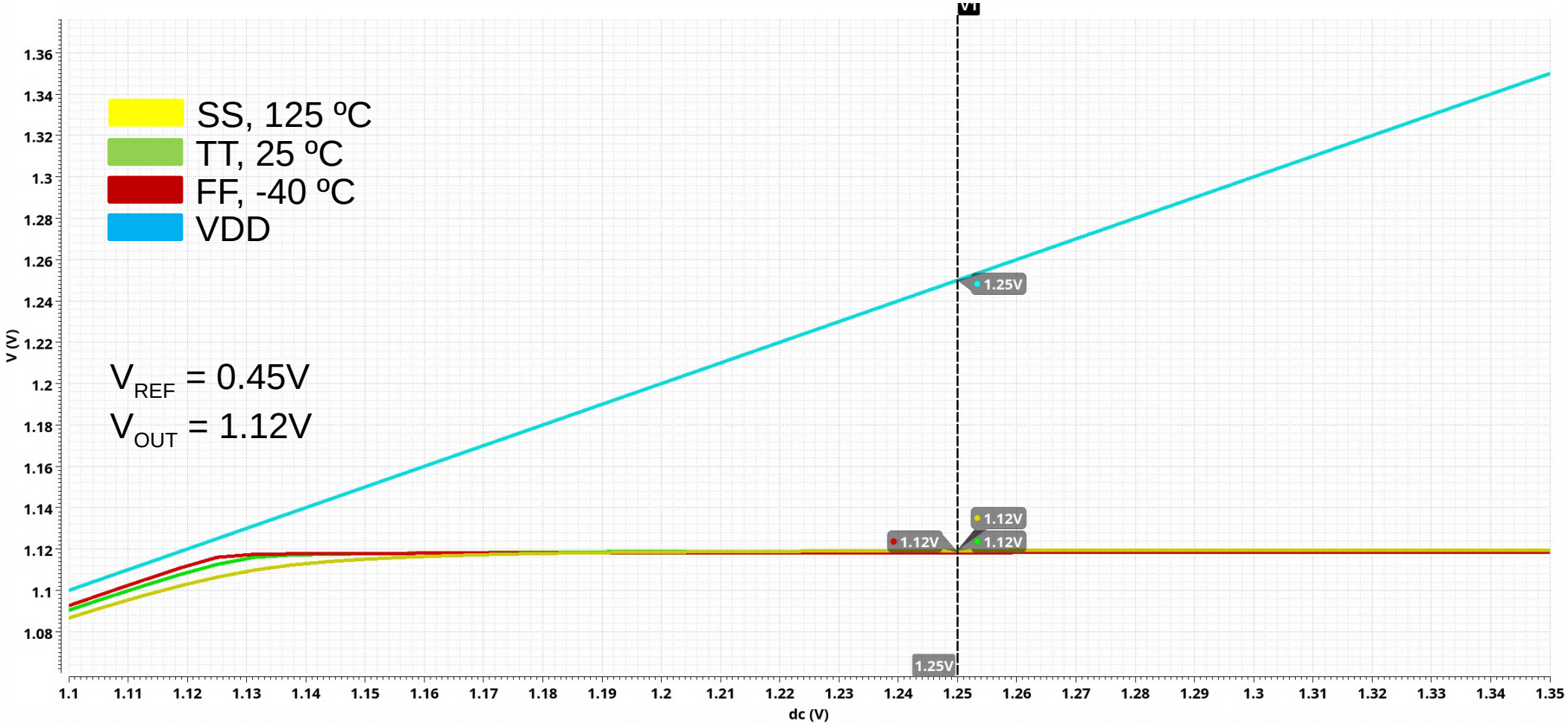


A: Biasing circuit **C:** FVF-based regulator
B: Error amplifier **D:** C_{OUT}

- **All** available **metal layers** are used to achieve $\mathbf{C_{out}}$ with **low parasitic resistance** at the output.

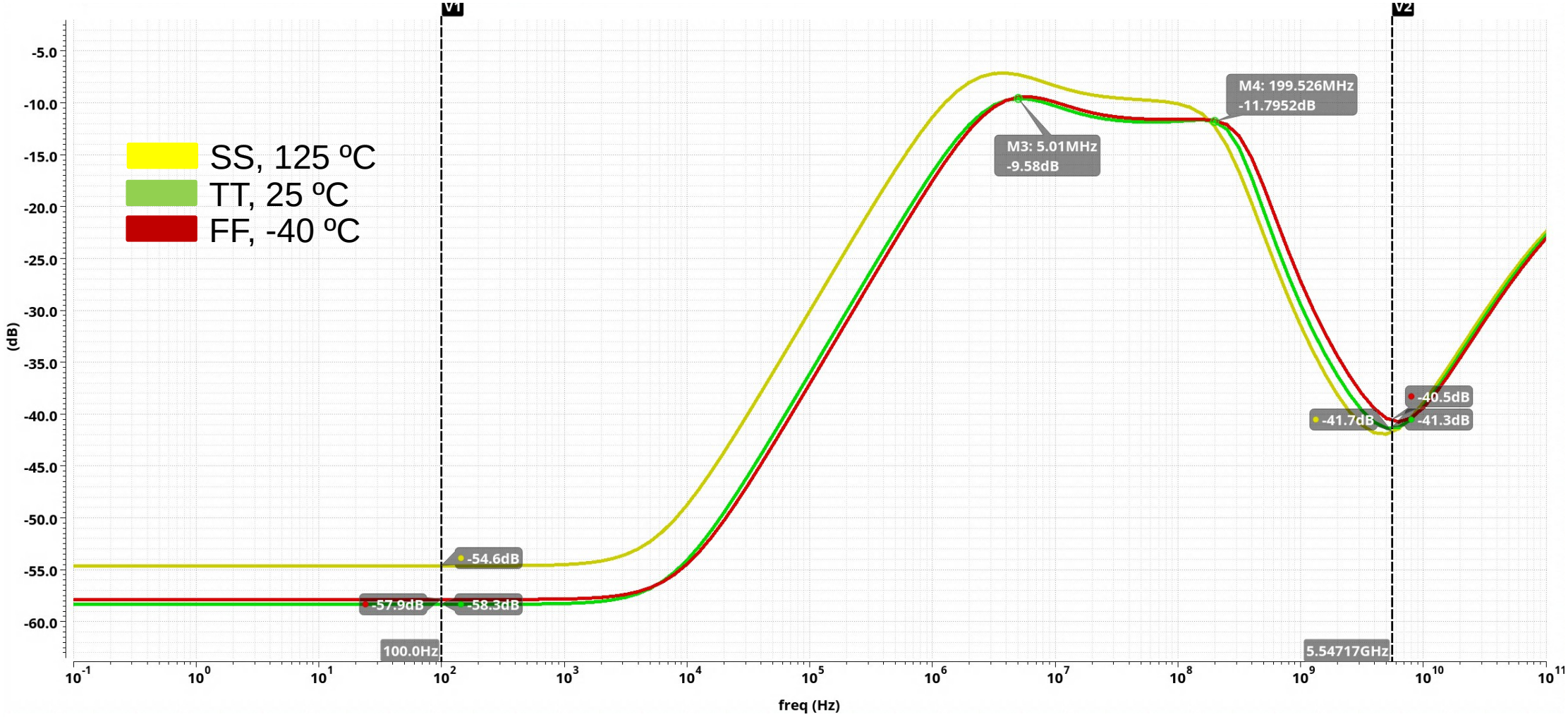
Post-layout Simulations - DC Sweep

- BGR
- TS
- **LDO**
- Conclusion



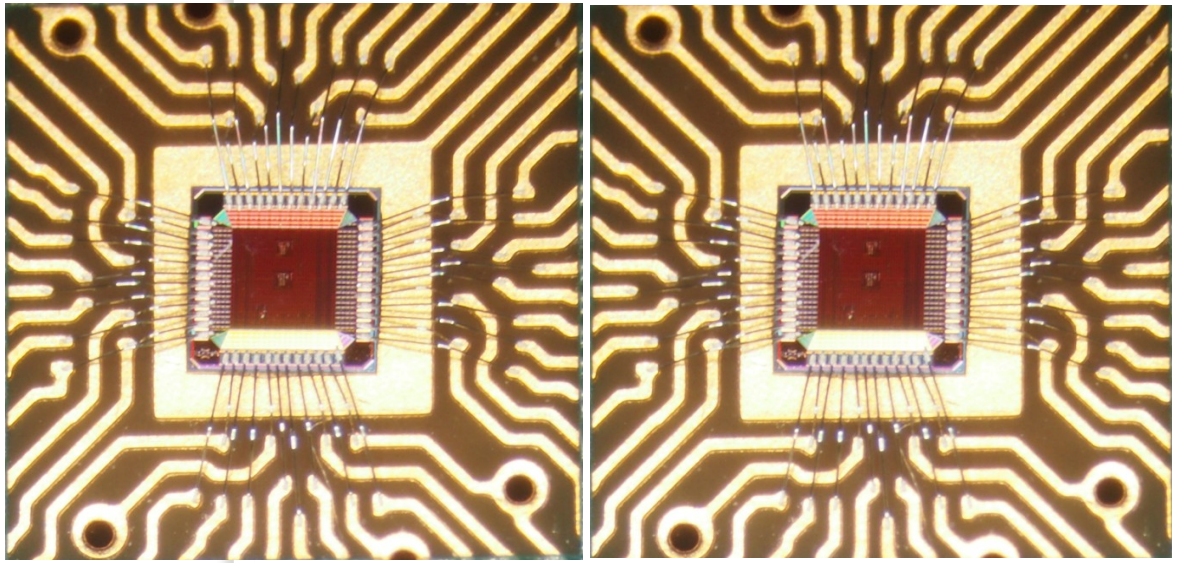
Post-layout Simulations AC Analysis - PSRR

- BGR
- TS
- **LDO**
- Conclusion

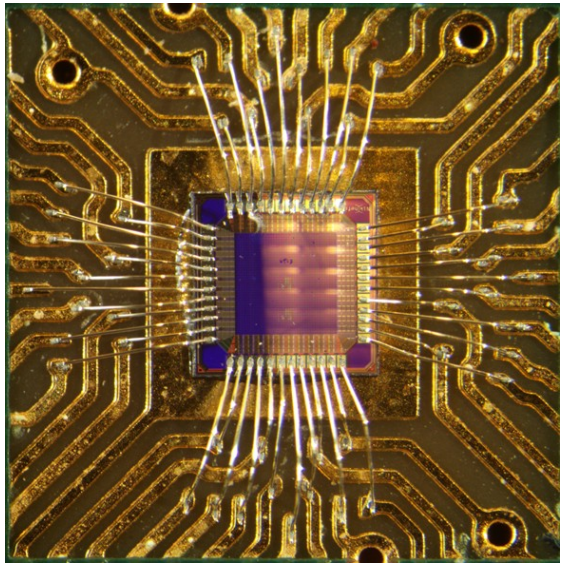


- PSRR up to **1 kHz** → **-58 dB**
- PSRR **around 5 MHz** → **-10 dB**

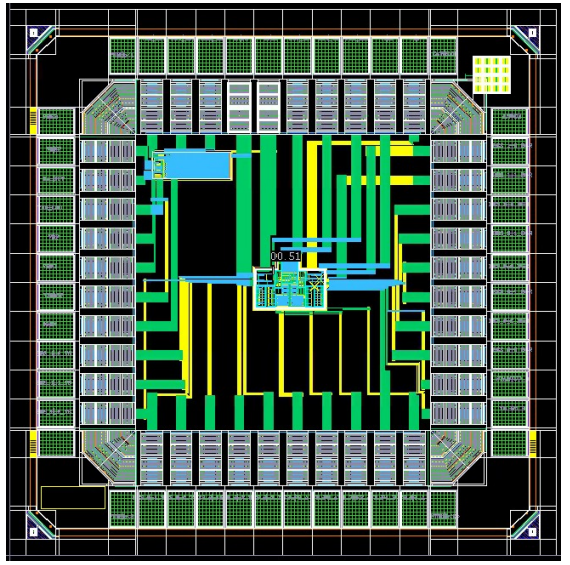
Conclusion



BGR with 4 flavours
TPSCo MLR1



TS with 2 flavours
TPSCo MLR1



LDO
TPSCo ER1

EP R&D

- BGR
- TS
- LDO
- Conclusion

Conclusion

- **ALICE ITS3** Upgrade deploys **Monolithic Active Pixel Sensors** (MAPS) in **stitched** manner and aims to have **very low material budget** (0.05 % X_0).
- **Measurements** of **DTMOST-based BGR** show that $\mathbf{V_{ref}}$ changes in the range of **462 ± 0.5mV** when **VDD** is **swept** from **1V to 1.3V**.
- Temperature scan measurements demonstrate that **DTMOST-based BGR** has the **lowest variation** of the value of $\mathbf{V_{ref}}$ with **475 ± 0.3 mV.**
- The measurements show that the output voltage of TS provides a **1mV/ºC gradient** within the **specified temperature range** (-30 ºC to 110 ºC).
- **FVF-based Output Capacitor-less LDO** provides **1.12 V of output voltage**, and has **PSRR** of **-59 dB** up to 1 kHz.

Acknowledgement

- Shi Qui (Utrecht University)
- Marcel Rossewij (Utrecht University)
- Alessandro Grelli (Utrecht University)
- Deepak Gajanana (NIKHEF)
- Vladimir Gromov (NIKHEF)

Q&A

Thank you very much for your attention!

Back-up

Table of Performance of Proposed LDO

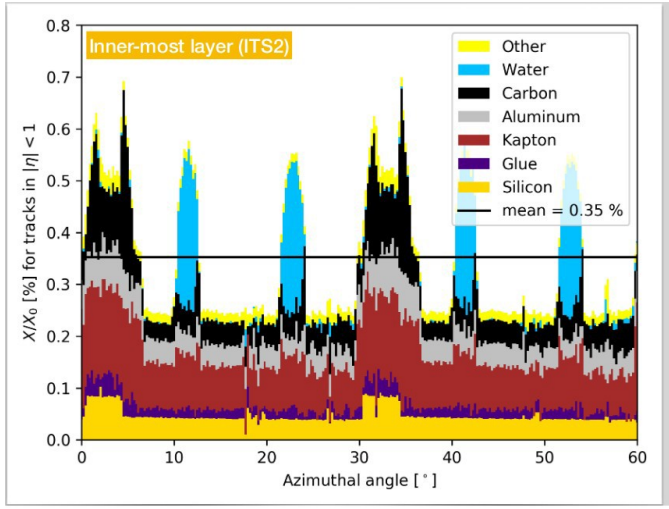
- Motivation
- Proposed Design
- Simulation Results
- Conclusion
- Future Work

Parameters	Units	Proposed LDO	
Technology	nm	TJ 65	
Chip Area	mm^2	0.014	
V_{in}	V	1.32	
V_{out}	V	1.12	
Dropout voltage	mV	200	
On-chip Capacitance	pF	80	
PSRR	dB	Best	Worst
		-58	-10
R_{OUT}	Ω	27 m	13
Phase margin (HF region)	Deg (º)	74	65.3
Phase margin (LF region)	Deg (º)	81	80

Conclusion

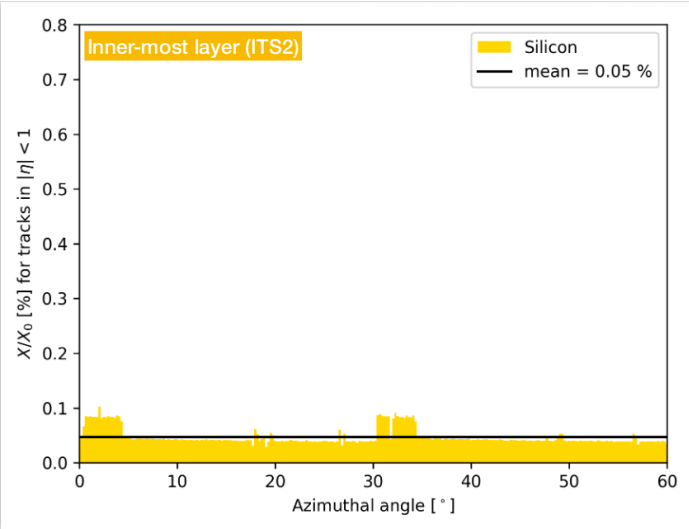
- **Clean output voltage (1.12V)** across VDD=1.15V to VDD=1.35V
- **Output impedance** (R_{out}) is around **27 to 50 mΩs** over the frequency range from a few Hz's to 10 kHz.
- R_{OUT} hits its maximum value **13 Ω** at **295 MHz**.
- **Nominal PSRR** value in the low frequency range (1-1kHz) is **-58 dB**.
  - After **2 GHz**, PSRR is getting decreased from **-27.4 dB** to **lower values.**
- **Fluctuations** on supply voltage can be **suppressed** when ripples are **less than 30 mV**.

- Motivation
- Proposed Design
- Simulation Results
- Conclusion
- Future Work



➡ Si only 1/7th of total material

➡ irregularities due to overlaps + support/cooling



➡ Si only 1/7th of total material

➡ irregularities due to overlaps + support/cooling

➡ remove water cooling

➡ possible by reducing power consumption in fiducial volume to <20 mW/cm²

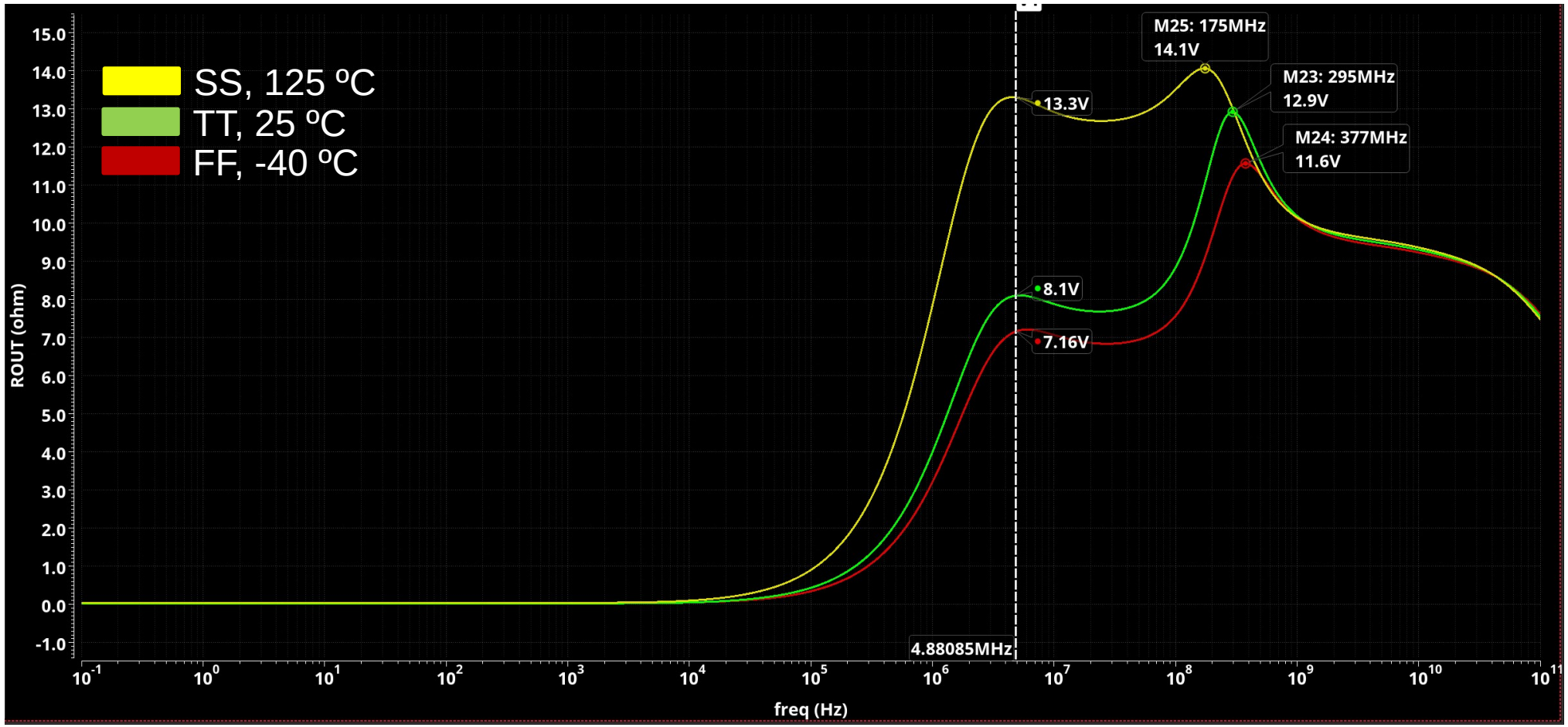
➡ remove external data lines + power distribution

➡ possible by making a single large chip and that for distribution

➡ move mechanical support outside acceptance

➡ benefit from increased stiffness by rolling Si wafers

Post-layout AC Analysis - R_{OUT}

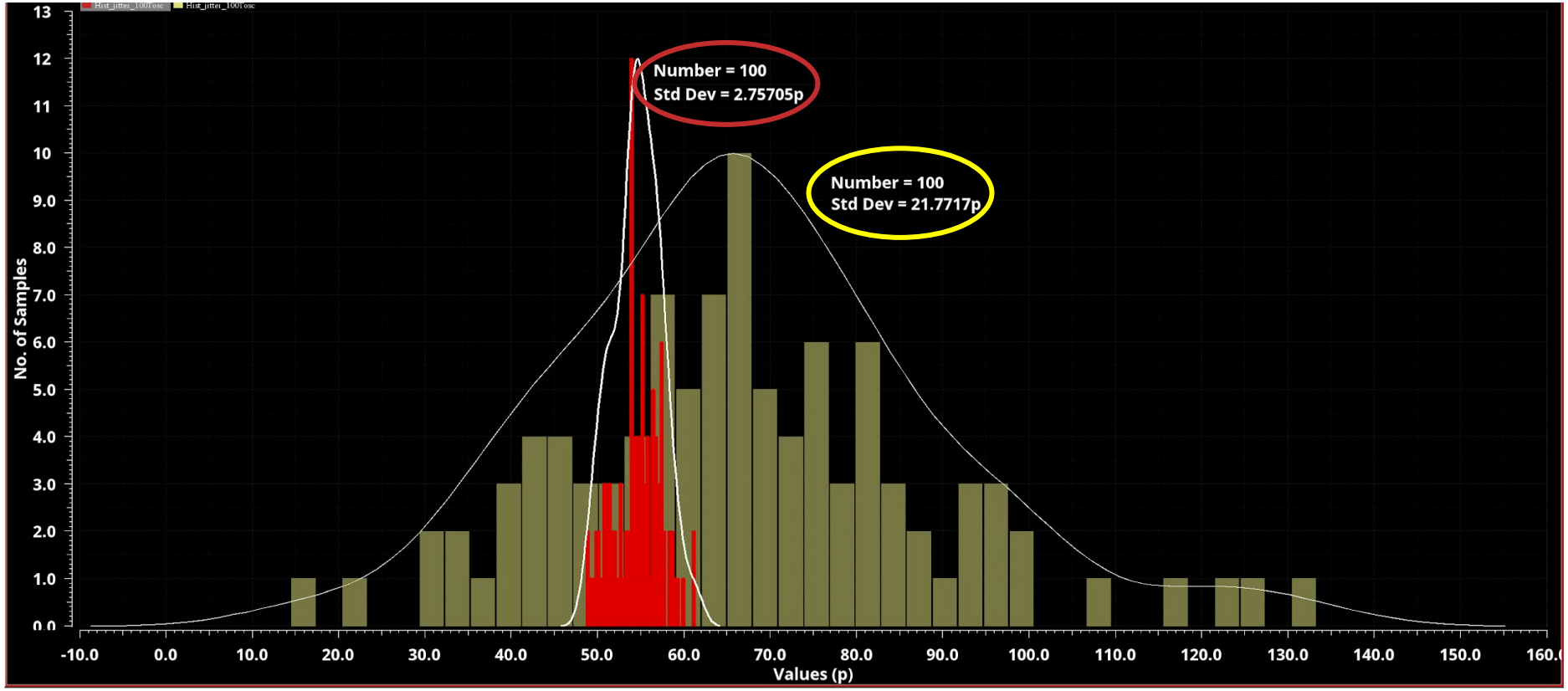


- Motivation
- Proposed Design
- Simulation Results
- Conclusion
- Future Work

- R_{OUT} at **low frequency** range (from 10 Hz to 10 kHz) → from **27 mΩ** to **50 mΩ**
- R_{OUT} at **higher frequencies** (> 100 kHz) →
  - One peak occurs at **5 MHz** as **8.1 Ω**
  - Hits its **maximum** at **295 MHz** as **13 Ω**

Internal Time Jitter of VCO (2)

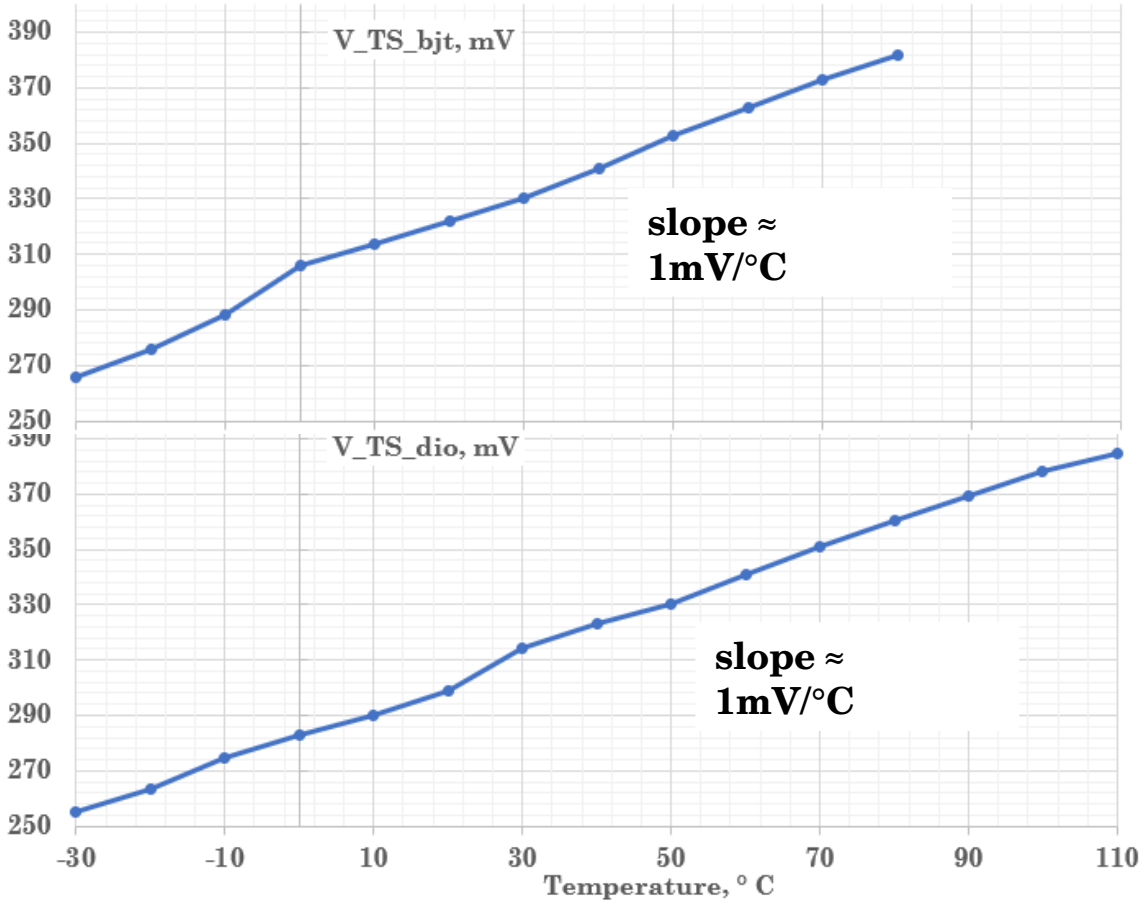
- Motivation
- Proposed Design
- Simulation Results
- Conclusion
- Future Work



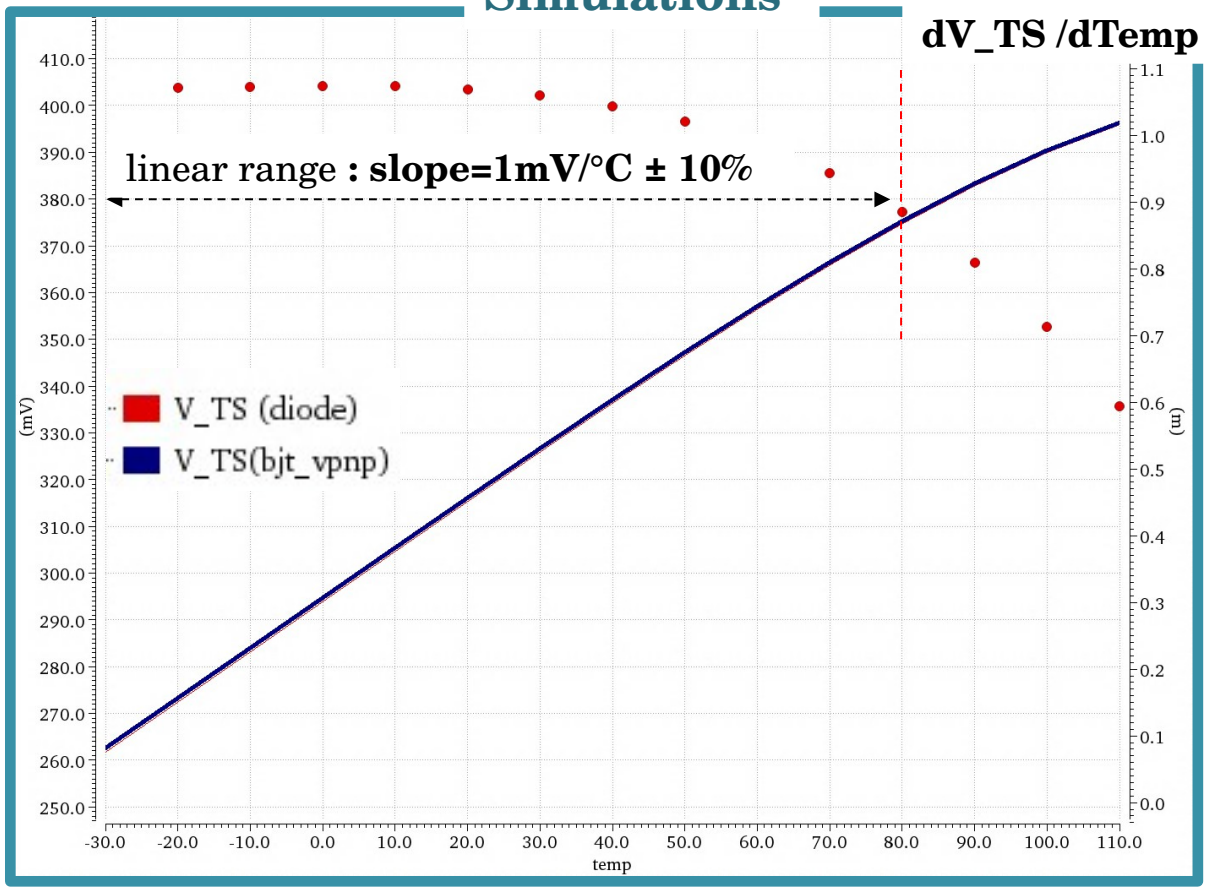
- Time jitter with Scenario #1 ⇒ **2.8 ps**
- Time jitter with Scenario #2 ⇒ **21.8 ps**

Temperature scan @ Voltage mode

Measurements (chip: Nikhef 3 @ Vdd=1.2V)



Simulations



- linear operation region of the TS circuit : -30°C .. 110° C
- a 1mV /°C low-slope characteristic and limited output range 260mV … 400mV
- an additional circuit will be probably required to enlarge the output range (sensitivity) up to the full dynamic range (0 …. 1.2V)

Internal Time Jitter of VCO

- Motivation
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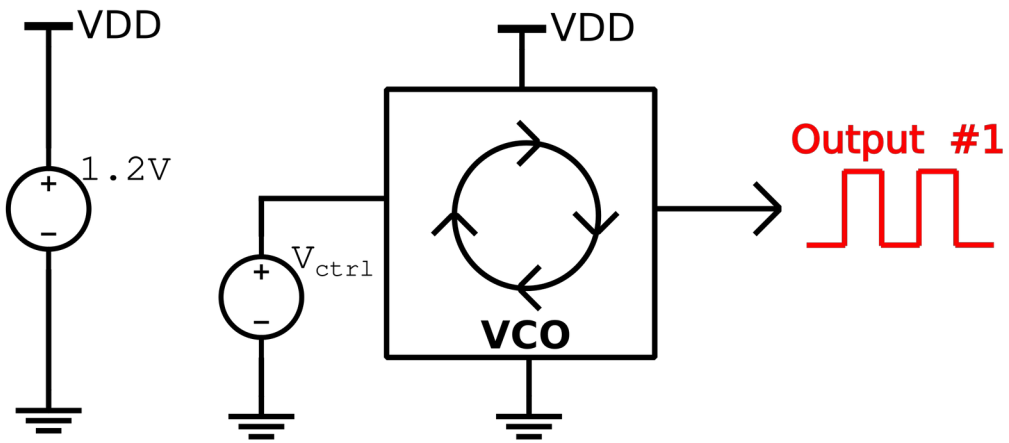
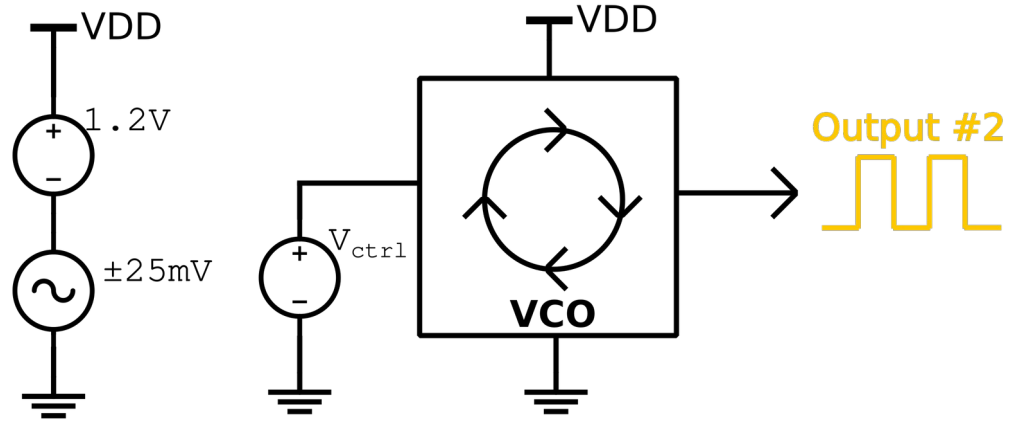
- Future Work

Scenario #1



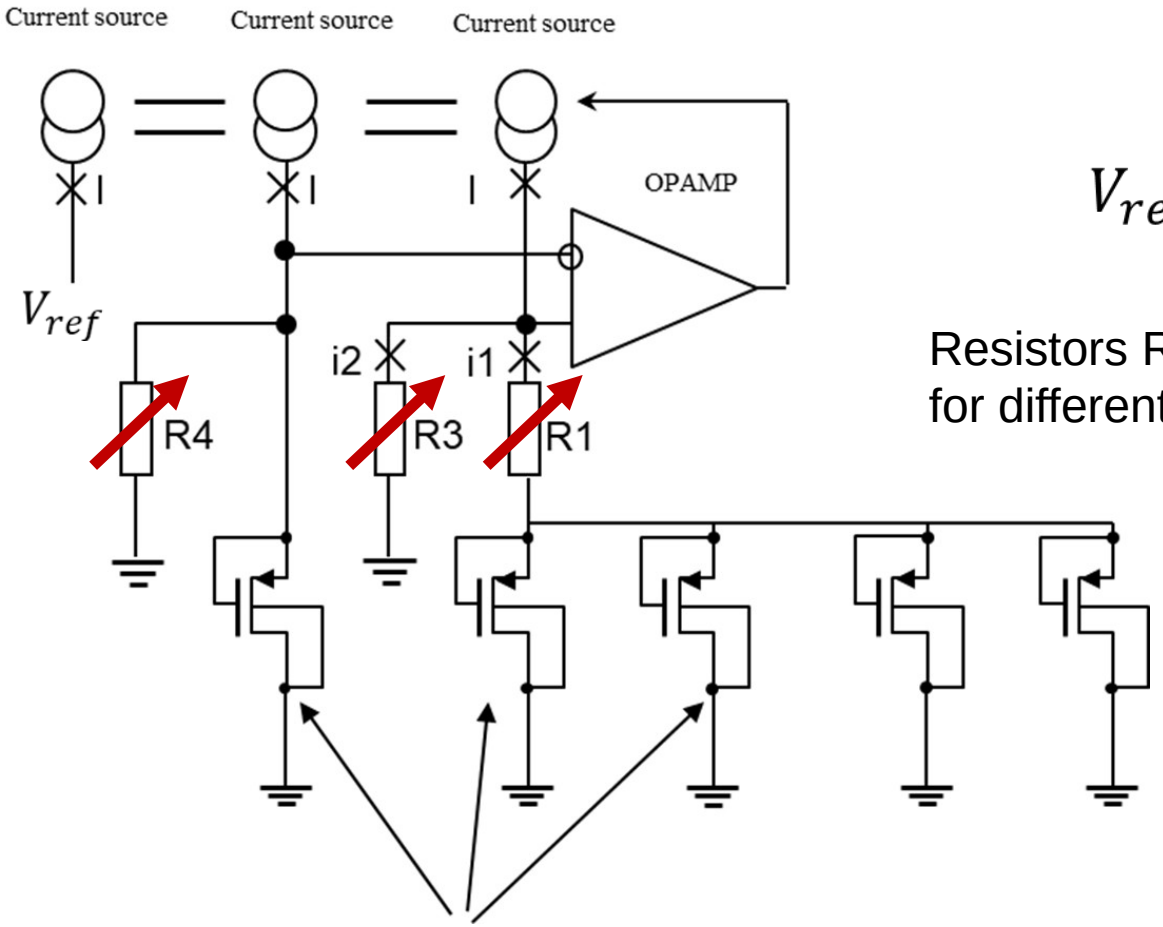
- **Ideal VDD** supply voltage at 1.2V
- **Ideal control** voltage for VCO
- **Noise contributor** is only **VCO**
- **Output #1** is indicative of **internal** time jitter

Scenario #2



- **Non-Ideal VDD** supply voltage
- **Ideal control** voltage for VCO
- **Noise contributor** is **VCO** and **VDD**
- **Output #2** is **indicative** of the effect of **non-ideal VDD** on time jitter

Proposed BGR Circuit



$$V_{ref} = \frac{R_4}{R_3} V_{ref,conv}$$

Resistors R1, R3, and R4 can be controlled for different process variations.

Reference elements: diode, BJT, gated-diode, DTMOST