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UVVM (Universal VHDL Verification Methodology) - The world-wide #1 for VHDL verification - Made in Norway

Wednesday, 21 September 2022 10:30 (45 minutes)

The UVVM (Universal VHDL Verification Methodology) is the fastest growing FPGA verification methodology world-wide - independent of language, and number 1 for VHDL. Furthermore, VHDL is used by 50% of all FPGA designers, and between 80% and 90% of all FPGA designers in Europe. Thus UVVM has become a very important verification methodology for FPGA designers, and in fact also for quite a few ASIC designers. And UVVM is made in Norway.

The fast growth and popularity is primarily due to the improvement that UVVM yields in both FPGA quality and development time. This open-source Library and Methodology has the most extensive VHDL verification support available and lets you verify really complex DUTs in a very efficient manner providing modularity, reusability, constrained-random stimulus and functional coverage similar to UVM, but all in a way familiar to VHDL designers. UVVM also has the largest library of open source VHDL verification models and components. With more than 50% of all FPGA designers using VHDL, UVVM provides a great verification solution for these users.

This presentation will first try to explain to non-FPGA designers what this is all about; - FPGA, Verification, UVVM...
Then we will go more into detail and show you how UVVM works and how it significantly helps on quality and efficiency through readability, maintainability, debuggability and reuse.

Espen Tallaksen is the CEO of EmLogic, a leading design centre for Embedded Systems and FPGA in Norway. He graduated from the University of Glasgow (Scotland) in 1987 and has 30 years experience with FPGA and ASIC development from Philips Semiconductors in Switzerland and various companies in Norway.

During twenty years Espen has had a special interest for methodology cultivation and pragmatic efficiency and quality improvement. One result of this interest is the UVVM verification platform that is the #1 VHDL verification methodology and library world-wide, and in fact the fastest growing FPGA verification methodology independent of HDL.

He has given many presentations internationally on various technical aspects of FPGA development, including lots of hands-on tutorials and keynotes, all with a crowded audience and great feedback. He is also giving courses world-wide on how to design and verify FPGAs more efficiently and with a better quality.

Summary (500 words)

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