CHIPS: CERN-HEP IC design Platform & Services

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On behalf of the CERN CHIPS team

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CHIPS is an ASIC support service for HEP

- The **CHIPS service started in January 2020** to address the concern, expressed by the CERN SPC (Scientific Policy Committee), that **delays in the development of some ASICs** could have serious repercussions on the physics programmes of the HL-LHC experiments

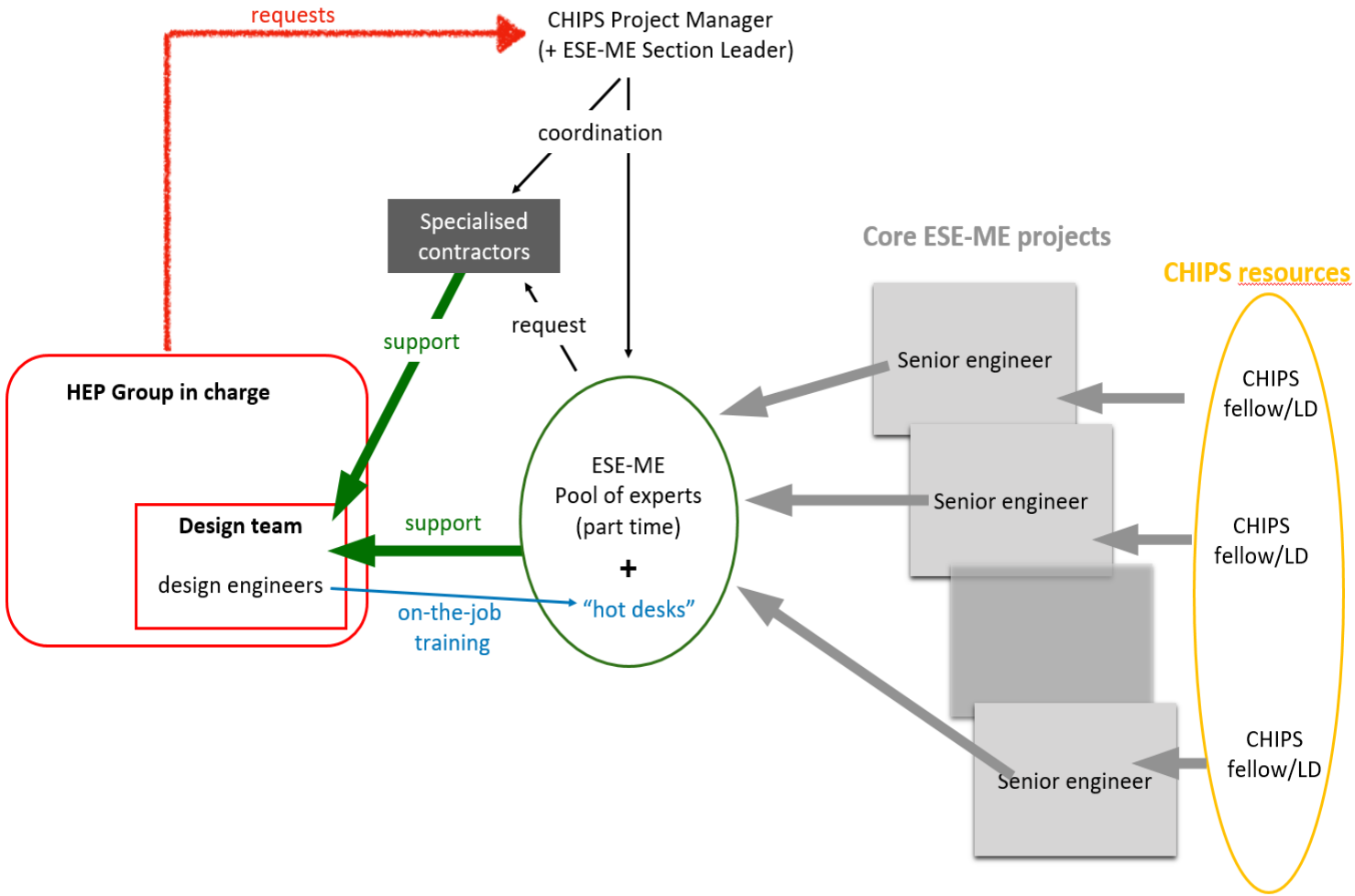
- These delays were attributed to the **increased complexity of both the ASICs and the tools** required for their development in the sub-micron technologies chosen for the upgrades

CHIPS: CERN-HEP IC design Platform & Services

- **ASIC design support from EP-ESE-ME experienced designers to HEP community**
- **Subcontract specialised ASIC design tasks**
- **Train and coach HEP ASIC designers in medium to long term**

Responsible: X. Llopart

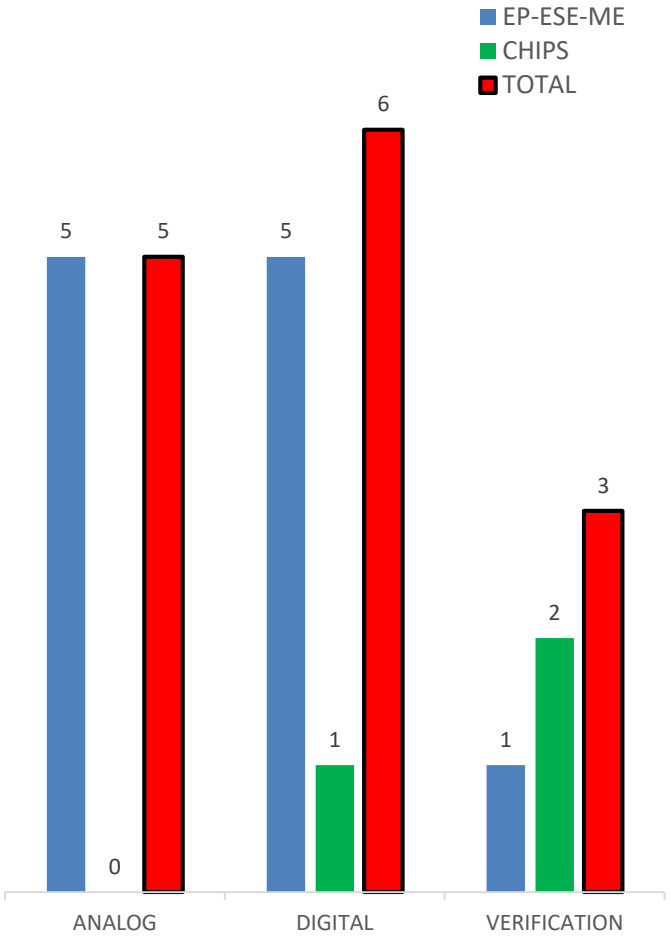
CHIPS Organization



CHIPS Manpower

- Support requests are shared amongst the EP-ME-ESE ASIC expert designers:
  - 5 FTE: Analog and macroblock design, radiation effects
  - 5 FTE: Digital implementation, timing closure and physical verification
  - 1 FTE: Functional verification and top-level simulation

- CHIPS resources **compensate the support** given by the ASIC experts and **correct the lack of verification engineers** in the section:
  - 2 Fellow from January 2020:
    - 1 Digital (Gianmario)
    - 1 Verification (Simone)
  - 2 Staff Verification Engineer from November 2020:
    - Stefano Esposito from November 2020
    - Matteo Lupi from January 2021
  - 2 New Staff engineers from January 2023



* CHIPS Fellows are unexperienced and require training. They are counted as 0.5 FTE

Sustained support provided since January 2020

	ASIC	Experiment	Support	Status
WP1	MPA and SSA	CMS outer tracker	• 1 fellow (digital design) from January 2020. 11 months full time + 6 months at 50% • 1 fellow (verification) from January 2020. 16 months full time + 3 months at 100%	**Finished on May 2021**
WP2	ALTIROC	ATLAS HGTD	• Hosted 1 engineer on September 2020 (Hot desk) • 1 fellow (digital design) from November 2020 at 50%, from September 2021 at 100% • 1 fellow (verification) from September 2021 at 100%	**On-going ALTIROC3 Q4-2022**
WP3	RD53_ATLAS RD53_CMS	ATLAS & CMS pixel detector	• 1 staff member (verification) from November 2020 • 1 staff member (verification) from September 2022 to December 2022 • 1 staff member (digital design) from September 2022 to December 2022	**On-going RD53C_ATLAS Q4-2022 RD53C_CMS Q2-2023**
WP4	ECON-T ECON-D	CMS HGCAL	• Occasional technical support (tools, digital flow scripts, SEE fault injection verification and use of TMRG tool,…) • 1 staff (verification) full time from January 2021 (100%) • 2 staff (digital design) from February 2022 (~60%) • Hosted 2 Fermilab engineers ~1week	**On-going ECON-D Q4-2022 ECON_T2 Q3-2023**
WP5 WP6	HCCstar	ATLAS ITK (Strip Detector)	• Rolling-review process: 25 meetings for 9 months (~160 EEH*) • Occasional technical support (SEE, TMRG, VOLTUS) • Evaluation and development of blocks to prepare a possible backup in 65nm	**Finished on August 2021**

*EEH: Engineer Equivalent hours

Occasional support provided in 2020-21

- CHIPS coordinates the participation of the ME-ESE engineers in ASIC Design Reviews and technical design meetings (verification, power analysis, TMR strategy):
  - >35 ASIC reviews since January 2020 with the participation of 2-4 ESE engineers

- Support given since January 2020 to:
  - ATLAS: RD53, ITK (HCC*, AMAC, ABC*), AM08, ALTIROC2, LAr ADC, BCM
  - CMS: RD53, HGCAL (HGCROCs, ECON-T), TOFHIR, LiTE-DTU, OT(MPA2, SSA2, CIC2.1), ETROC2
  - Others: lpGBT chipset, ALICE ITS3, H2M, BLM, ACCURATE, MALTA, …

Most common type of Support

- By order of effort required:
  1. **Functional verification:**
     - Lack of strategy from project start: Mixed signal, gate-level netlist, SEE verification?
     - Appropriate choice of methodology: Tools, randomization approach,…
  2. **Digital design (RTL) + PNR:**
     - Digital flow scripts
     - Power analysis (Voltus)
  3. **SEE robust designs (TMR):**
     - Task is often taken too late in the project → unexpected area/power increase
  4. **Transisiton to digital-on-top (DoT) designs:**
     - Characterization on Memories and full custom blocks
  5. **Analog design support**

Observations

- CHIPS used as “panic” button:
  - CHIPS activity proposed as a mid/long-term support, but has been called for projects running late (LS3 upgrades)
  - Often pushed by management but not by ASIC designers
  - Not uniform effort from CHIPS support and external groups

- CHIPS manpower is limited and long term committed:
  - All sustained support is continuously been extended
  - Some internal R&D projects delayed to free “key” engineers to give CHIPS support

- General observations on current designs:
  - Small scale prototyping strategy is not always ideal (floor-planning, verification architecture,…):
    - “Building a house is not the same as building a skyscraper”
  - Multiple and continuous prototyping doesn’t leave room to solid and robust designs:
    - “For the last 4 years we have to submit next month…”
  - Incremental prototyping requires anyway full functional verification
  - SEE design strategy seems to converge towards TMRG tool (https://tmrg.web.cern.ch/):
    - But, in general, TMRG has been used very late in the project (often skipped during prototype phase)
    - SEE testing often reveals multiple unexpected bugs
  - ASICs designers should not verify their own chips before submission:
    - Analog, digital and verification design partition is required

Summary

- CHIPS is a service aimed to give ASIC design support to HEP ASIC designers:
  - Involve experienced practitioners (EP-ESE)
  - Subcontract specialized tasks
  - Train and coach ⟵ After the COVID stop, we can resume “hot desks” for on-site coaching

- Service is hosted in the EP-ESE-ME (chips.support@cern.ch):
  - Occasional support requests are shared amongst ~11 FTE (analog, digital and verification experts)
  - 6 engineers are directly supporting design teams: 2 fellows and 4 staff members
    - In 2022 4 Staff members not from direct CHIPS resources (2 HGCAL, 2 RD53)

- Support given to many projects since 2020:
  - Occasional support in the form of dedicated reviews, specific SEE meetings, TMRG tool, …
  - Long term support to the development of ASICs for 6 detector systems: CMS Outer Tracker, CMS pixels, ATLAS pixels, ATLAS ITK, CMS HGCAL and ATLAS HGTD

- Outlook:
  - RD53 support scheduled until Q2 2023
  - HGCAL support scheduled until July 2023
  - Other designs in the near future: FastRich, Alice ITS3, Velopix2 (PicoPix), R&D…
  - Ambition to provide a support service that doesn’t need to run in panic mode