

Irradiation at CHARM of a HL-LHC prototype board for the CMS Muon DT On detector electronics based on the PolarFire FPGA

2 OBDT-v1 boards

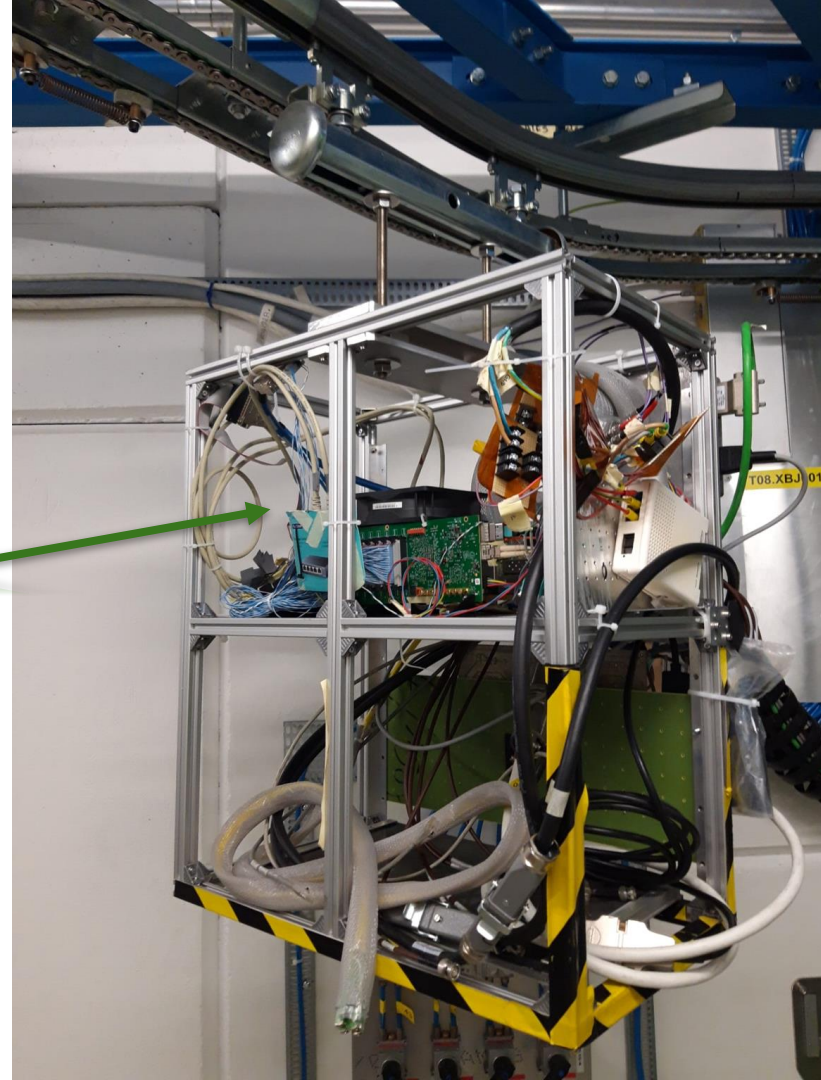
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(CIEMAT)



MINISTERIO
DE CIENCIA
E INNOVACIÓN

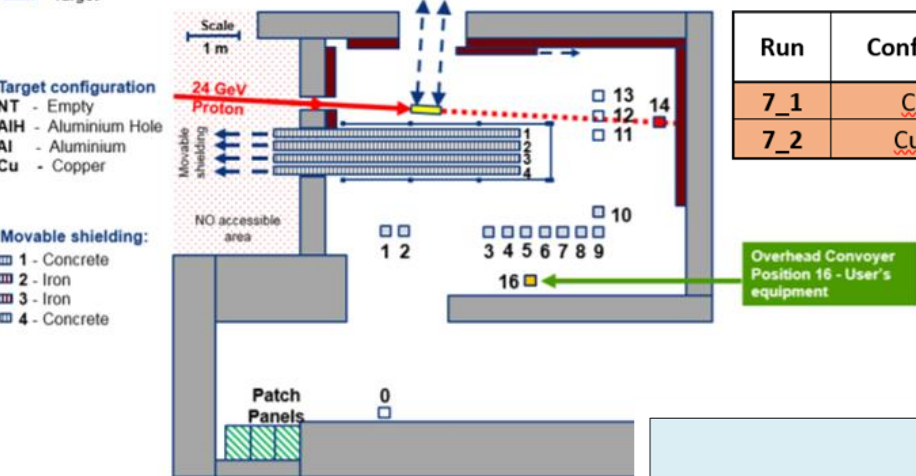


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CHARM FACILITY AND DOSIMETRY

Target



Run	Configuration	POT	TID [Gy]	HEH Fluence [cm ⁻²]	ThN Fluence [cm ⁻²]	1MeV [cm ⁻²]
7_1	CuOOIC	1.54E+15	1.7	4.99E+09	3.76E+10	5.30E+10
7_2	CuOOOO	1.93E+16	108.1	3.28E+11	5.99E+11	1.84E+12

~12 days



- Dosimetry provided by CHARM facility through [this report](#).
- Thanks to M. Brucoli and S. Danzeca for providing data vs. time.
- Most of the time without shielding, but for the first night with the CuOOIC shielding
 - 1 % of the dose received at lower rate (1/5 of the TID rate), larger relative fraction of neutrons.

RADIATION LEVEL	Target inside 03/11/2021 17:23
	Configuration change 12-11-21 16:40
Dose (Gy)	109.8
HEH fluence (cm ⁻²)	3.33·10 ¹¹
ThN fluence (cm ⁻²)	6.37·10 ¹¹
1MeVneq fluence (cm ⁻²)	1.89·10 ¹²
R factor (CuOOIC)	7.54
R factor (CuOOOO)	1.83
Total POT*	2.08·10 ¹⁶

*POT is the total number of protons hitting the target.

The OBDT (On-detector Board for Drift Tubes)

Time digitization (~ 1 ns) of DT cells

Muon DT electronics



OBDT v1:

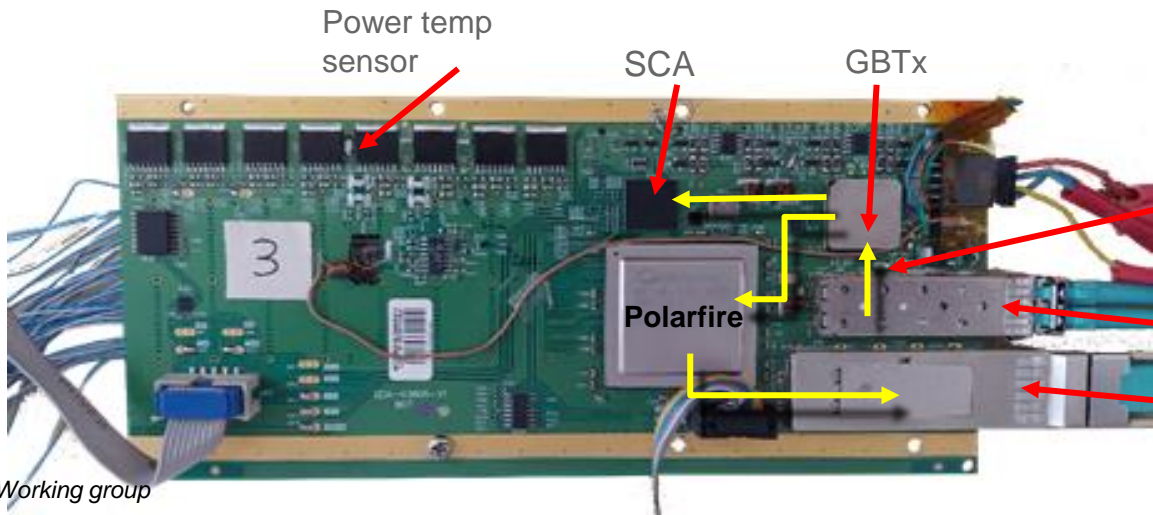
- 240 input differential channels
- 3.3V and 5V power (linear regulators)
- CERN's GBTx for communication
- CERN's SCA chip for slow control and monitoring
- Microsemi Polarfire FPGA (MPF300T-1FCG1152E)
 - Time digitization through ISERDES
 - Buffer and data funneling
 - Data transmission through GBTx protocol
 - elink for fast synchronization and slow control

PUFO fw:

- OBDT v1 board but with a different firmware
- Firmware from OBDT modified to use the **input signals as output signals**
- Hits are produced at a fixed value with respect to the arrival of the BC0 (117 signals GPIO)
- Rest of the logic is the same as the OBDT

Firmware included
TMR in logic and
CRC in RAMs

(nothing on iserdes
and TX/RX)



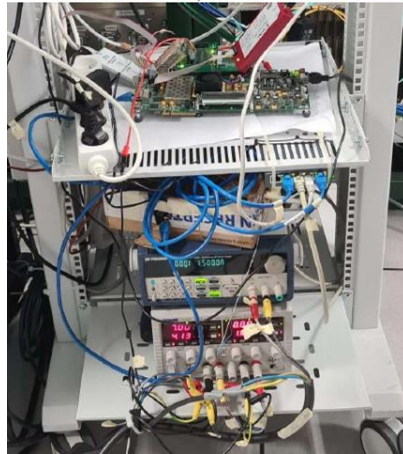
Optics
Temp
sensor

SFP+ (TCDS, clock and
synchronization commands)

QSFP (output readout
data in GBTx protocol but
from FPGA)

Irradiation Test Stand

- Backend trolley in the control room



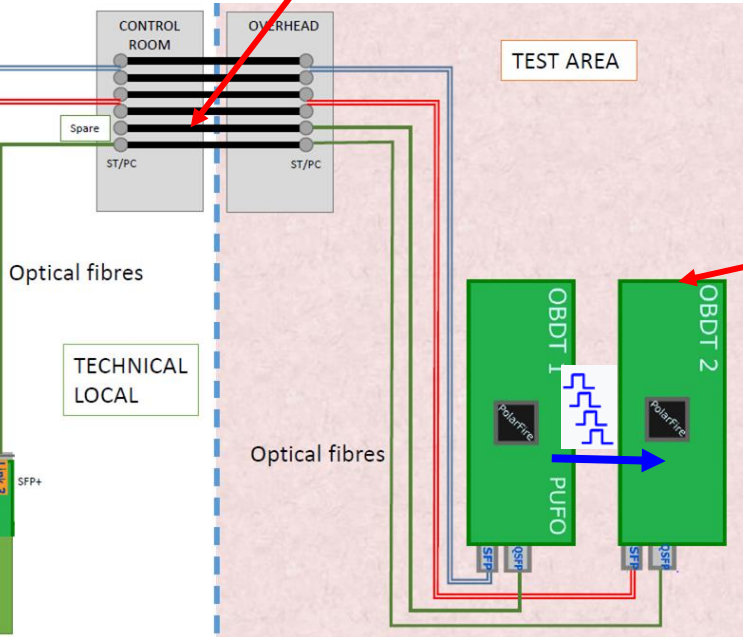
- VC707 evaluation board
- FM-S14 optical expander
- XM105 for copper link
- Rasp. pi for remote reconfiguration
- Custom PCBs for voltage translation



LXI standard
(Ethernet)



IPBUS
(Ethernet)



- Hits were sent from PUFO to OBDT
- OBDT time digitized and forward to VC707 simultaneously through optical link and copper link



- Patch panels for interconnection to the bunker

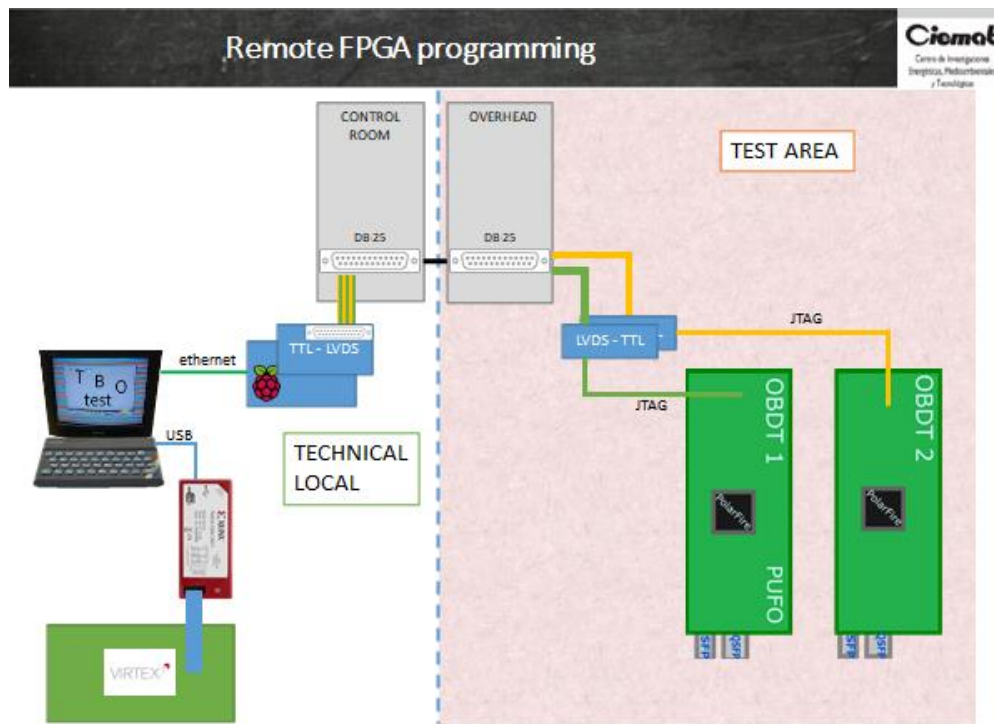
- Overhead conveyor (mock up)



POLARFIRE FPGA FIRMWARE's VERIFICATION

- We built a system to program and verify remotely the Polarfire's FPGAs firmware (that could cope with the 35 meters which prevented Flashpro/USB cables or expanders)
- Remote FPGA verify worked fine before the radiation test (bunker zone)
- First time we tried a verify during radiation was on Friday Nov. 5th at 13:00, **after 15.55 Gy, and firmware verification was NOT working.**
- IDCODEs were being read properly but the verification was failing at 66% and 45% of the process on each FPGA respectively. Same issue happened a couple more times we tried (some times not at 66% but at other values)
- However at the end of the irradiation period we were capable of loading the **firmware remotely so the programming system seemed to work fine after 109,8 Gy** (though still the verify was incorrect)

Raspberry pi running Direct C libraries from Microsemi+ custom TTI to LVDS and LVDS to TTL converters (DS90LV048 and DS90LV047 had already been validated under radiation)



Polarfire SEU-reference test

A reference logic was implemented both in OBDT and PUFO to obtain SEU values comparable to the ones reported in the literature[ref]

Firmware logic structures of the SEU reference test:

- FF All 1s : Flip-flop chain feed with 1s
- FF All 0s : Flip-flop chain feed with 0s
- CKBRD 40 MHZ: Flip-flop chain feed with a fast checkerboard 1010101 @40 MHz
- CKBRD 10 MHZ: Flip-flop chain feed with a fast checkerboard 111100001111000011110000 @ 40 MHz
- LSRAM: Errors detected in 17 bit words in a 2^{17} positions RAM memory. Errors detected when scrubbing all the RAM.

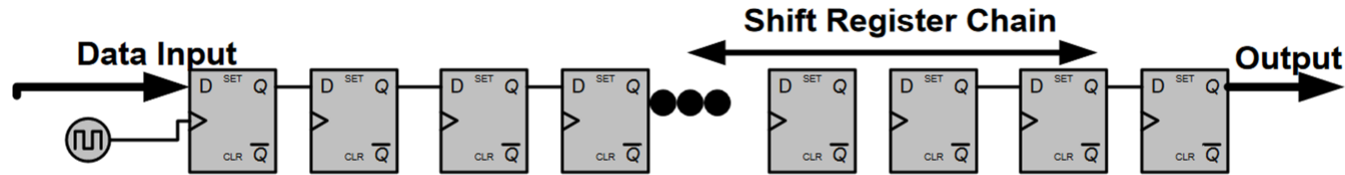


figure 13: Traditional Shift Register only contains sequential logic.

Polarfire SEU-reference test

Unfortunately there was a problem with the logging of the data until November 6th and this reference test was not working during the low dose period

Other periods where the monitoring was not working have also been removed.

	Total integrated dose	Seu_test integrated dose
Dose (Gy)	109,8	79,82
HEH fluence (cm-2)	3,33E+11	2,42E+11
ThN fluence (cm-2)	6,37E+11	4,63E+11
1MeVneq fluence (cm-2)	1,89E+12	1,37E+12

	OBDT	PUFO					OBDT	PUFO	Average
	#SEUs	#SEUs		#FF or bits	Fluence (p/cm2)		Cross-section (cm2/bit)	Cross-section (cm2/bit)	Cross-section (cm2/bit)
CKBD 40 MHz	60	71		4096	2,42E+11		6,05E-14	7,16E-14	6,61E-14
CKBD 10 MHz	33	25		4096	2,42E+11		3,33E-14	2,52E-14	2,93E-14
FF All 1s	16	20		4096	2,42E+11		1,61E-14	2,02E-14	1,82E-14
FF All 0s	29	22		4096	2,42E+11		2,93E-14	2,22E-14	2,57E-14

Cross section

$$\sigma(cm^2/bit) = \frac{\#SEUs}{\phi(p/cm^2)*\#bits}$$

Polarfire SEU-reference test

LSRAM error counters:

- Instantiated one LSRAM with 2^{17} positions of 17 bit word each.
- The firmware was scrubbing all the RAM memory and counting when the word was not the one

	OBDT	PUFO				OBDT	PUFO	Average
	#SEUs or #MBUs	#SEUs or #MBUs	#FF or bits	Fluence (p/cm2)		Cross-section (cm2/bit)	Cross-section (cm2/bit)	Cross-section (cm2/bit)
LSRAM SEUs	19414	16673	2228224	2,42E+11		3,60E-14	3,09E-14	3,35E-14
LSRAM MBUs	1	2	2228224	2,42E+11		1,85E-18	3,71E-18	2,78E-18

- Few times we could find that the LSRAM error counter has a very high value, manifested as a crazy running of the SEU counter.
- Could be SEFI but in reality the rest of the system was working fine. More likely is part of the logic that affects the SEU-reference counters
- We are cataloguing those as MBU (Multiple Bit Upsets) or larger logic upsets

Polarfire SEU-reference test: LSRAM results

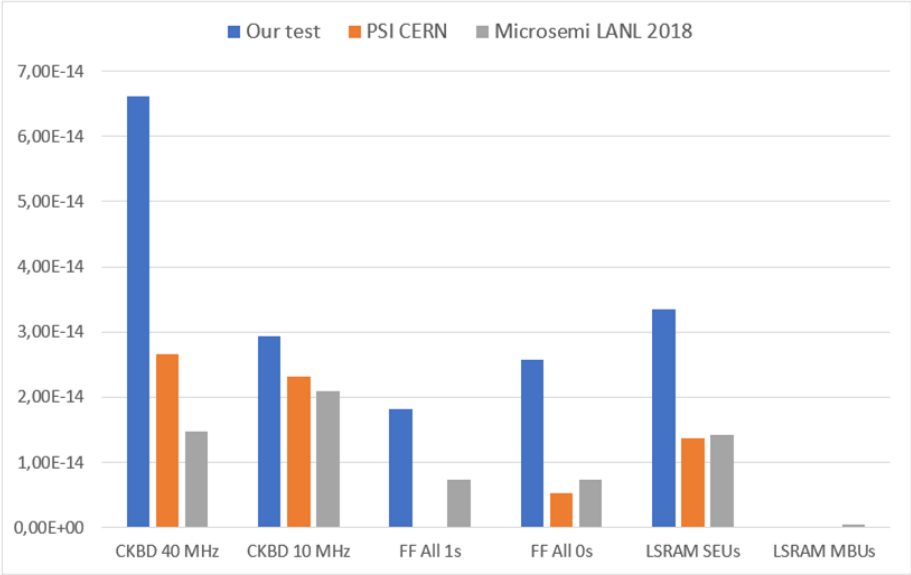
Qualitative comparison with other irradiation tests on Polarfire devices with same or very similar reference logic:

Microsemi results can be found: >10 MeV neutron field

https://www.microsemi.com/document-portal/doc_download/1244460-polarfire-neutron-see-test-report

PSI CERN results can be found: 200 MeV protons

<https://edms.cern.ch/ui/#!master/navigator/document?D:100764438:100764438:subDocs>



	Our test	PSI CERN	Microsemi LANL 2018
	Cross-section (cm2/bit)	Cross-section (cm2/bit)	Cross-section (cm2/bit)
CKBD 40 MHz	6,61E-14	2,66E-14	1,47E-14
CKBD 10 MHz	2,93E-14	2,31E-14	2,09E-14
FF All 1s	1,82E-14		7,39E-15
FF All 0s	2,57E-14	5,31E-15	7,39E-15
LSRAM SEUs	3,35E-14	1,37E-14	1,42E-14
LSRAM MBUs	2,78E-18	< 9,5e-18	5,58E-16

Caveats: different particles, energies, different clock frequencies, different firmware implementations...

FLASH MT25QL01GBBB8ESF-0SIT

* Before CHARM:

we could reload the Polarfire with the fw stored on the flash, it worked fine (we load a different fws and verify that they have changed)

* During CHARM:

we did not load the Polarfire because we did not want to break the test in the middle of the irradiation period

* Last day of CHARM (Nov 12th):

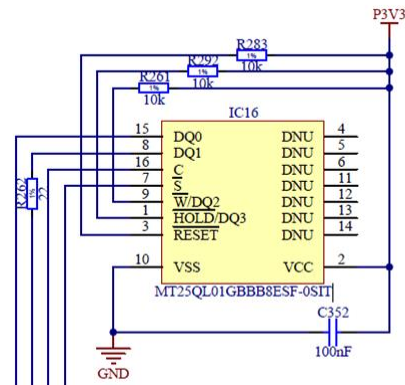
Tried to load the Polarfire from the Flash:

- it did not work during radiation time
- it did not work once radiation was over

Polarfire is loaded in Master mode. It could be the Polarfire logic that was not working or it could be the flash being dead.

However the Polarfire could be programmed through JTAG at the end of the irradiation.

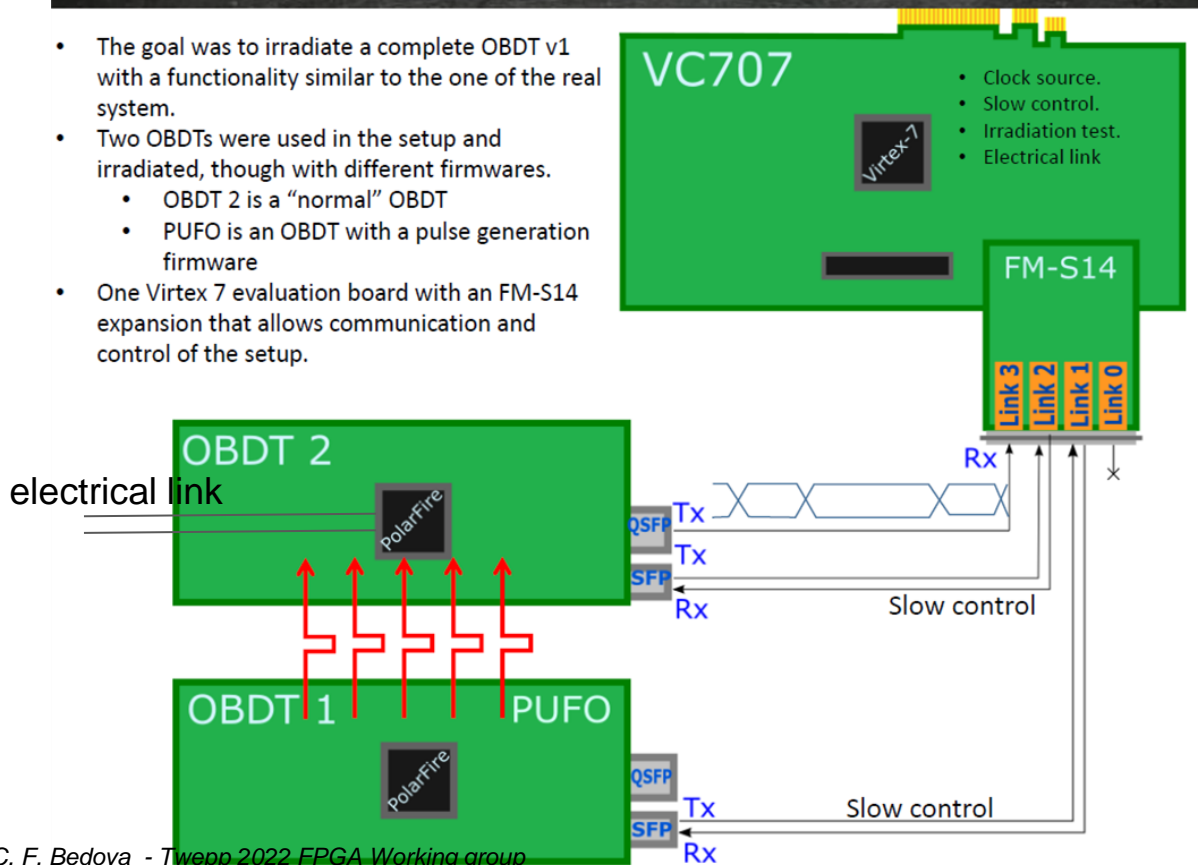
Summary, the mechanism did not work after the full irradiation (109.8 Gy). Further radiation tests devoted specifically to the FLASH will be required.



Polarfire & OBDT: Timing test counters

Test Stand Overview

- The goal was to irradiate a complete OBDT v1 with a functionality similar to the one of the real system.
- Two OBDTs were used in the setup and irradiated, though with different firmwares.
 - OBDT 2 is a “normal” OBDT
 - PUFO is an OBDT with a pulse generation firmware
- One Virtex 7 evaluation board with an FM-S14 expansion that allows communication and control of the setup.



Hit errors counters:

- an expected hit it is not received,
- the hit is received with wrong timing
- or there is more than one hit received in a time window.

Triple counters monitoring:

- A: Hits read through link 3 from OBDT 2 (normal optical readout) and error counters implemented in the VC707
- B: Error counters implemented in Polarfire and read through link 3
- C: Error counters implemented in Polarfire and read through an electrical link

Dose collected during the test at CHARM

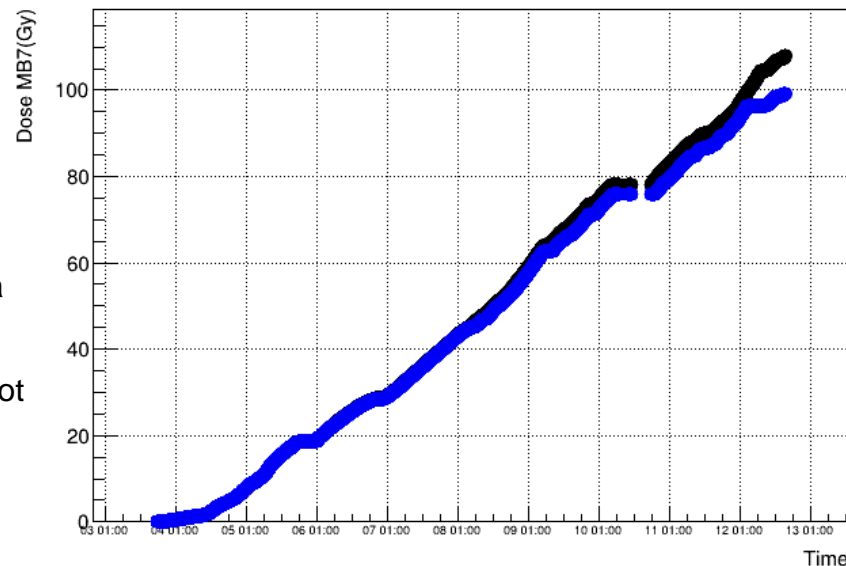
November 3rd, 2021 to November 12th, 2021

	Total	With good monitoring
Dose (Gy)	109,80	93,96
HEH (High Energy Hadrons) (cm-2)	3,33E+11	2,90E+11
Total Hadrons (cm-2)	6,37E+11	5,54E+11
1 MeV n eq (cm-2)	1,89E+12	1,64E+12

During this period (10 days 24h shift) there are times in which the data is not reliable and has been removed.

Basically there are the following causes in which the monitoring was not operational (efficiency 85%):

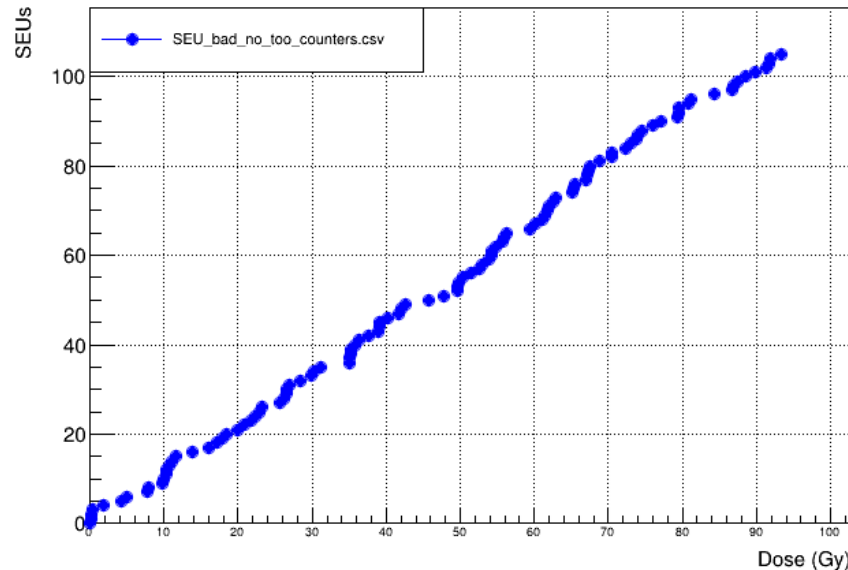
- Monitoring routines crashed but we did not realize from the dashboard or not properly launched
- Measurement of optical power and wrong interconnection afterwards
- Periods where verify or tests on purpose were being done
- Periods where the SFP+ that recovered the clock was not working properly and the clock was unstable



Black: Total integrated dose
Blue: Dose with good monitoring

Polarfire & OBDT: Timing test counters:

- Missing hit, wrong timing or duplicated hit all considered as failures of SEU type (could be in the OBDT or in the PUFO)
- Typically all of the SEUs affected all of the channels simultaneously, meaning, the SEU was not on the time measurement itself but in the BC0, reset distribution or similar logic.
- If all channels equal errors simultaneously => 1 SEU
- Crosschecked the counters seen from the three different monitoring paths, coherent result.
- Electrical path allowed to identify some burst of errors in the optical path that were not real SEUs (clearly due to link instabilities) (17 events)
- 107 real SEUs counted through all the irradiation campaign The cross section obtained with this number of failures and the amount of logic contained in the Polarfire firmwares is $2.33 \cdot 10^{-15} \text{ cm}^2/\text{bit}$



Caveat: the SEUs from the TX at the Polarfire are not accounted for in this test since optical links were not reliable. The rest of the logic could be considered very similar to the firmware to be used during HL-LHC (including TMR in logic and CRC mechanisms in RAMs).

Polarfire extrapolation of SEUs to HL-LHC for DT

	All 840 boards	MB1s externals (72)	MB4s (240)	MB3s (240)
#failures/system	107	107	107	107
#failures/board	53,5	53,5	53,5	53,5
#failures for 840 boards	44940	3852	12840	12840
Total dose integrated at CHARM (Gv)	93,96	93,96	93,96	93,96
Dose at HL-LHC (Gy)	0,505	2,10	0,59	0,06
Dose factor	186,06	44,74	159,25	1566,00
#failures all HL-LHC	241,54	86,09	80,63	8,20
#failures/year	24,15	8,61	8,06	0,82
#failures/day (100 operating days/year)	0,24	0,09	0,08	0,01
#days between failures	4,14	11,62	12,40	121,963

Summary

- The OBDT v1 with a firmware similar to what expected in HL-LHC has been tested under radiation at CHARM
 - The electronics could be very similar though we had commercial optical transceivers (dominant source of problems in this test)
- No latch-up has been seen in the Polarfire FPGA
- No loss of configuration has been seen.
- No SEFI has been identified (electrical FF test has been operating correctly all the time).
- Major sensitivity observed in the Optical transceivers and in the Flash
- Cross sections have been measured in a benchmark system and with the expected firmware. Numbers are adequate for our application.
- Extrapolated number of errors to HL-LHC is acceptable for our application. (~4 days without SEU failures for the full system (it contains 1000 boards))

The list of the main integrated circuits part numbers which have been verified during the OBDtv1 radiation test is summarized here:

Part number	Manufacturer	Package	#/board	Function
MPF300T-1FCG1152E	MICROSEMI	BGA1152	1	PolarFire FPGA, 512 I/O, 300000 Logic Elements, 1152-Pin FBGA, Extended Commercial Grade
GBT-SCA_REV 6.2	CERN	BGA196	1	Slow Control Adapter ASIC for the GigaBit Transceiver ASIC (GBT)
GBTX ASIC V0.1	CERN	BGA400	1	GigaBit Transceiver ASIC (GBTX)
MT25QL01GBBB8ES-F-0SIT	MICRON TECHNOLOGY	SOIC16	1	1Gbit (128MB), 1.8V, Multiple I/O Serial Flash Memory
SN74LVC2T45DCTT	TEXAS INSTRUMENTS	TSSOP8	1	Dual-Bit Dual-Supply Bus Transceiver With Configurable Voltage Translation and 3-State Outputs
LTC2052HVCS#PBF	LINEAR TECHNOLOGY	SOIC14	1	Quad Zero-Drift Operational Amplifier
LM340MP-5.0/NOPB	TEXAS INSTRUMENTS	SOT223	1	5V, 1A Positive Voltage Regulators
MM3Z5V6B	ON SEMICONDUCTOR	SOD-323F	1	5.6V 200mW Zener Voltage Regulator
MM3Z12VB	ON SEMICONDUCTOR	SOD-323F	1	12V 200mW Zener Voltage Regulator
1N5819	FAIRCHILD SEMICONDUCTOR	DO-41	3	40V 1A Schottky Barrier Rectifier
FXL4TD245BQX	ON SEMICONDUCTORS	QFN16	4	4-Bit Low-Voltage Dual-Supply Signal Translator with Configurable Voltage Supplies and Signal Levels and 3-STATE Outputs
MIC69502WR	MICROCHIP TECHNOLOGY	S-PAK-7	8	Adjustable Low VIN, Low VOUT uCap LDO Regulator
POK1.1206.2P.A	IST (INNOVATIVE SENSOR TECHNOLOGY)	0805	2	-50°C to 150°C, 100 Ohm at 0°C, SM Platinum Temperature Sensor

Table 1: Main components list of the OBDtv1

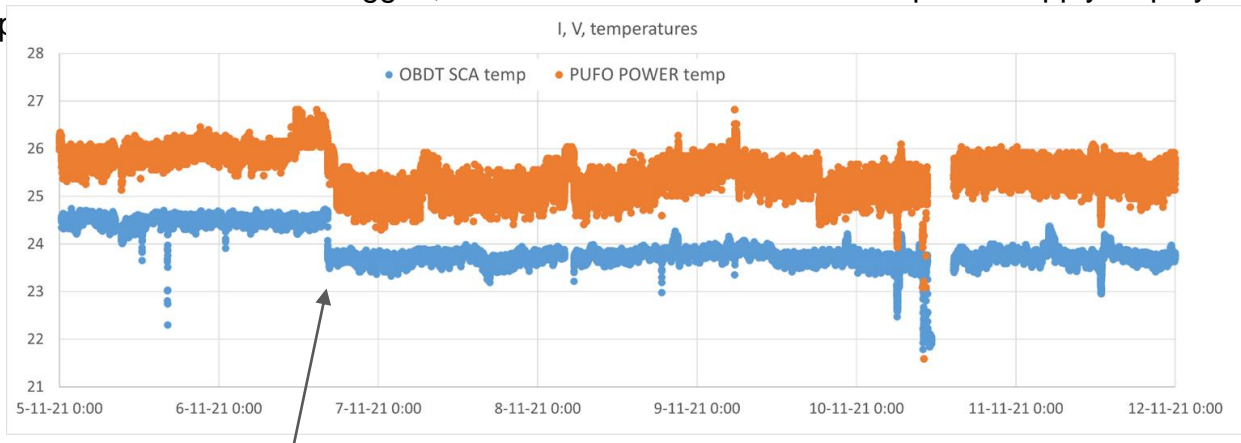
FANS

Two fans were installed in the setup to guarantee redundancy so that the cooling will work during the test (without cooling the boards had to be switched off)

- One AC fan: Axial AC EBMPAPST 4650N
- One DC fan (max 12 volts): DC brushless AFC1212DE delta electronics

Temperature was relatively stable, no issues of fans not working or degrading observed

The current of the DC fan was not logged, but the current measured on the power supply display did not increase over the irradiation



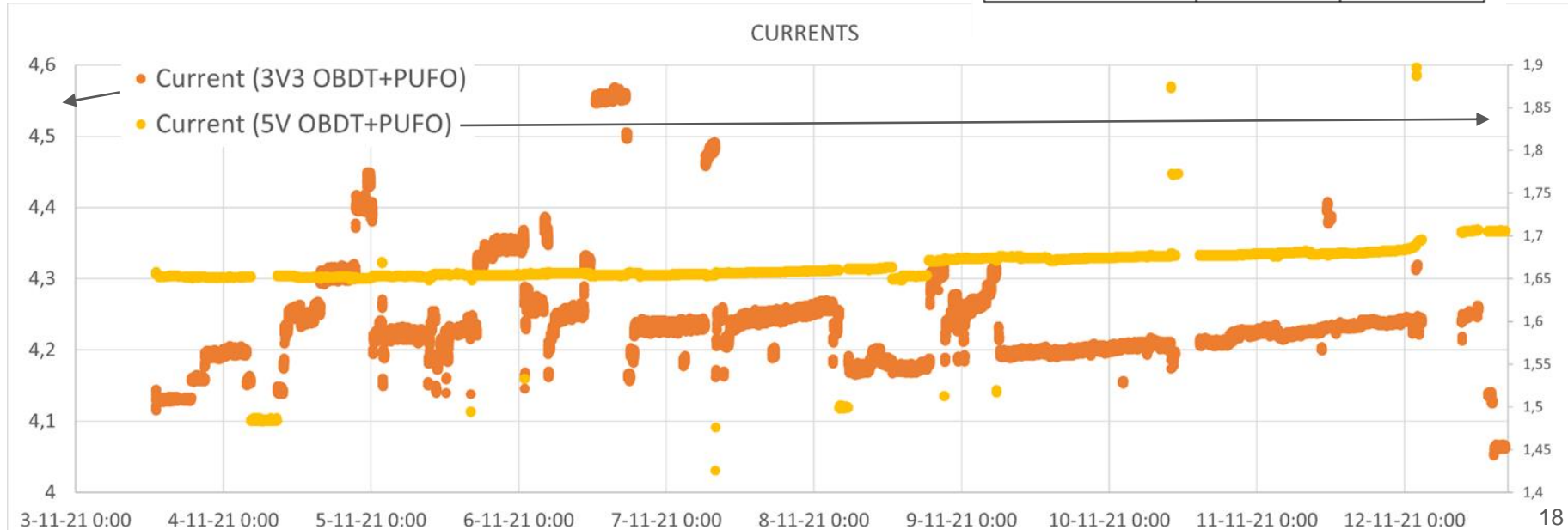
Temperature drop due to increasing DC fan from 8 V to 11 V

Both fans worked satisfactorily throughout the test (109.8 Gy) and both remained operational

POWER SUPPLY CURRENTS

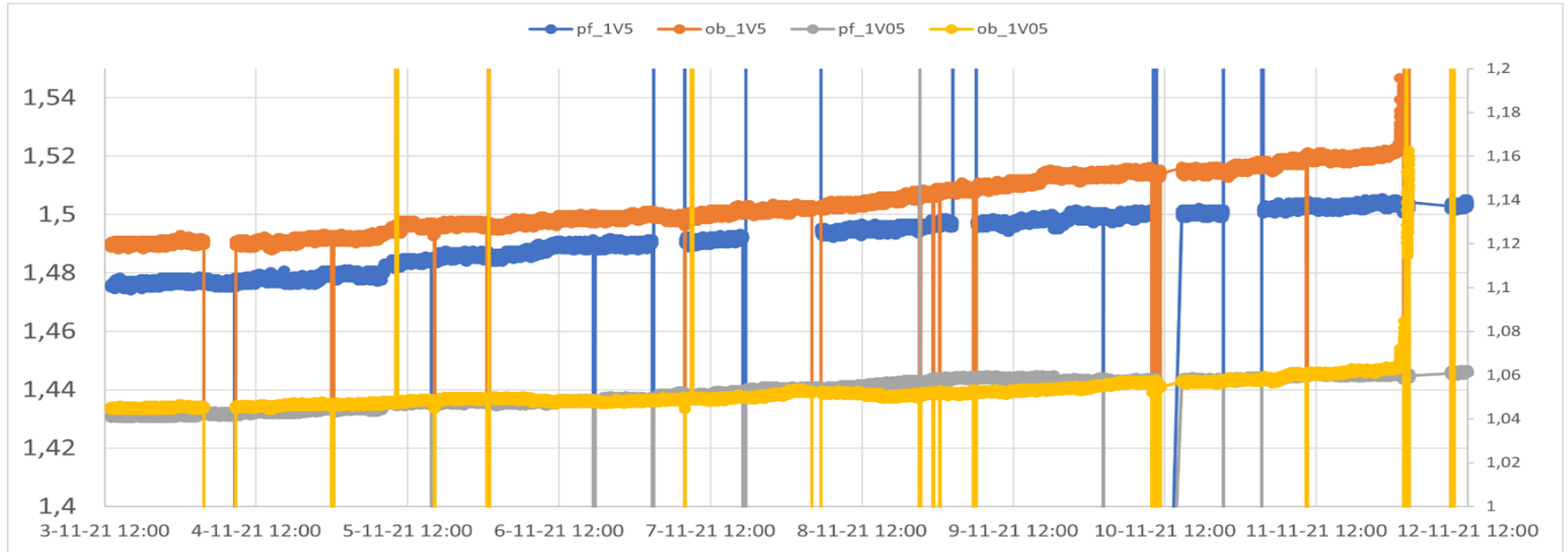
- Besides of the sporadic increases related with malfunctioning of the optical modules, the average current increase in the system has been approximately a 3% in both power rails.
- (Regulators GND current?)

	3V3 CURRENT	5V CURRENT
START of the irradiation period CURRENT (AMPS)	4,127	1,653
END of the irradiation period CURRENT (AMPS)	4,256	1,705
TOTAL CURRENT INCREASE (mA)	129	52
% CURRENT INCREASE	3,13	3,15



POWER SUPPLY VOLTAGES

- Voltages at the output of the Micrel MIC69502WR regulator also seen an increase $<1\%$ throughout the radiation period
- Compatible with previous irradiation tests of this technology



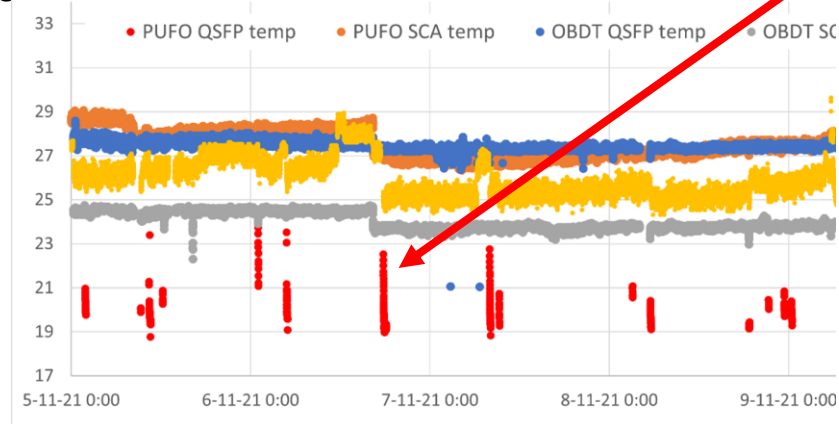
OPTICAL TRANSCEIVERS

These devices are not radiation tolerant, indeed it was clear that they were the main source of troubles during the test

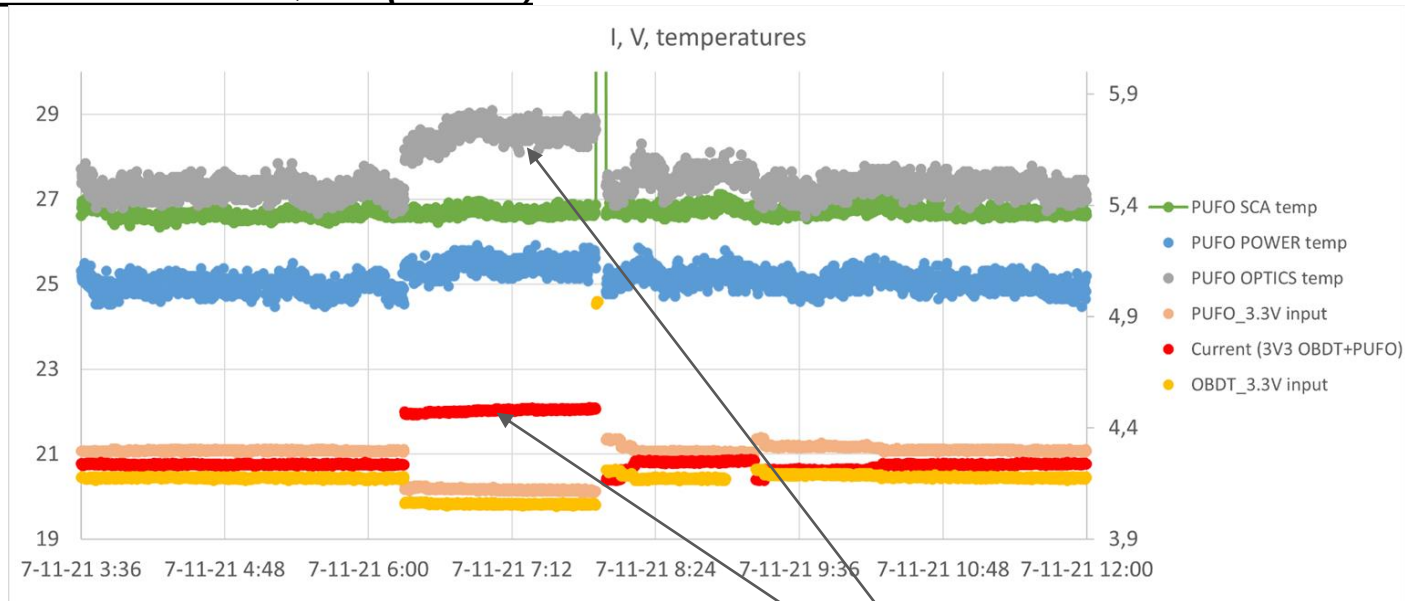
An parallel electrical link was developed to read Polarfire (OBDT and PUFO) status from remote.

Commercial optical transceivers installed on the OBDTs:

- SFP+ OBDT: AA13323A3ME (Avago)
- SFP+ PUFO: FTLX8574D3BCL (Finisar)
- QSFP OBDT: FTL414QB2C (Finisar), beige handle
- QSFP PUFO: FTL410QD4C (Finisar), orange handle. Internal I2C temperature reading failed since the beginning of the test



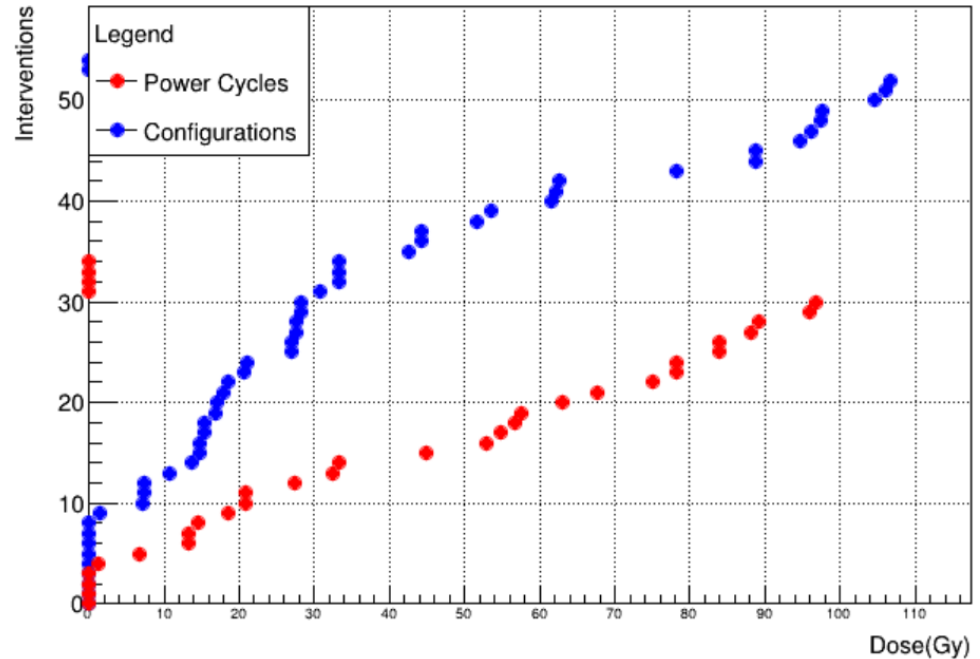
QSFP PUFO: FTL410QD4C (Finisar)



- PUFO optics' temperature in grey (read from a PT1000 which is nearby) has increased significantly following the input currents.
- This temperatures increases are correlated with **increases in the input current** (red) that, among others, serves the QSFP
- Total current is increased by 0.4 A. This increases the voltage drop of the incoming power cables and thus, the voltage seen at the PUFO 3.3V input is lower (though large enough for the board to operate).
- The PUFO SCA temperature is much smoother (green)
- The rest of the test metrics was unaltered during the high current period and SEUs could be measured correctly.
- Currents and temperatures recover after a power cycle

Manual Interventions: Power cycles and reconfigurations

- Power cycles (red)
 - Exclusive configurations (blue)
- All these power cycles belong to two types:
 - Interventions (17) to recover commercial optical transceivers.
 - Shifter actions without system malfunctioning (making verifies, etc)
 - If we were to operate with these optical transceivers: for a total dose of 109,8 Gy it would result in 3,67 power cycles/year. (Using the actual dose expected per chamber)
 - (Note however that the actual BER of this optical transceivers is larger than just these power cycles, so still, we would not recommend to use them)



ESTIMATION OF THE FAILURE RATE OF THE OPTICAL TRANSCEIVERS

Beyond the power cycles, made an estimation of the failure rate based on two variables (none of them is perfect):

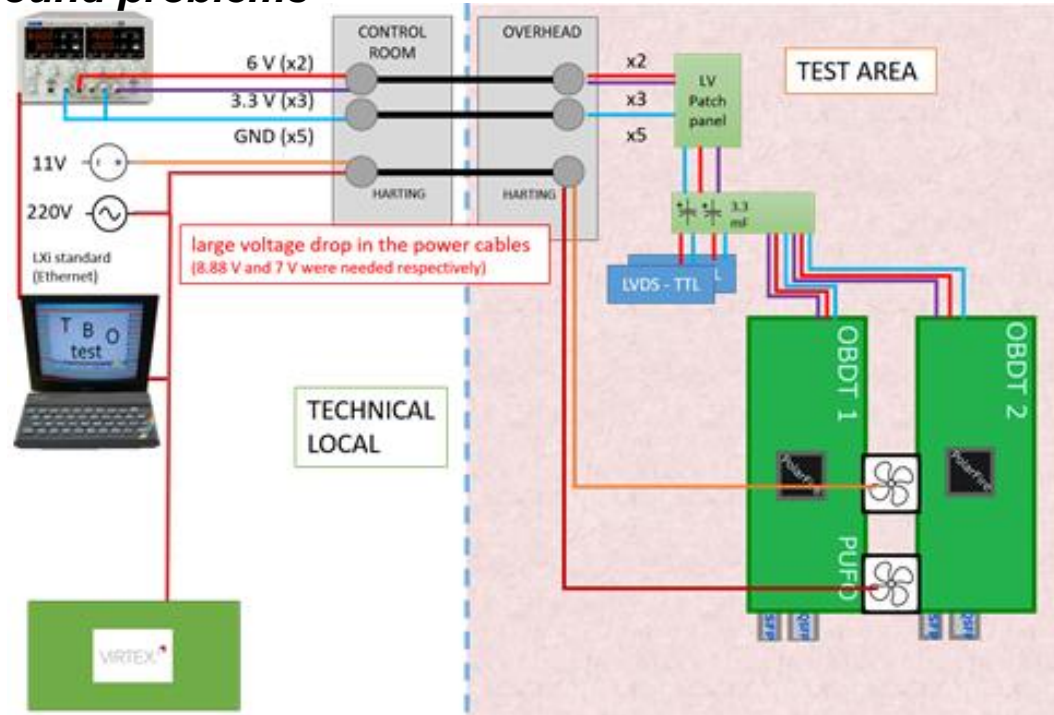
- LOS (Loss of signal) at the VC707 side, no light at the optical receiver
- RX_data_error variable provided by the GBT VHDL as data received being corrected (data is then valid. This variable is only relevant during periods when LOS is ok)

			% time at 0 errors
Link 1 (SFP+ PUFO)	FTLX8574D3BCL (Finisar)	LOS 1	91,7
Link 2 (SFP+ OBDT)	AA13323A3ME (Avago)	LOS 2	90,3
Link 3 (QSFP OBDT)	FTL414QB2C (Finisar), beige	LOS 3	99,5

			% time at 0 errors
Link 1 (SFP+ PUFO)	FTLX8574D3BCL (Finisar)	rx_data_error_cntrs_1 == 0	99,5
Link 2 (SFP+ OBDT)	AA13323A3ME (Avago)	rx_data_error_cntrs_2 == 0	93,7
Link 3 (QSFP OBDT)	FTL414QB2C (Finisar), beige	rx_data_error_cntrs_3 == 0	95,1

Some of the SFP+ LOS events had some impact because the clock was lost, this data has been removed from the measurements

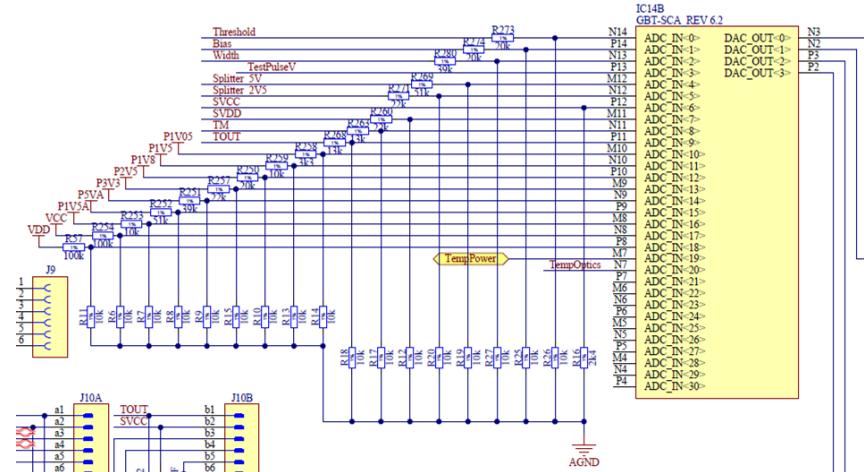
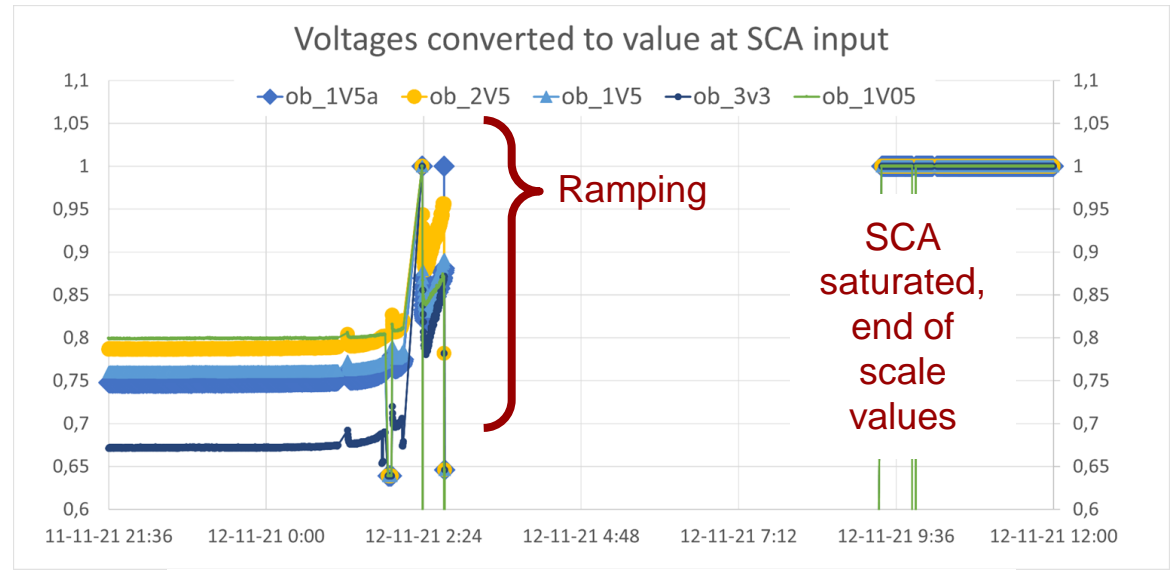
Power distribution, ground problems



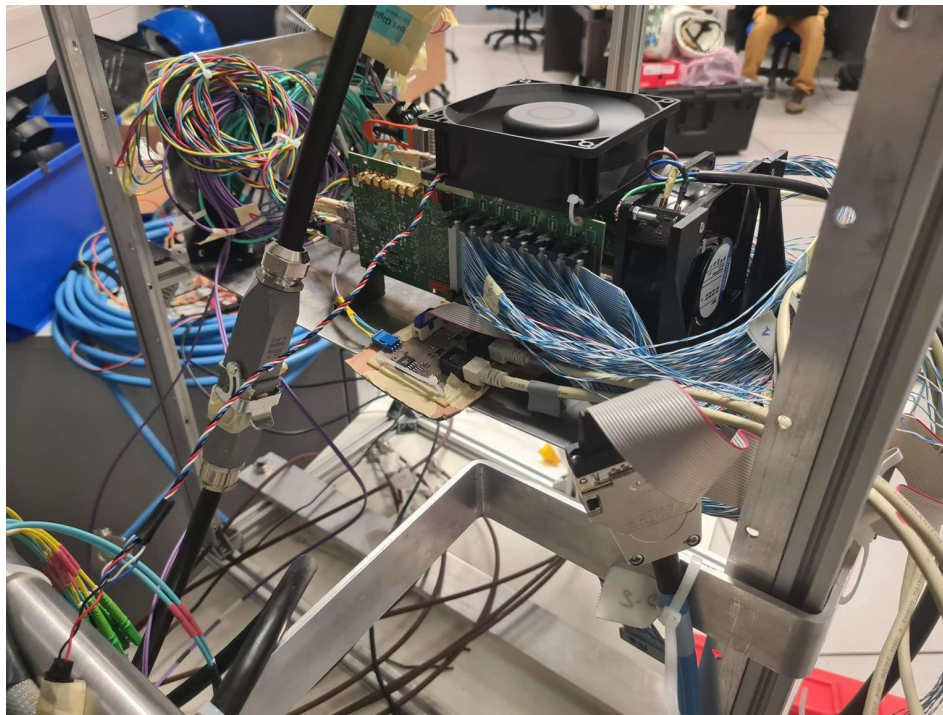
- 35 meters long cables are installed between the power supply and the OBDT boards. The section of the cables was 1.5 mm² and this implied that a significant voltage drop (maximized the number of cables that we could use)
- Voltage drop is dependent on the current and current consumption (configured and locking to the clock). Current between 1 Amp to 2.4 Amps => voltage drop from 1.3 volts to 3.2 volts
- Maximum input voltage is 6 volts for the regulators.
- Problems with the grounding for the secondary link (copper)

CERN's SCA event

- Last day (November 12th at around 02:46, after 98.77 Gy):
- Temperatures and voltages of the OBDT as measured by the SCA started to increase gradually until they reached saturation point (unphysical temperatures)
- It did not seem a real increase, currents were stable, temperature from the remote sensor was stable, it was an SCA artifact
- ADC values were incorrect but the rest of the SCA functionality was intact
- Similar behaviour as when a high voltage is present at SCA pins input and the ADC saturates.
- Post mortem analysis of the OBDT would be needed to understand why this happened

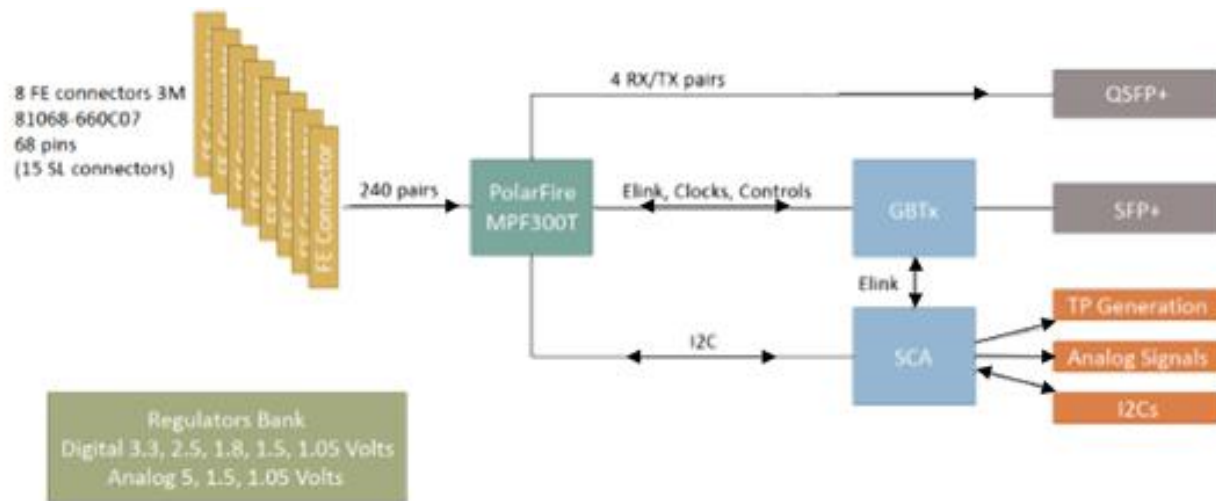
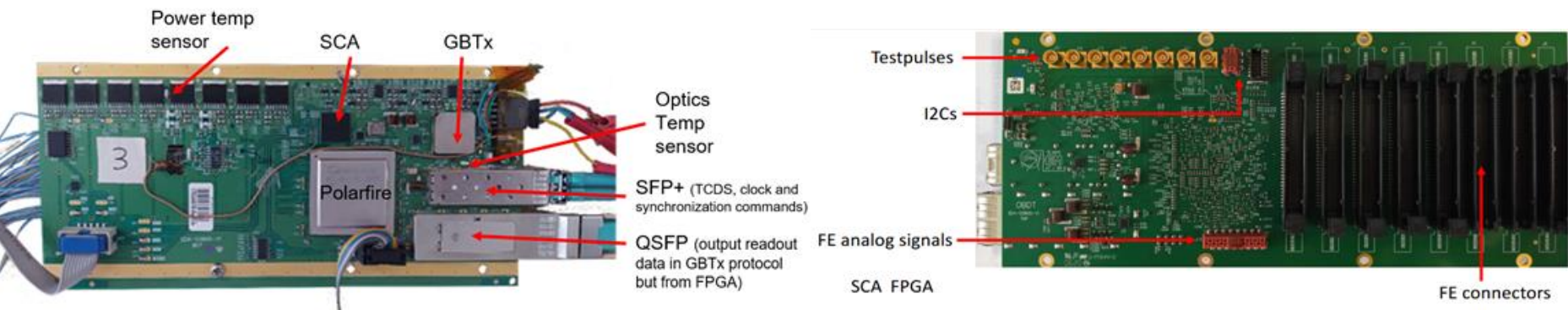


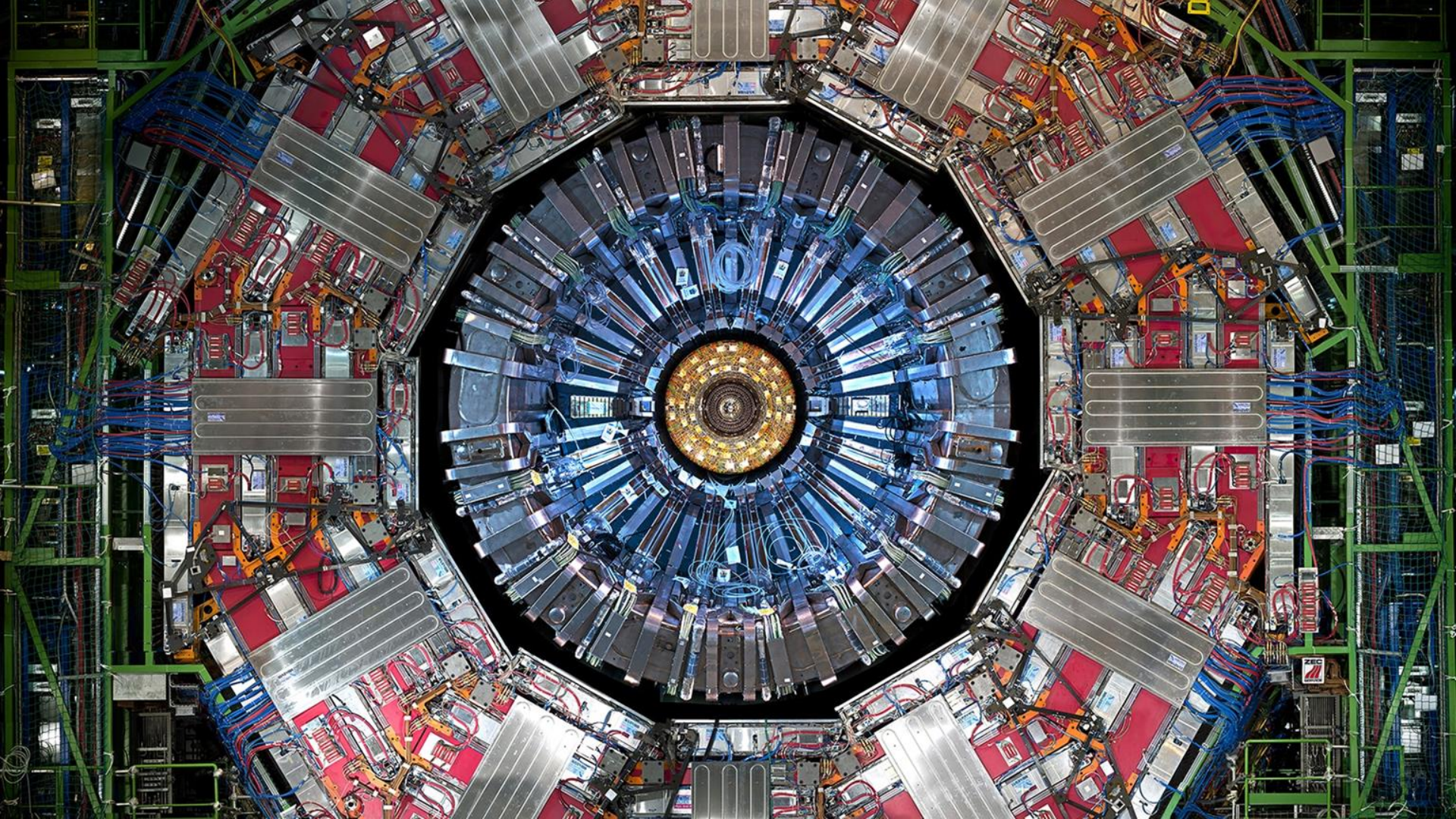
Backup



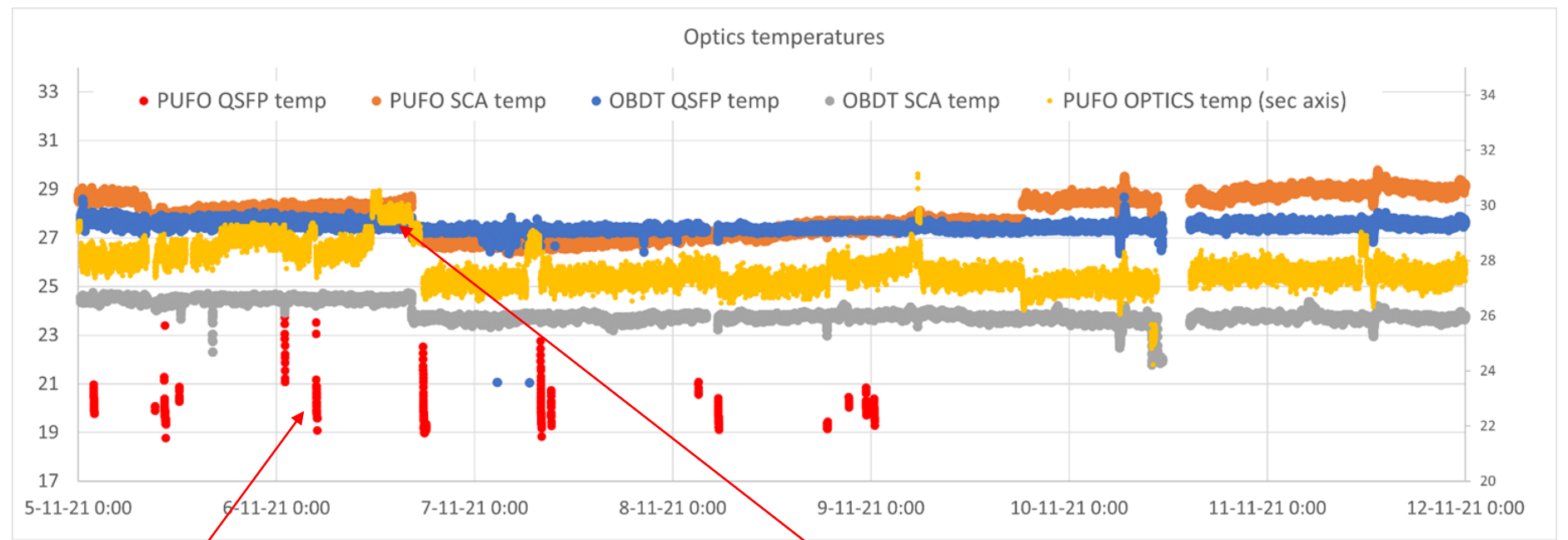
RESULTS

- Fans
- Currents, voltages, temperature. SCA event (in the backup)
- Optical transceivers
- Flash
- Polarfire firmware verification
- Polarfire: Reference SEU test:
 - Part of the OBDT and PUFO logic devoted to a specific firmware implementation used by CERN and Microsemi
 - Obtain cross-section of errors in the device and validate the irradiation performed
- Polarfire & OBDT: Timing test counters:
 - measure time digitization in all the channels every orbit.
 - Behaviour of the OBDT in standard operation mode
 - Extrapolating number of errors seen in the radiation test to the expectations during HL-LHC





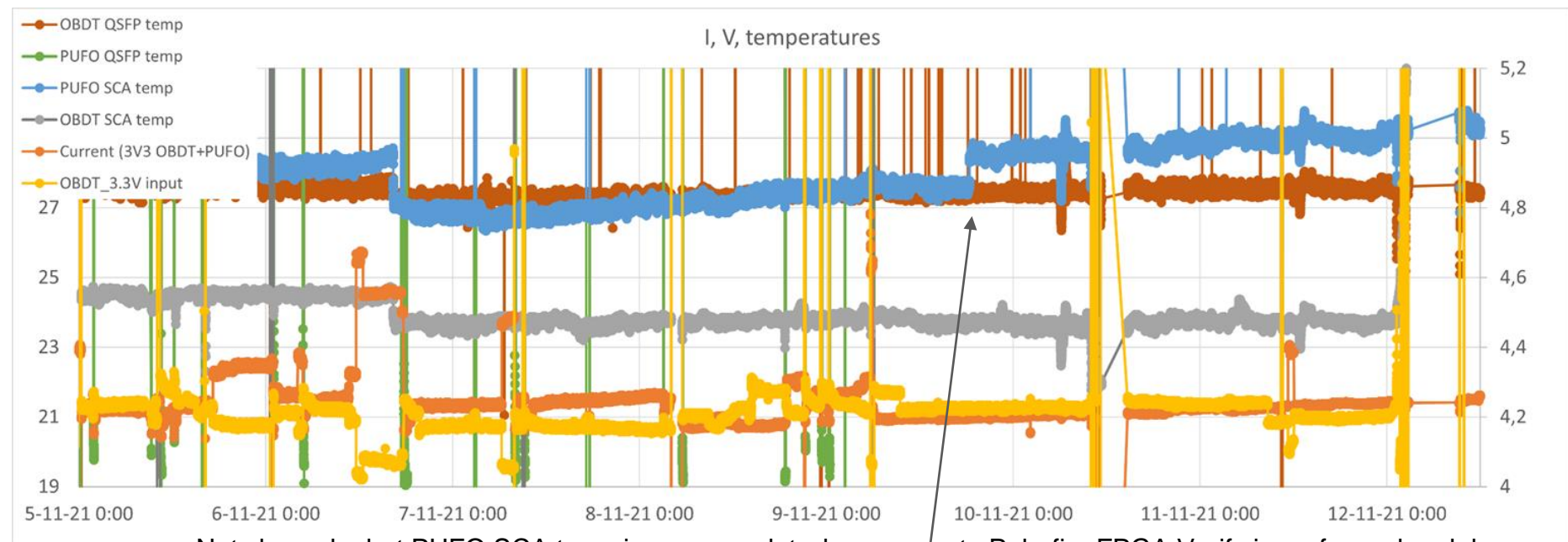
QSFP PUFO: FTL410QD4C (Finisar)



PUFO QSFP temperature reading not working. Recovered briefly just right after power cycles.

Temperature of PUFO optics had sporadic increases which seemed real (and they were correlated with total currents increases). This sensor is a PT1000 read by the SCA which is placed close to the PUFO QSFP (and to the SPF+)

POLARFIRE FPGA FIRMWARE'S VERIFICATION

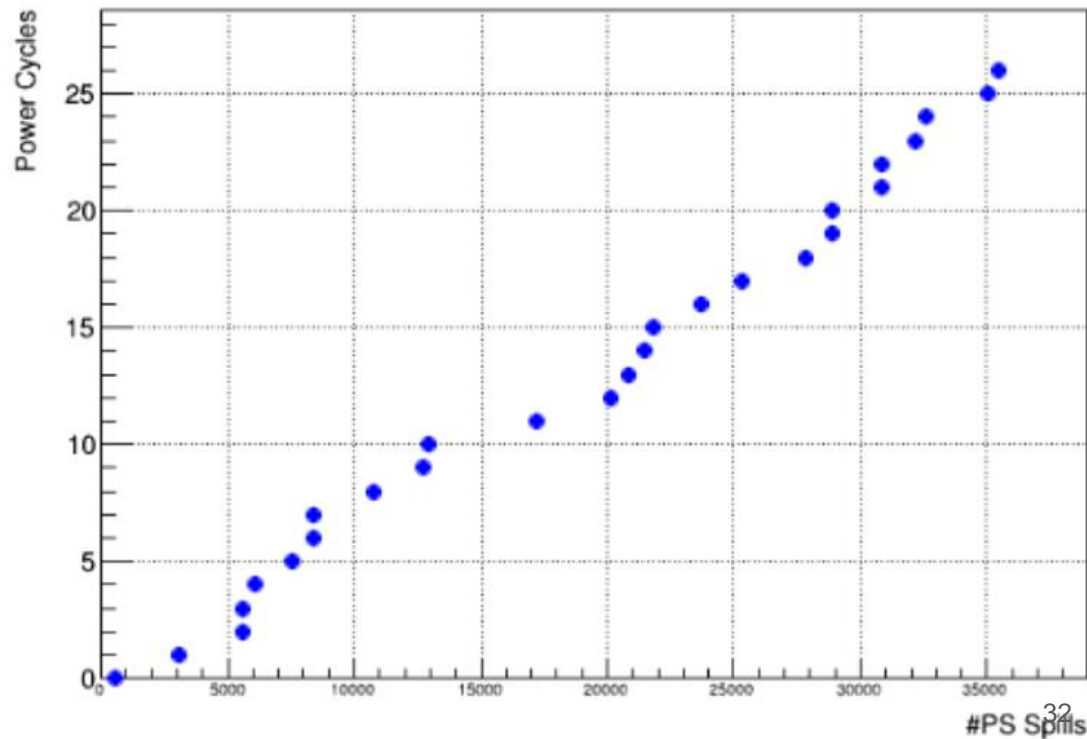


Not clear why but PUFO SCA temp increases a lot when a remote Polarfire FPGA Verify is performed and does not recover afterwards
OBDT SCA temp is not altered and no other symptom is detected

Remote FPGA verify worked fine before the radiation test (bunker zone)
First time it was tried was on Friday Nov. 5th at 13:00, after 15.55 Gy, and it was not working.
IDCODEs were being read properly but the verification was failing at 66% and 45% of the process on each FPGA respectively each time we performed it during the irradiation
However at the end of the irradiation period we were capable of loading the firmware remotely...

Manual interventions: Power cycles

- Most of the interventions (17) to recover commercial optical transceivers.
- Rest due to shifter actions (making verifies, fixing sw, etc)
- If total dose is 200 Gy (tbc) it would result in one power cycle every 4x HL-LHC dose in our hottest area.

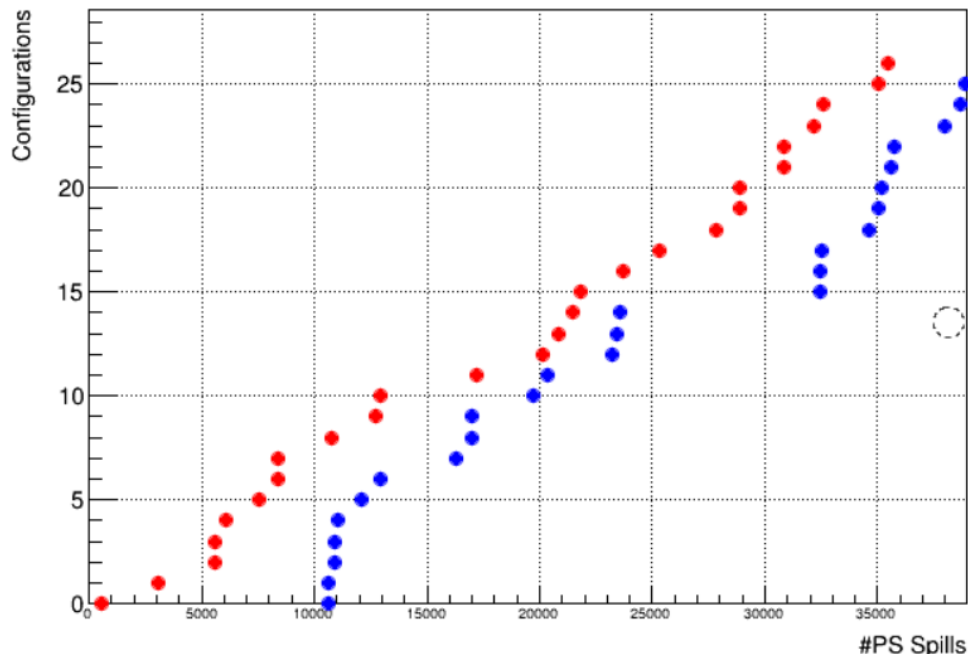


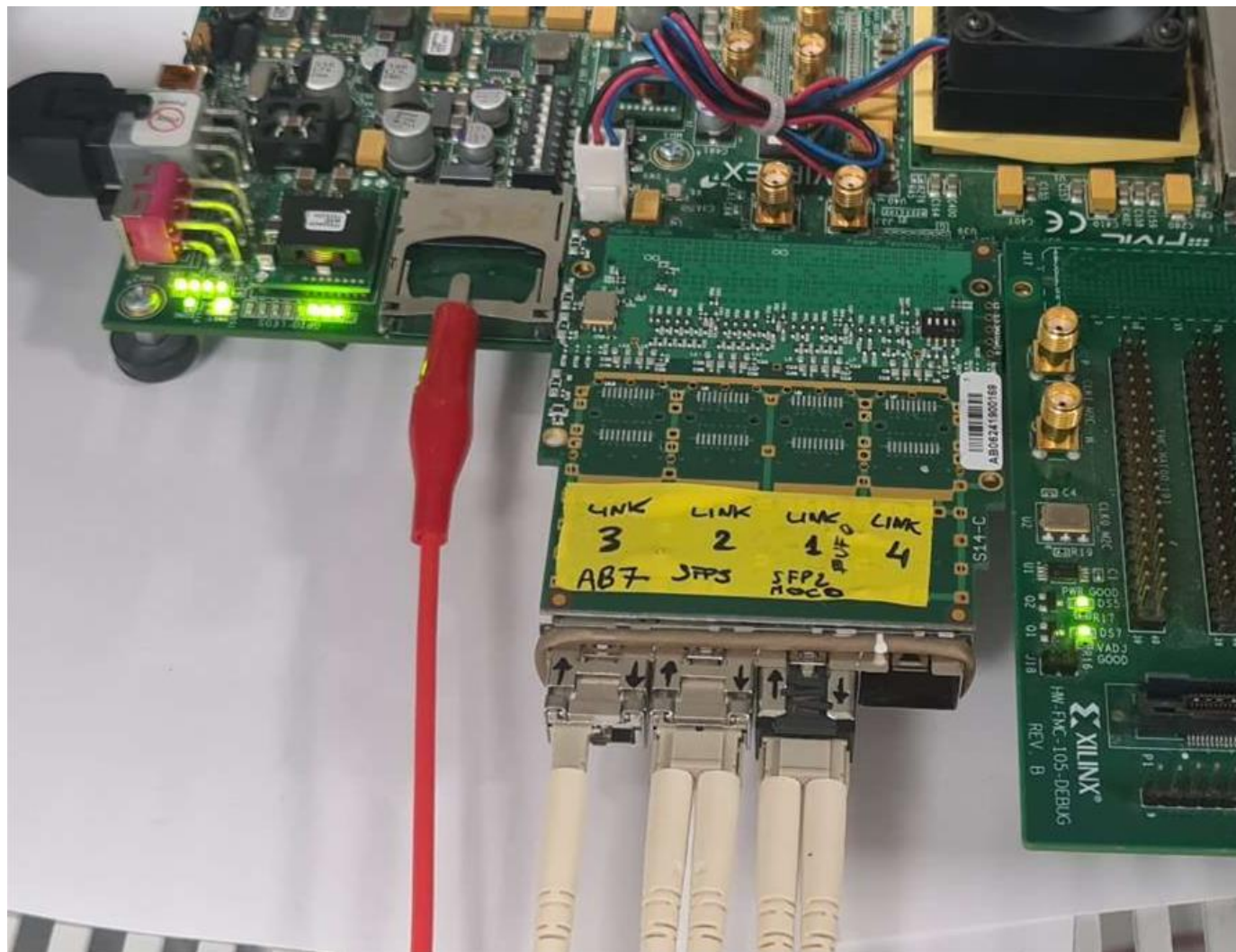
Manual interventions: Configurations

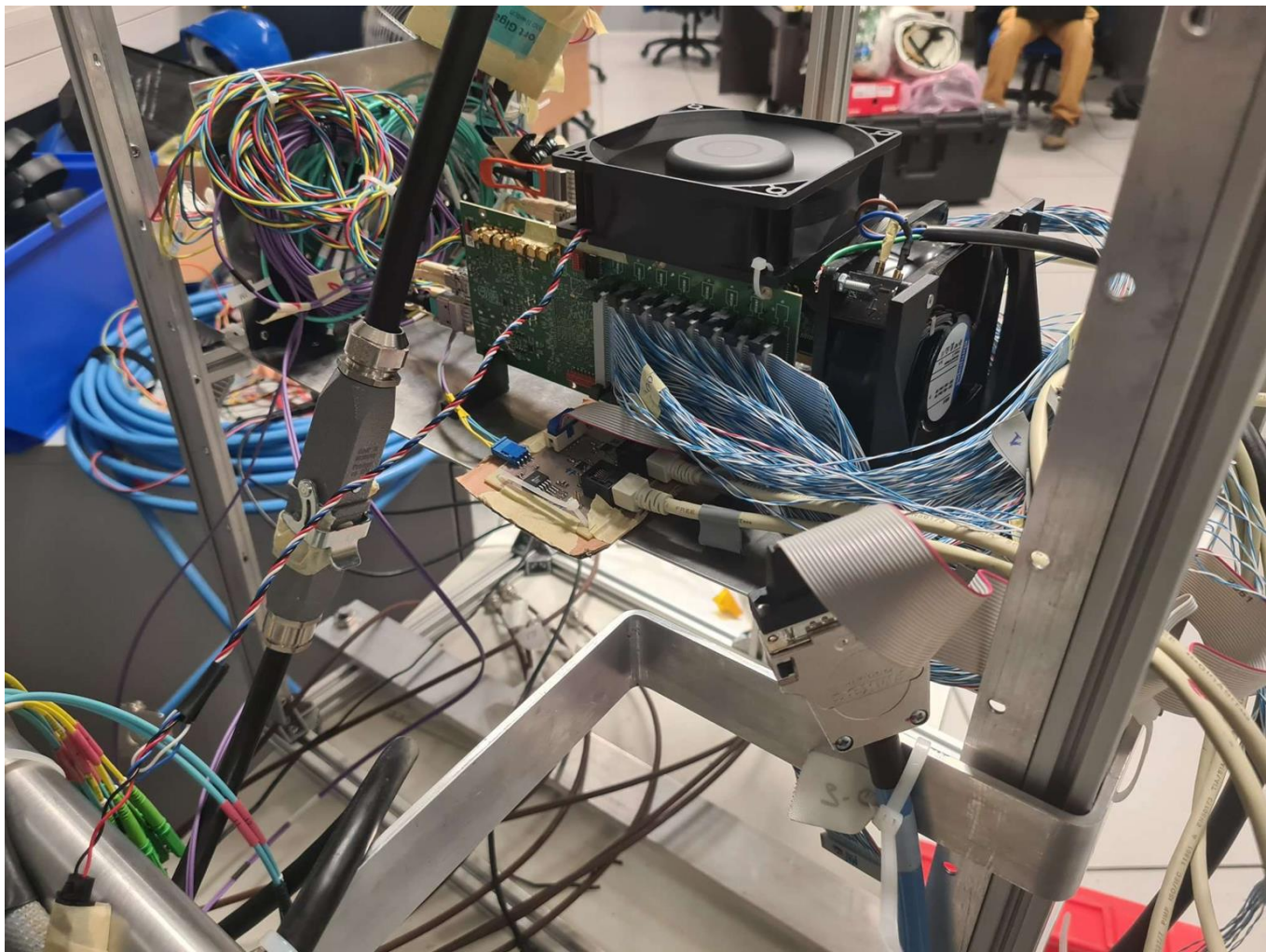
Power cycles (red)
Exclusive configurations (blue)

- Configuraciones exclusivas
- Clara ha hecho este plot, lo ha juntando con el de los power cycles, aqui en rojo (siguiente slide) para ponerlo en el mismo plot

(notese que las configuraciones empiezan mas tarde)



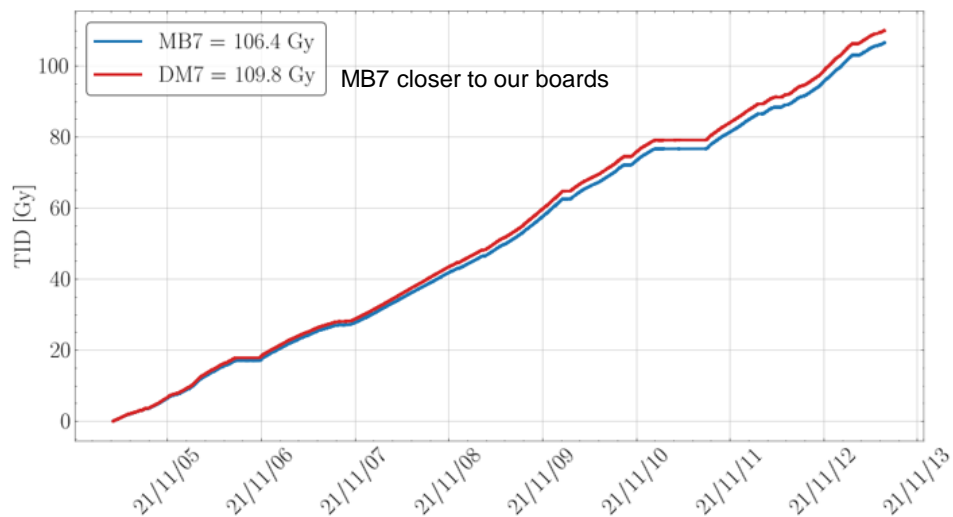




Dosimetry

- Dosimetry provided by CHARM facility through [this report](#).
 - Thanks to M. Brucoli and S. Danzeca for providing data vs. time .
- Most of the time without shielding, but for the first night with the **CuOOIC** shielding
 - 1 % of the dose received at lower rate (1/5 of the TID rate), larger relative fraction of neutrons.

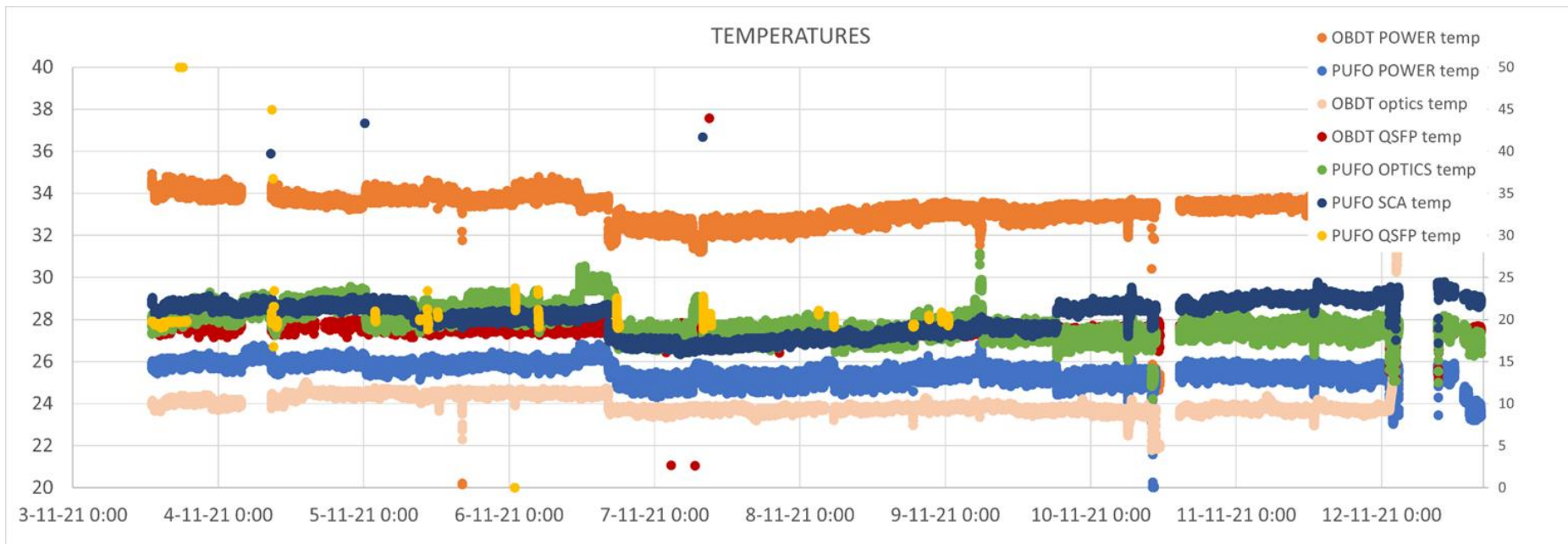
Run	Configuration	POT	TID [Gy]	HEH Fluence [cm ⁻²]	ThN Fluence [cm ⁻²]	1MeV [cm ⁻²]
7_1	CuOOIC	1.54E+15	1.7	4.99E+09	3.76E+10	5.30E+10
7_2	CuOOOO	1.93E+16	108.1	3.28E+11	5.99E+11	1.84E+12

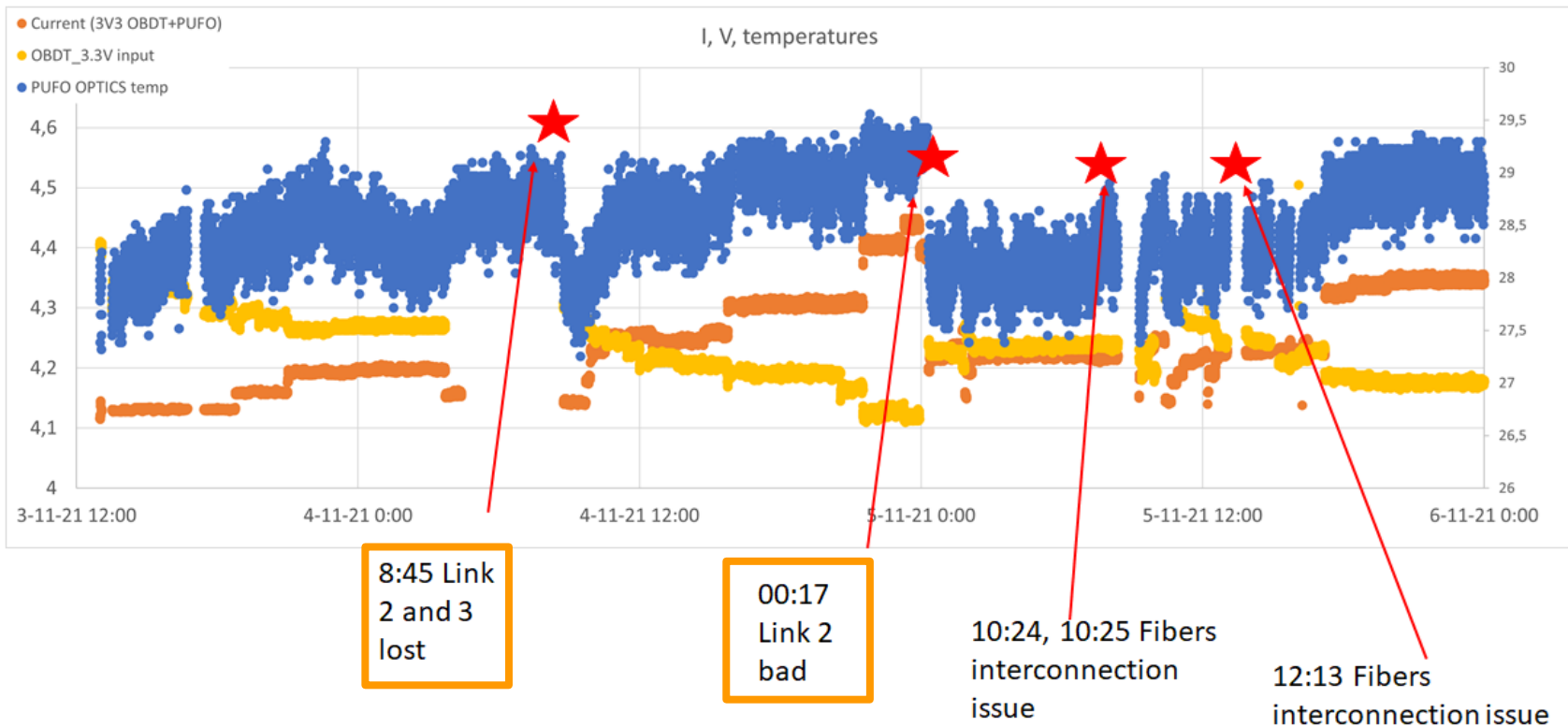


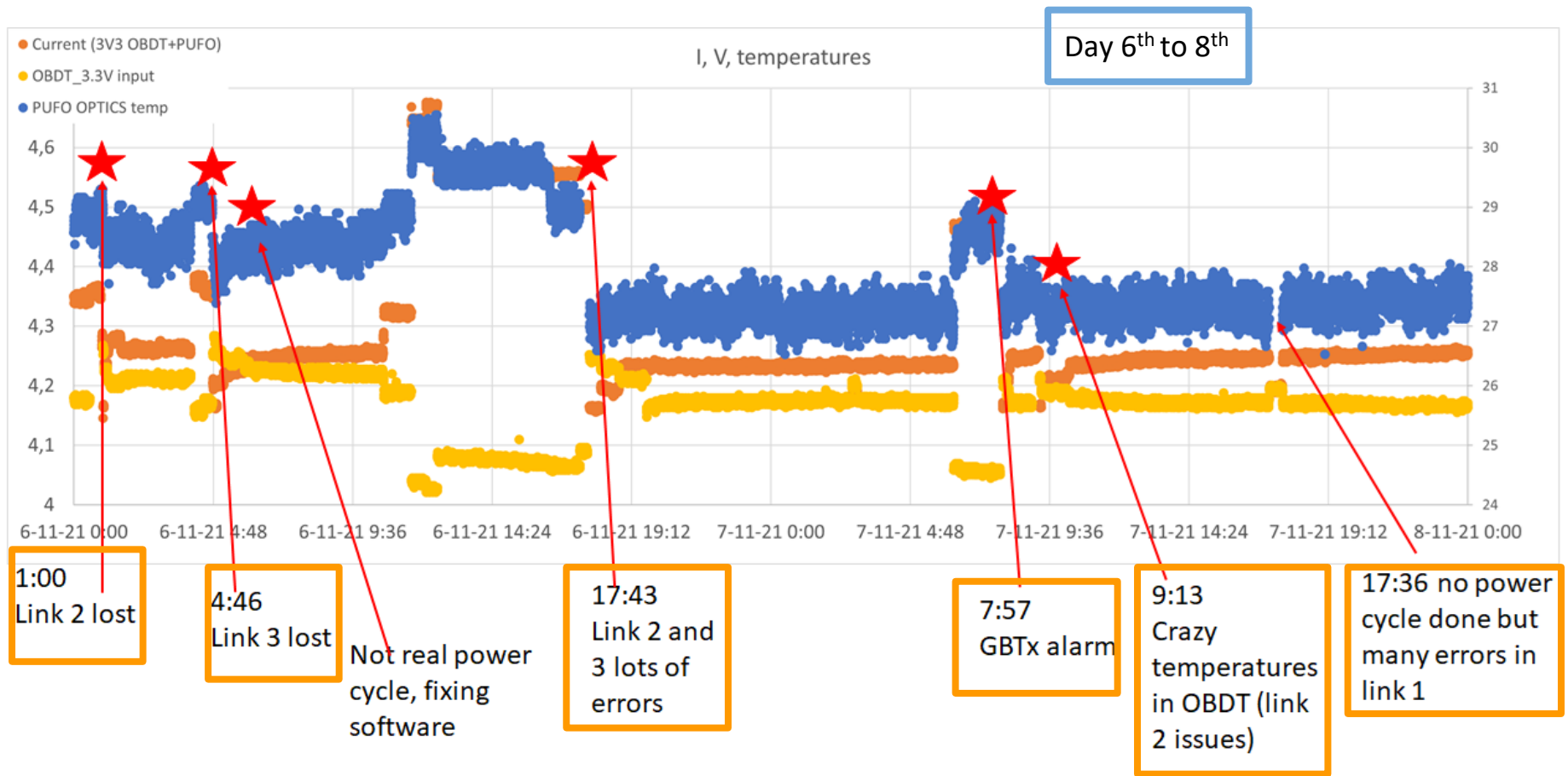
TOTAL received RADIATION LEVEL	Target inside 03/11/2021 17:23
	Configuration change 12-11-21 16:40
Dose (Gy)	109.8
HEH fluence (cm ⁻²)	3.33·10 ¹¹
ThN fluence (cm ⁻²)	6.37·10 ¹¹
1MeVneq fluence (cm ⁻²)	1.89·10 ¹²
R factor (CuOOIC)	7.54
R factor (CuOOOO)	1.83
Total POT*	2.08·10 ¹⁶

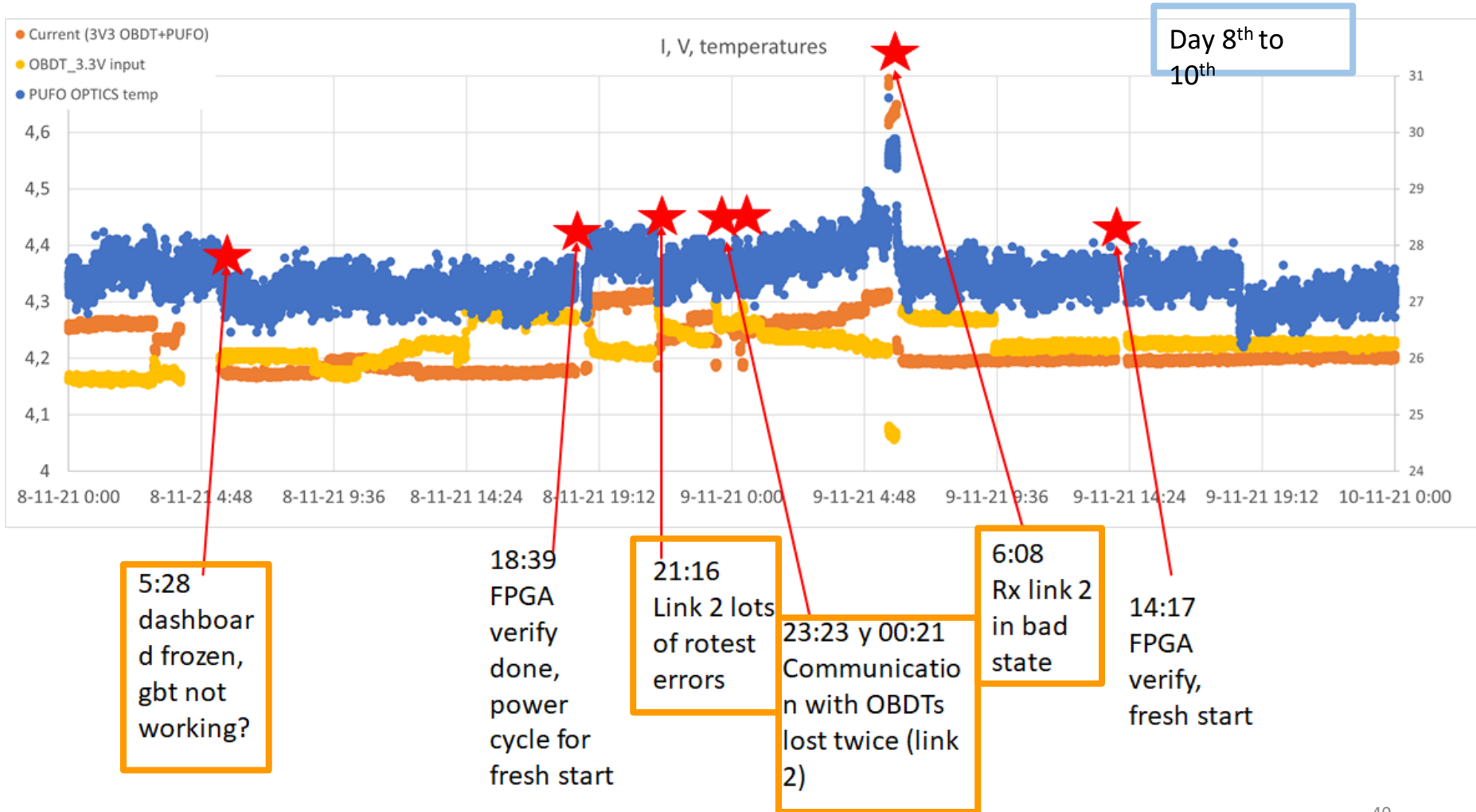
*POT is the total number of protons hitting the target.

TEMPERATURES

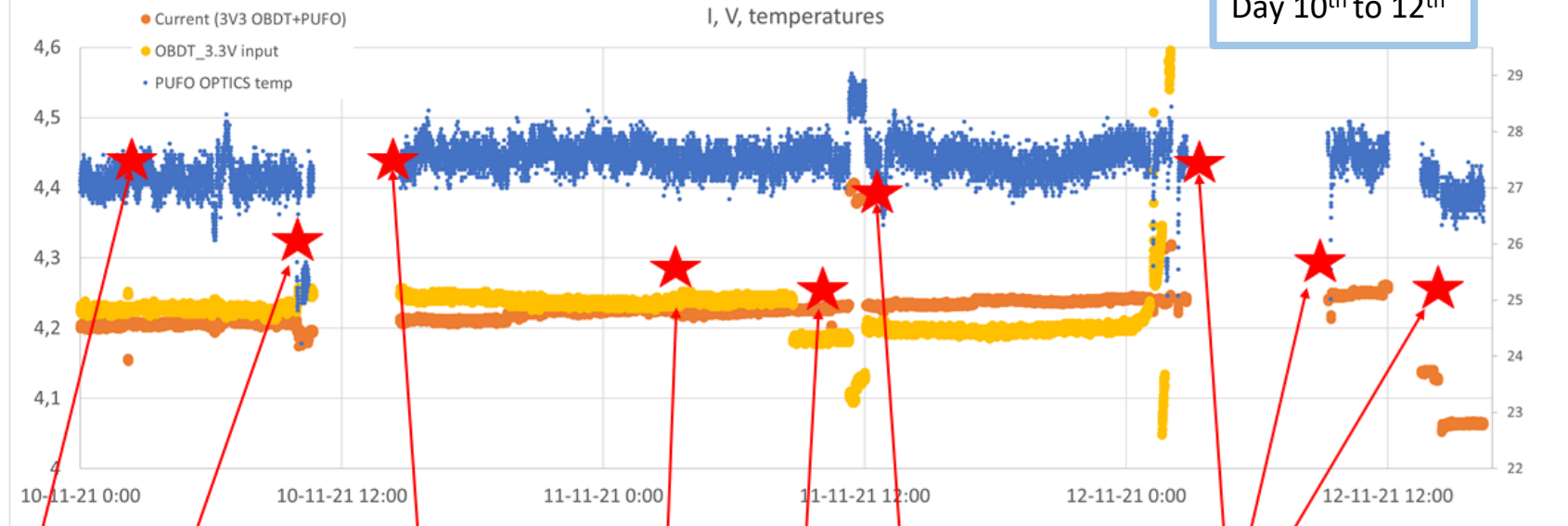








Day 10th to 12th



2:13 link 1
not
working

10:43
FPGA
verify
fresh start
(no beam)

13:18 y
14:39
testing
(no beam)

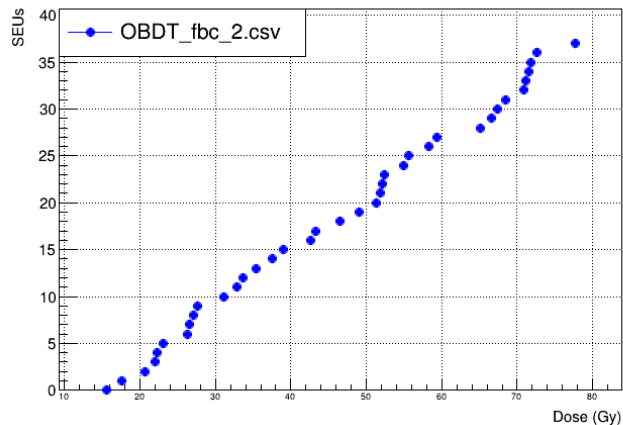
3:32 links
lost

10:34 Link 2
problems,
wrong
temperature
values

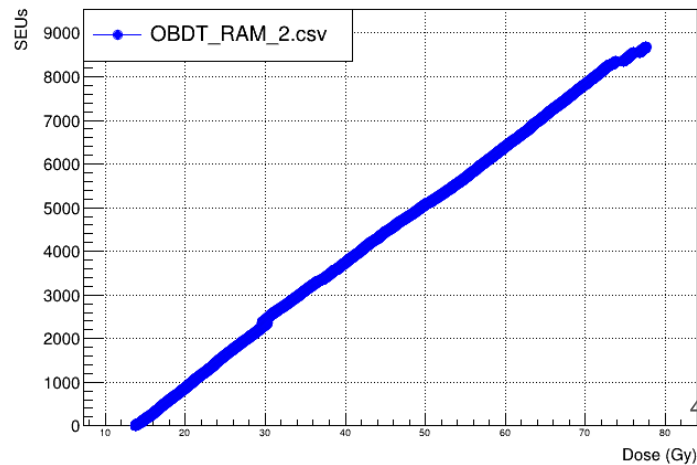
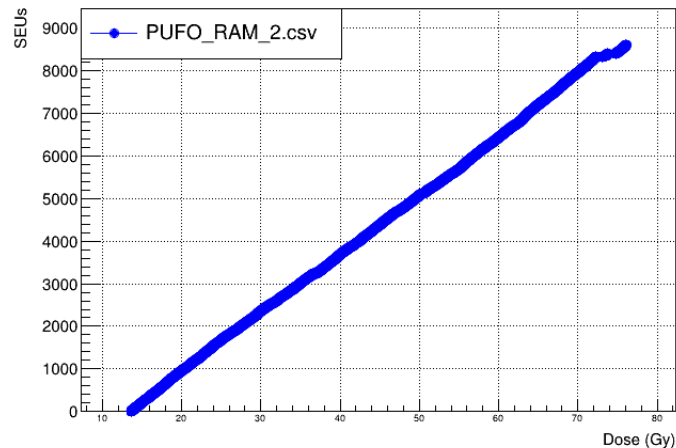
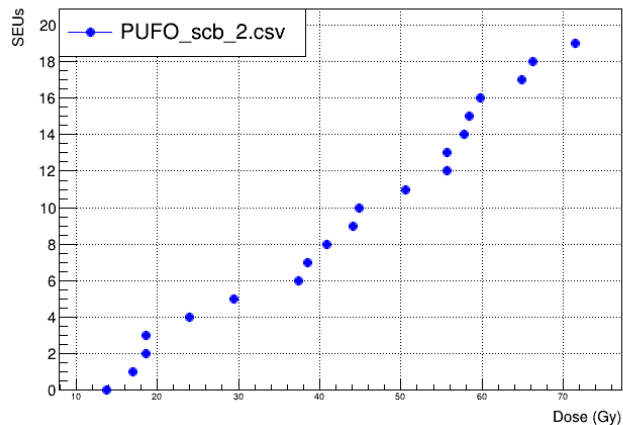
12:02 high currents
(PUFO QSFP?)

00:58 SCA
temperat
ures go
crazy

Polarfire SEU-reference test



A few examples of how the number of SEUs in this reference test where increasing versus the integrated dose



Polarfire & OBDT: Timing test counters:

Expected dose in the CMS detector during HL-LHC

	Dose at LHC	Dose at HL-LHC	#boards	
MB1 central	0,07	0,7	108	75,6
MB1 external	0,21	2,1	72	151,2
MB2	0,023	0,23	180	41,4
MB3	0,006	0,06	240	14,4
MB4	0,059	0,59	240	141,6
TOTAL			840	0,505

Gy

The cross section obtained with this number of failures and the amount of logic contained in the Polarfire firmwares is $2.33 \cdot 10^{-15} \text{ cm}^2/\text{bit}$

Extrapolation of the #SEUs for the OBDT at HL-LHC

#failures/system	107
#failures/board	53,5
#failures for 840 boards	44940
Total dose integrated at CHARM (Gy)	93,96
Dose at HL-LHC (Gy)	0,565
Dose factor	166,30
#failures all HL-LHC	270,23
#failures/year	27,02
#failures/day (100 operating days/year)	0,27
#days between failures	3,70

Expected SEU rate in the detector during HL-LHC with the firmware used at CHARM (TMR included)