4D fast tracking for LHCb U2

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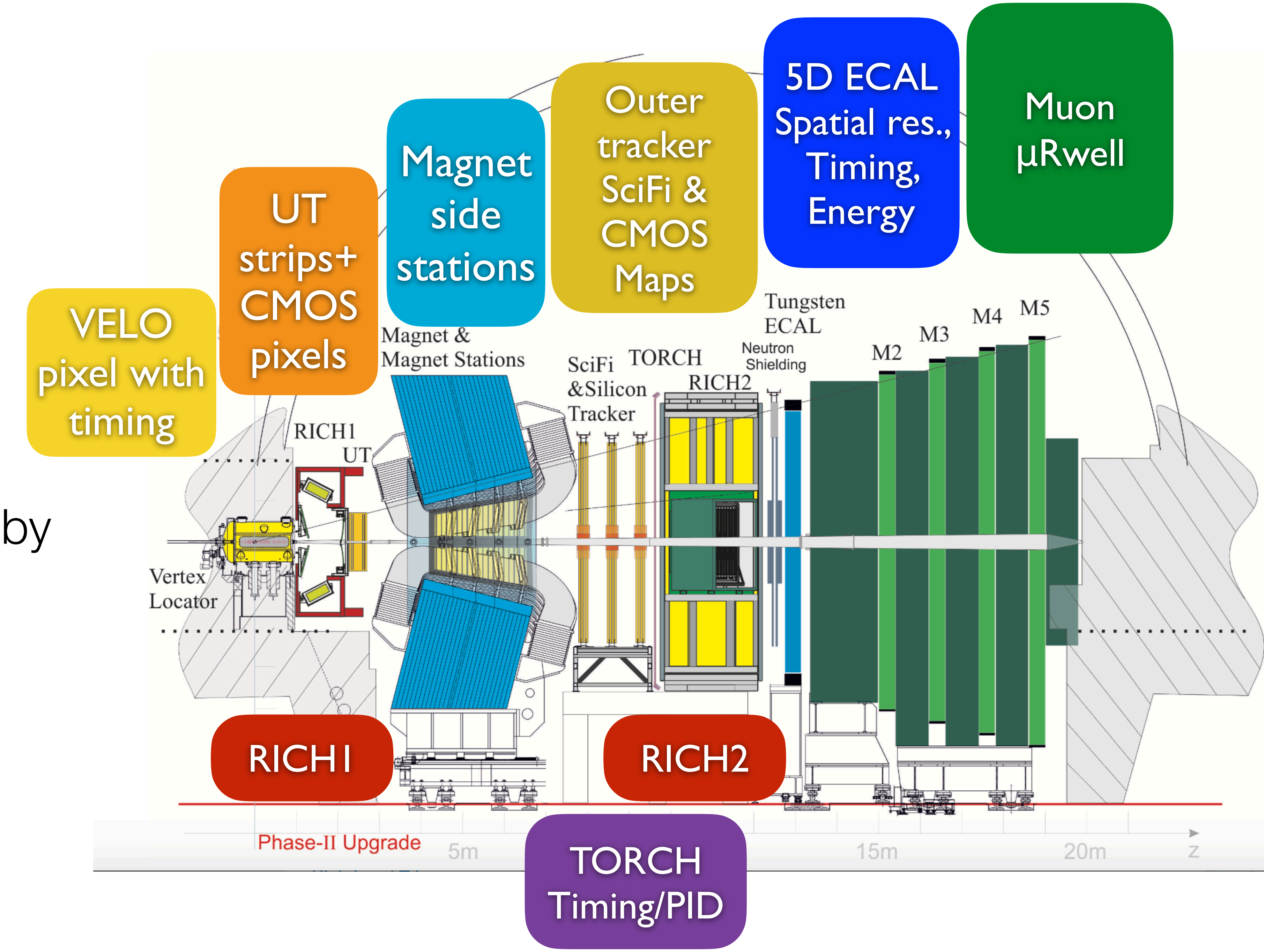
Outline

- LHCb upgrade II
- Timespot R&D
- 4D fast tracking algorithm
- Performance
- Implementation in FPGA
- R&D and plans for the future
- Summary

LHCb Upgrade II

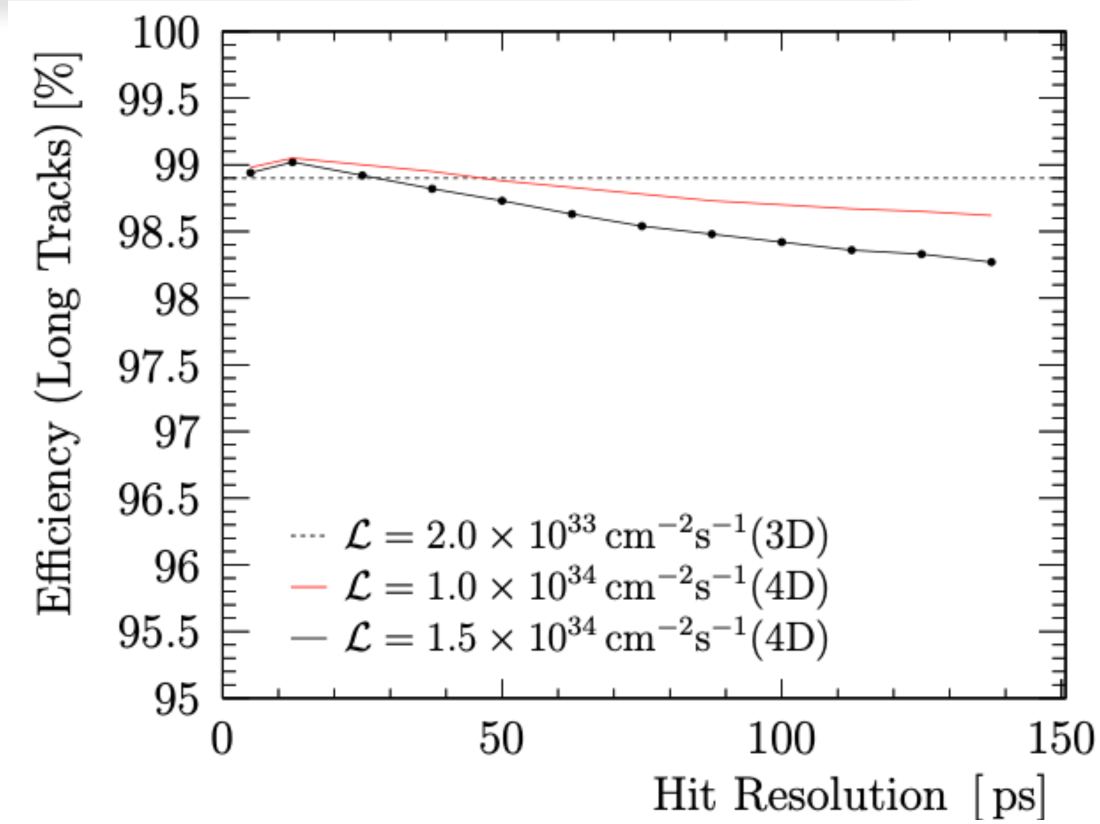
- Achieve ultimate precision on heavy flavour physics with LHCb U2
- Inst. lumi 1.5×10^{34} $cm^{-2}s^{-1}$ in Run5 ($\times 7.5$ increase wrt U1)
- Data sample 300 fb^{-1} by the end of Run 6
- LHCb U2 detector installation in LS4 (2033-2035)

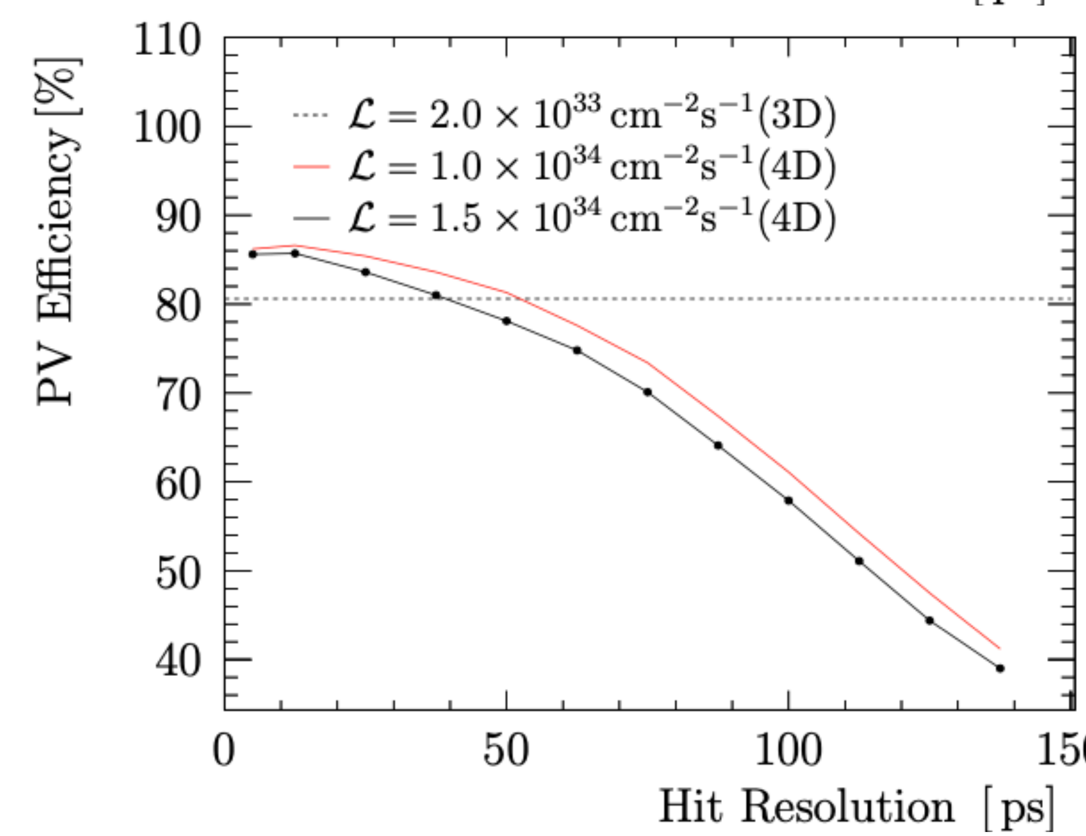


LHCb Velo U2 studies

CERN-LHCb-PUB-2022-001

- Time resolution for hits in the VELO driven by tracking and PV reco
- Time spread among PVs is about 180 ps. Time info helpful to reduce hit combinations for track reco
- Nominal requirement for single hit time resolution 50 ps





R&D projects at INFN

https://web.infn.it/timespot/

TIMEPOST R&D project
-**TIME** & **SP**ace real-time **O**perating **T**racker
-Three years project, from 2018, funded by **INFN**
-Development of a **silicon and diamond 3D tracker with fast timing: demonstrated 20 ps** hit resolution at testbeam at PSI
-**Construction of a demonstrator** integrating sensors, front-end electronics, **real-time** processors

https://tinyurl.com/yxeemhgm

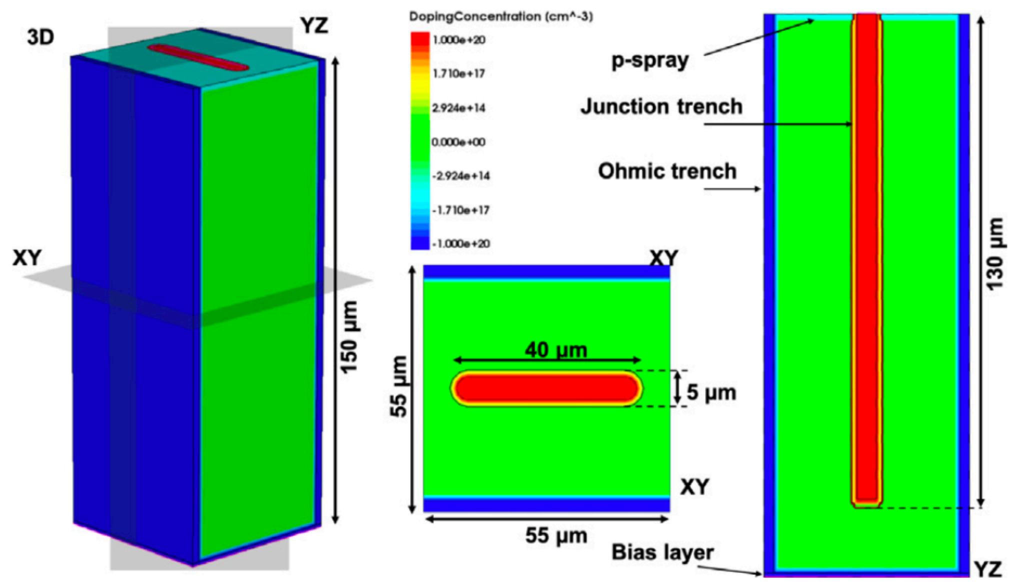
INSTANT project phase-1 funded by **ATTRACT** programme
-**I**maging i**N S**pace-**T**ime **AN**d **T**racking
-Development of a **compact imaging and particle-tracking device**
-Application in HEP, medical imaging, fast neutron source monitoring

Timespot sensors

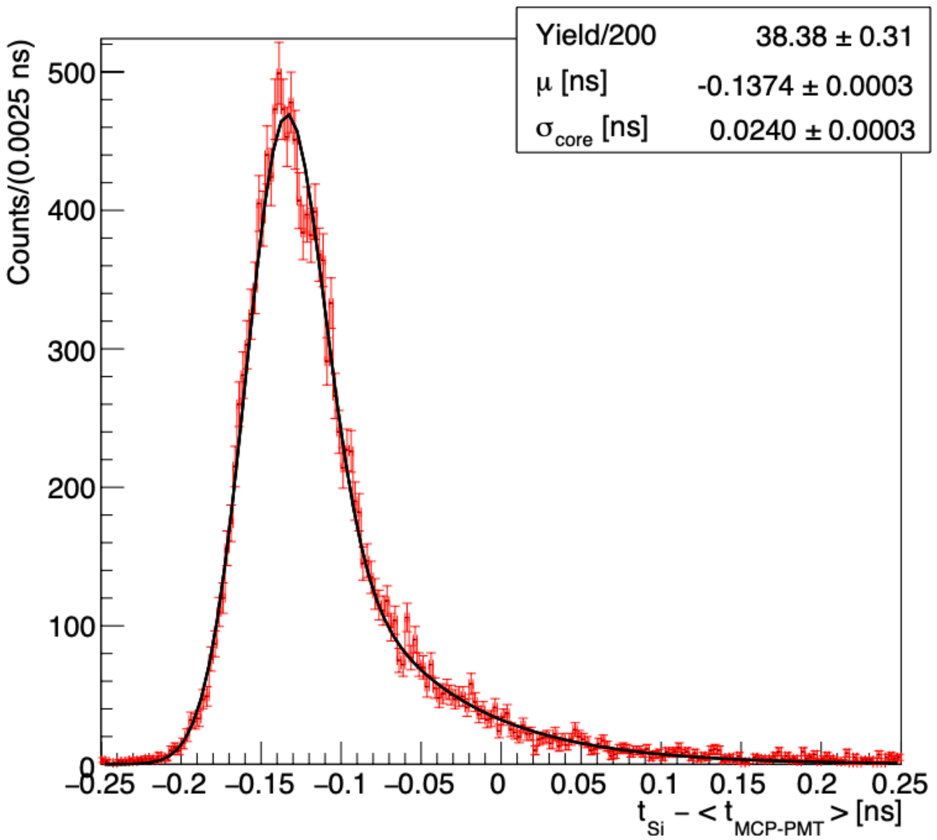
- 3D sensors: 55 µm × 55 µm pixel and 150 µm thickness
- Short drift distance of charge carriers: excellent radiation hardness and fast signals
- 3D-trench geometry for uniform electric field
- 20 ps time resolution measured on charged pion beam at PSI

NIM, A 981 (2020) 164491
L. Anderlini *et al* 2020 *JINST* **15** P09029
JINST 16 (2021) 09, P09028

Nuclear Inst. and Methods in Physics Research, A 981 (2020) 164491



L. Anderlini *et al* 2020 *JINST* **15** P09029

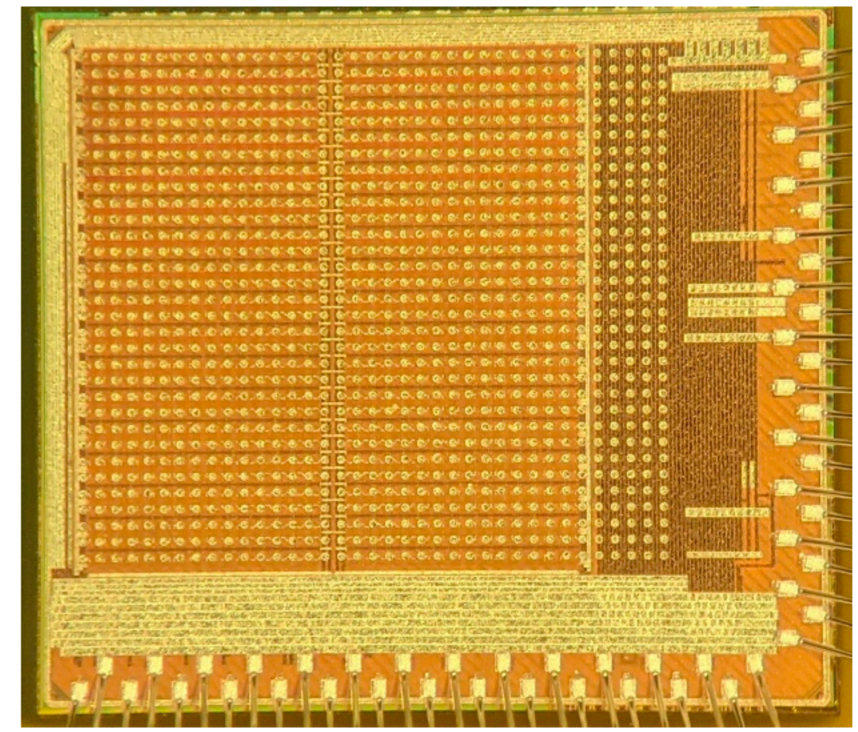


Timespot ASIC

arXiv:2201.13138, TWEPP2021

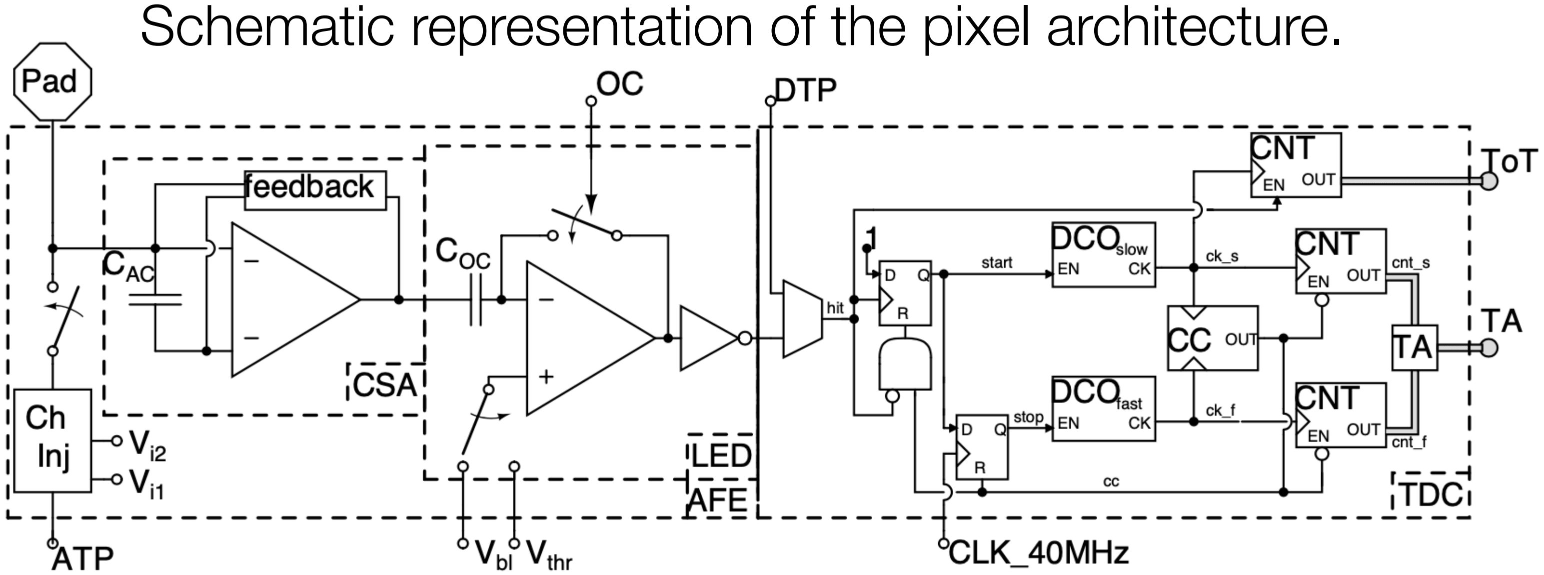
- Timespot1 ASIC: 28-nm CMOS technology, 32×32 pixel matrix, 55 µm pitch
- First standalone ASIC tests are very encouraging: TDC average resolution 23 ps, analog front-end average resolution 43 ps. Tests with sensor and particle generated signals are ongoing
- Possibility to improve performance with minor corrections to the design

Timespot1 ASIC 2.6 mm × 2.3 mm



Timespot1 PBC board 8 cm × 12 cm

Schematic representation of the pixel architecture.



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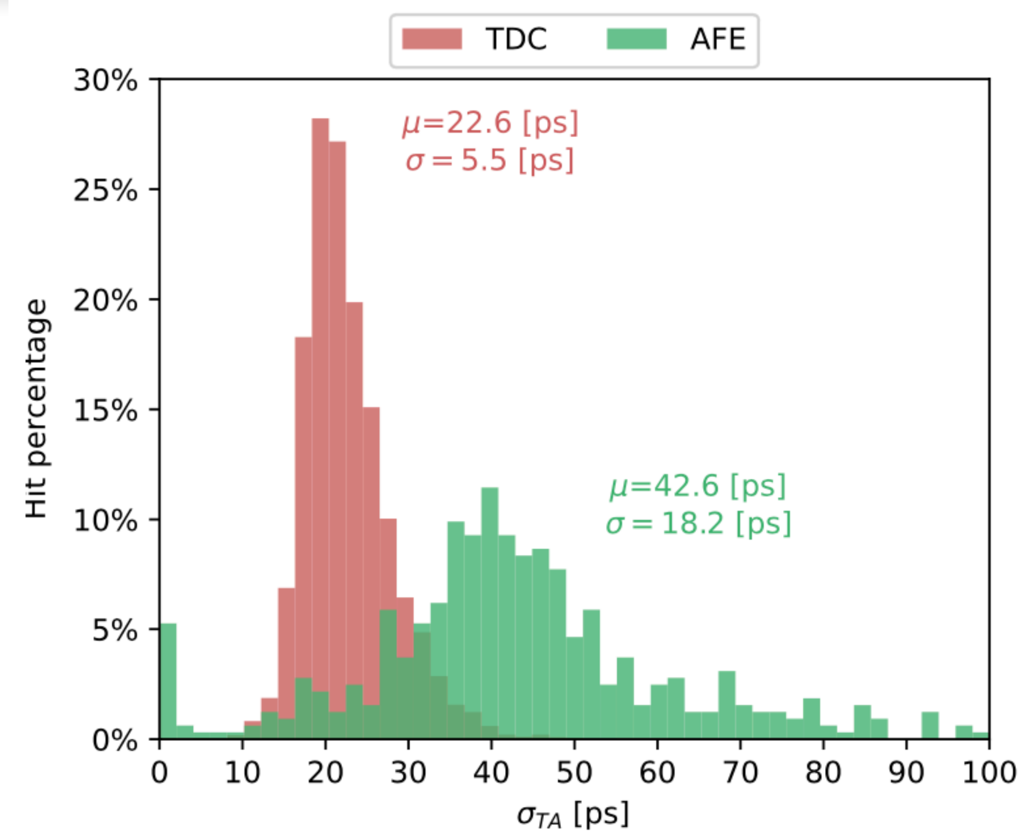
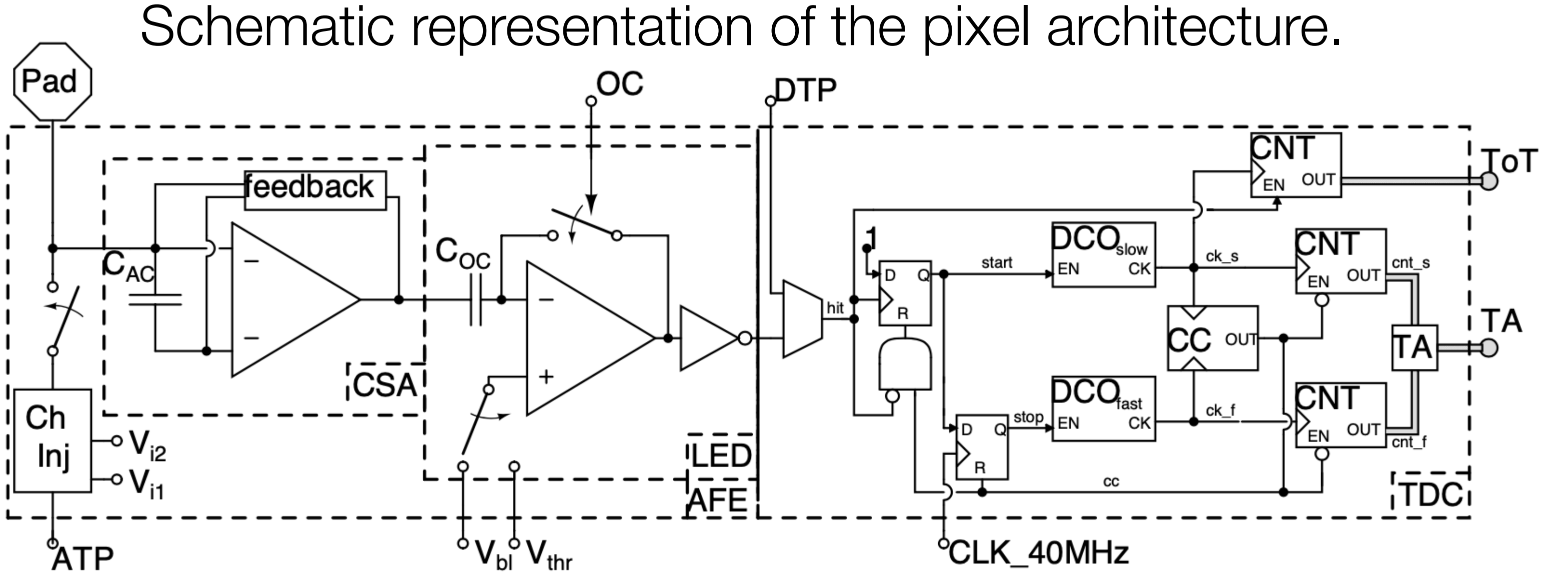
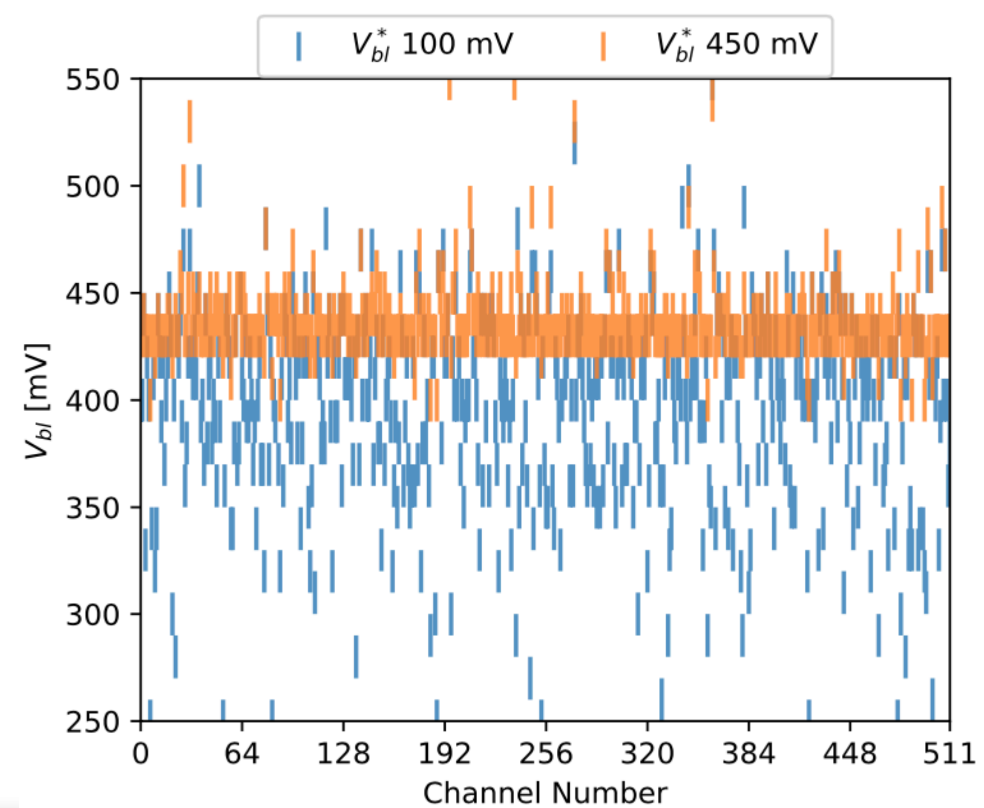


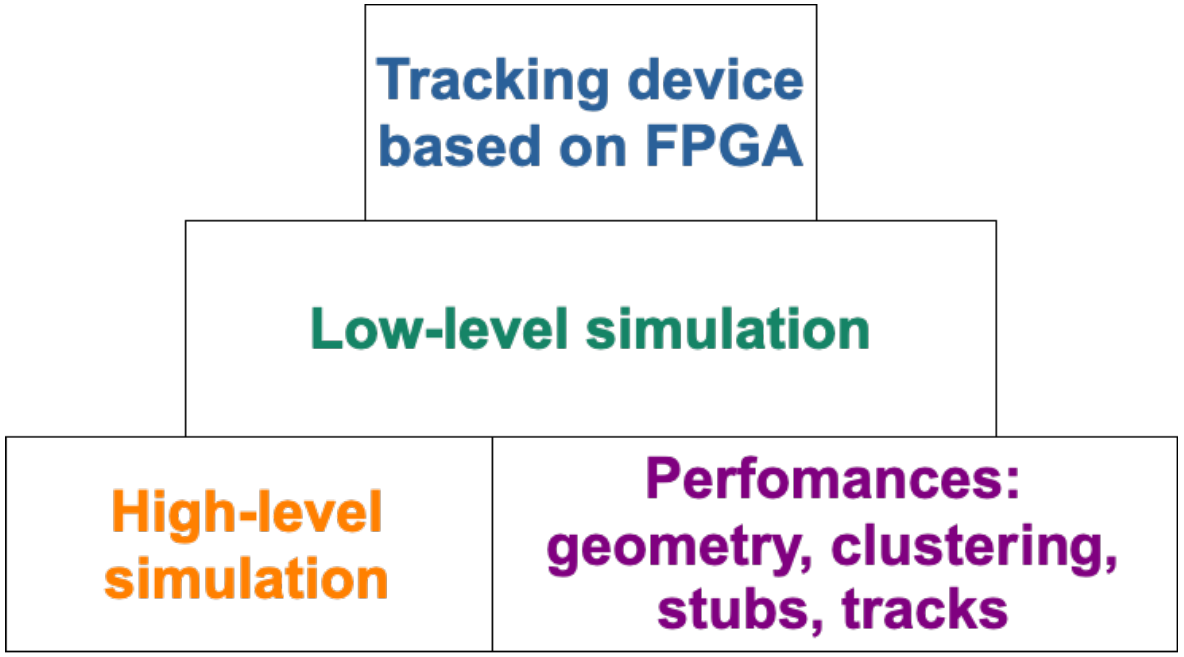
Schematic representation of the pixel architecture.



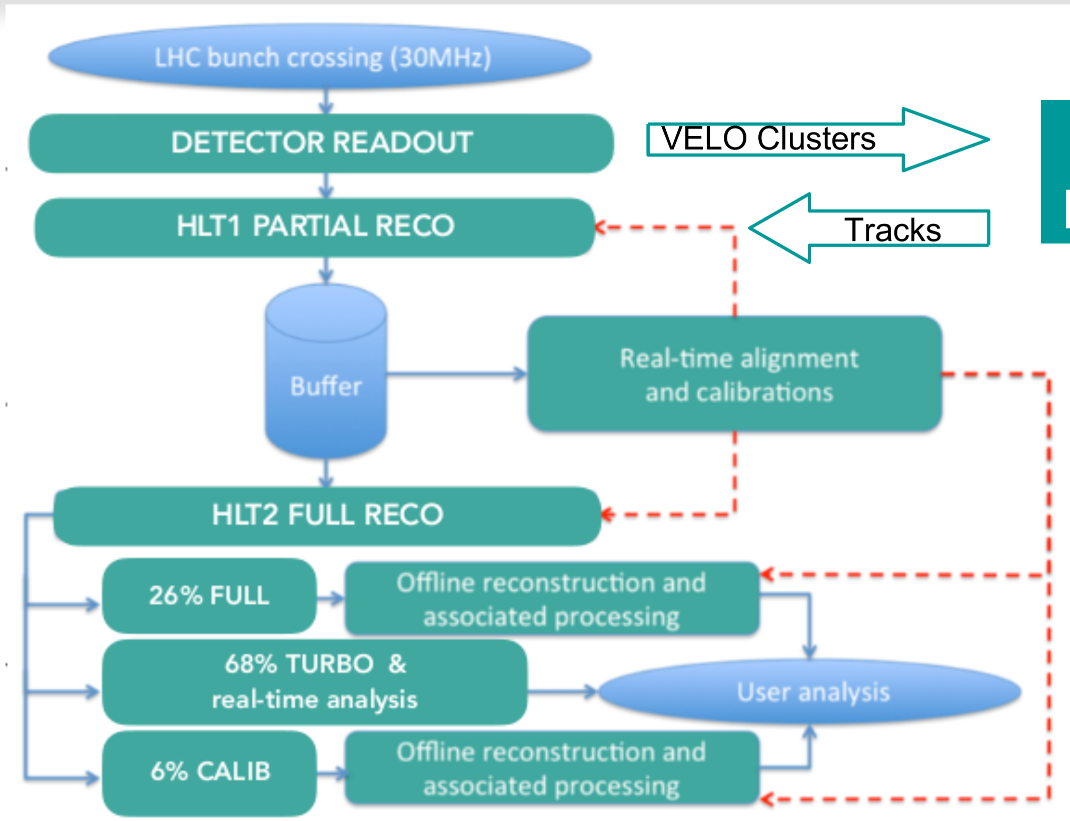


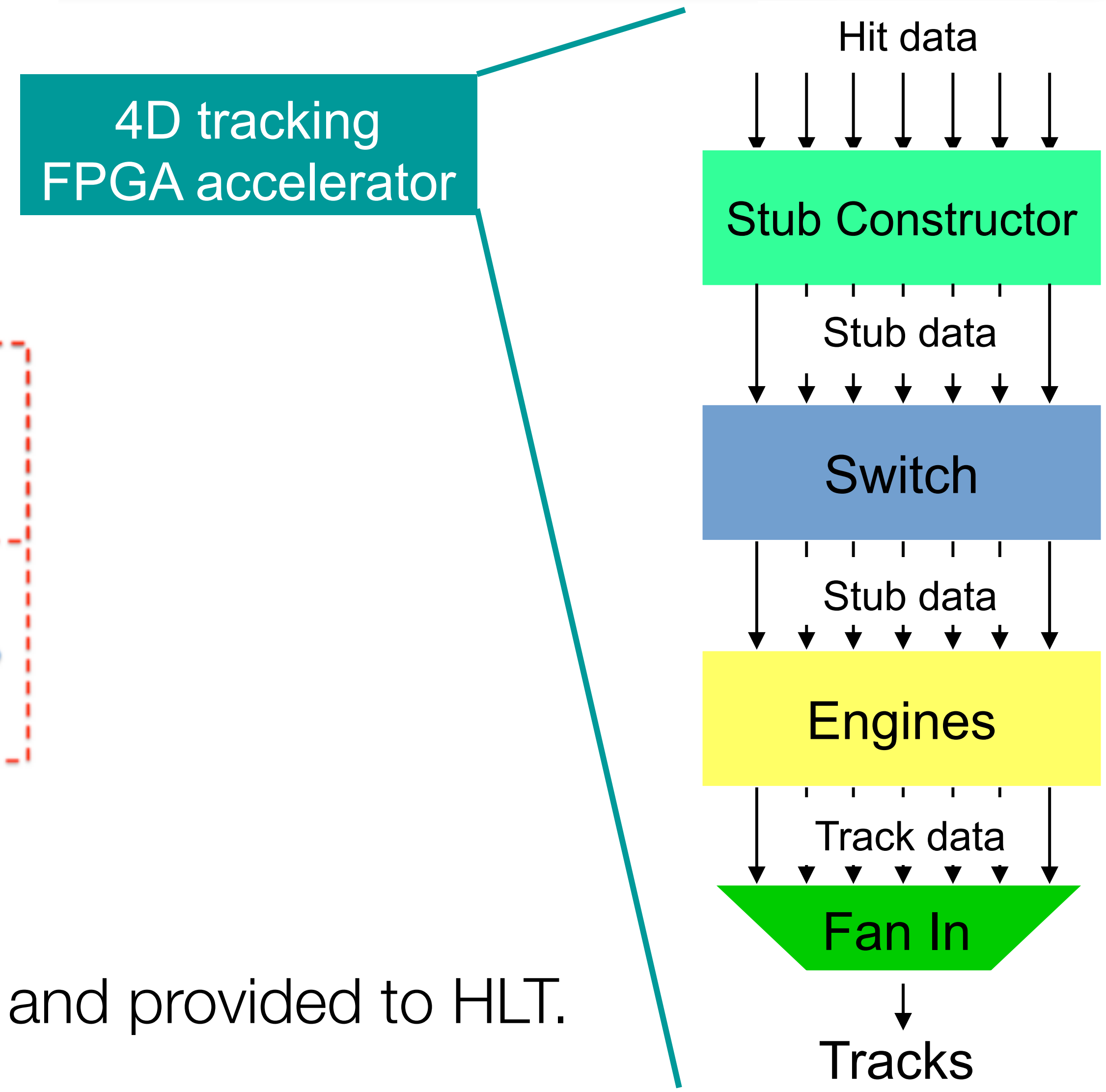
4D fast tracking studies

- Objectives:
  - Fast Tracking at HL-LHC 40MHz event rate
  - Simulate a LHCb VELO sector
  - FPGA processing: clustering, parallel track reconstruction
  - Performance studies: latency, FPGA usage, max. evt. rate, tracking efficiency, resolution
  - Optimisation of detector geometry



Fast tracking in FPGA for U2

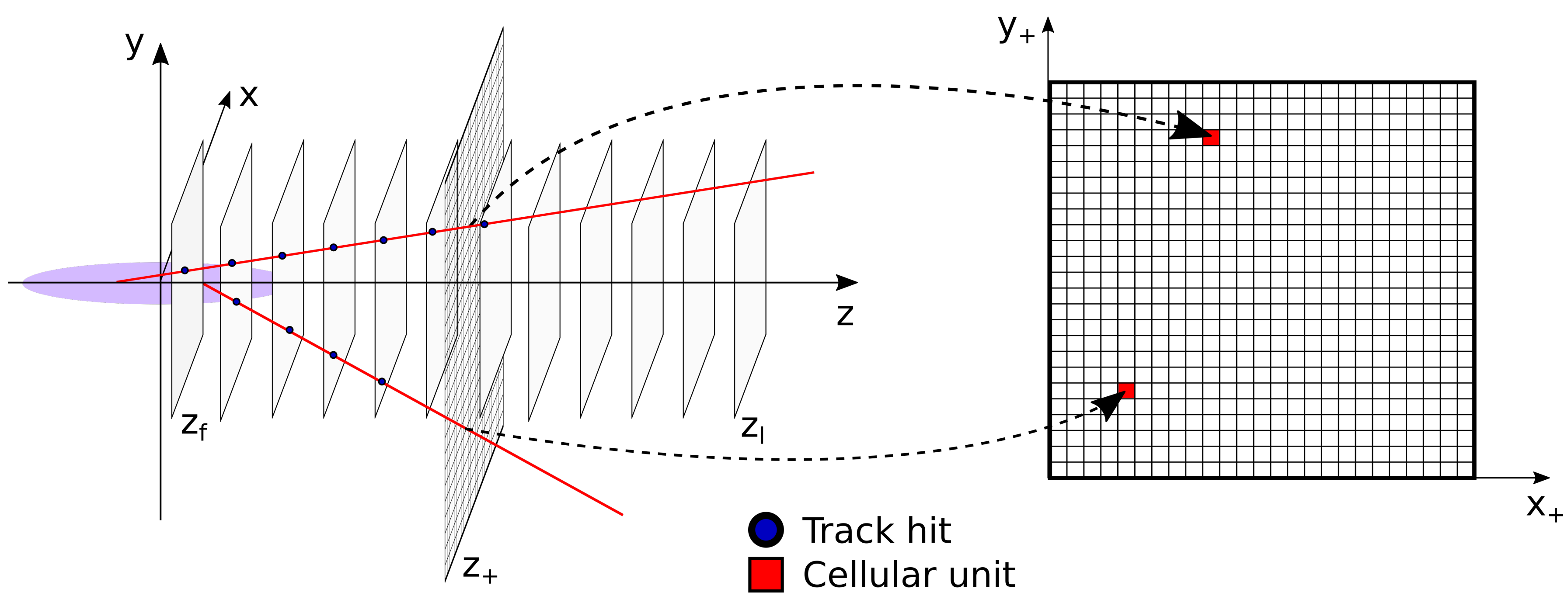


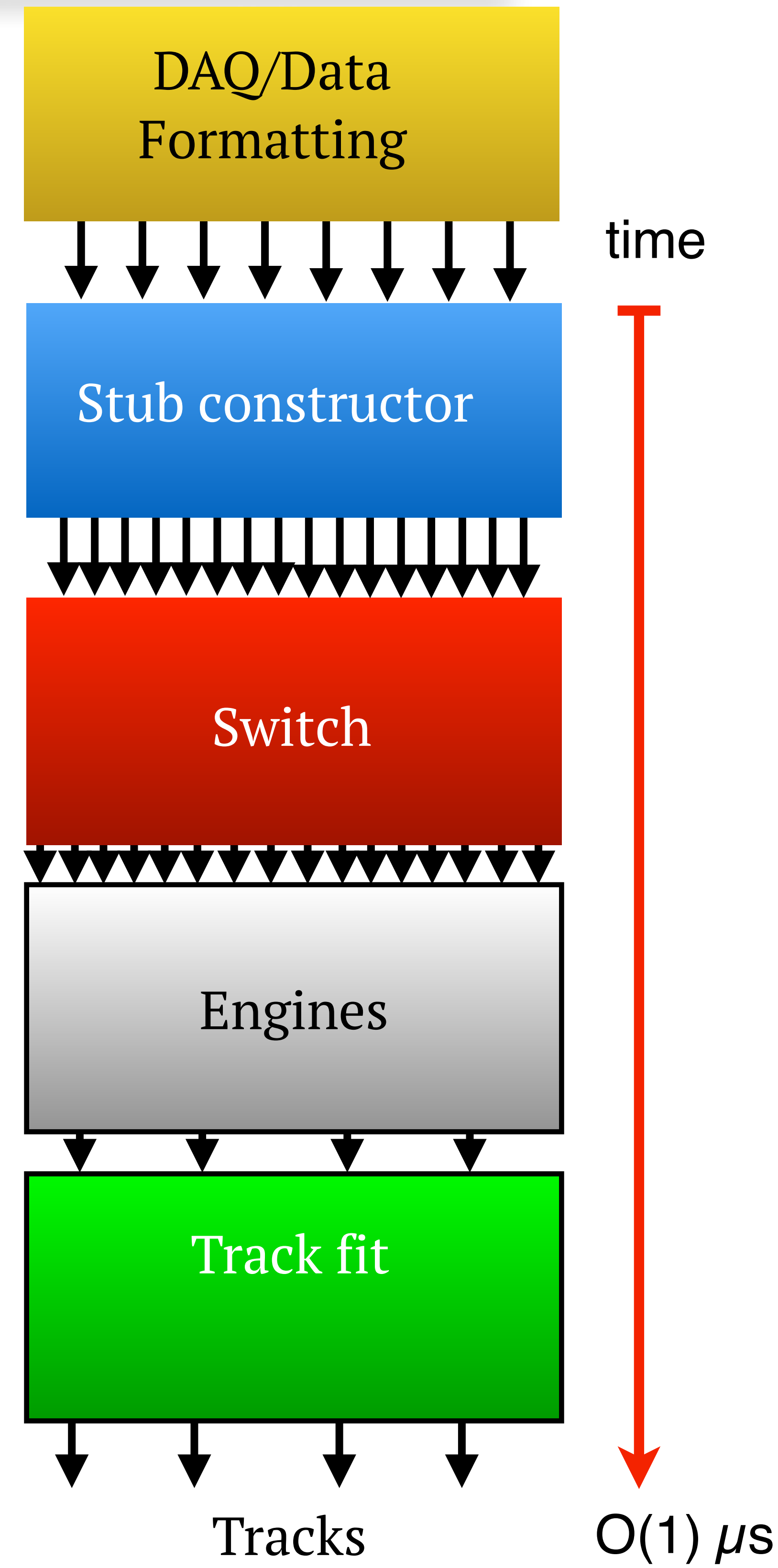


- Tracks can be reconstructed in **FPGA** and provided to HLT. **Low latency** order 1 μs
- Both **tracks** and collection of hits can be provided to the HLT
- Reduce HLT data processing since early stages, e.g. analyse 1 interesting *pp* collision only per event

4D fast tracking

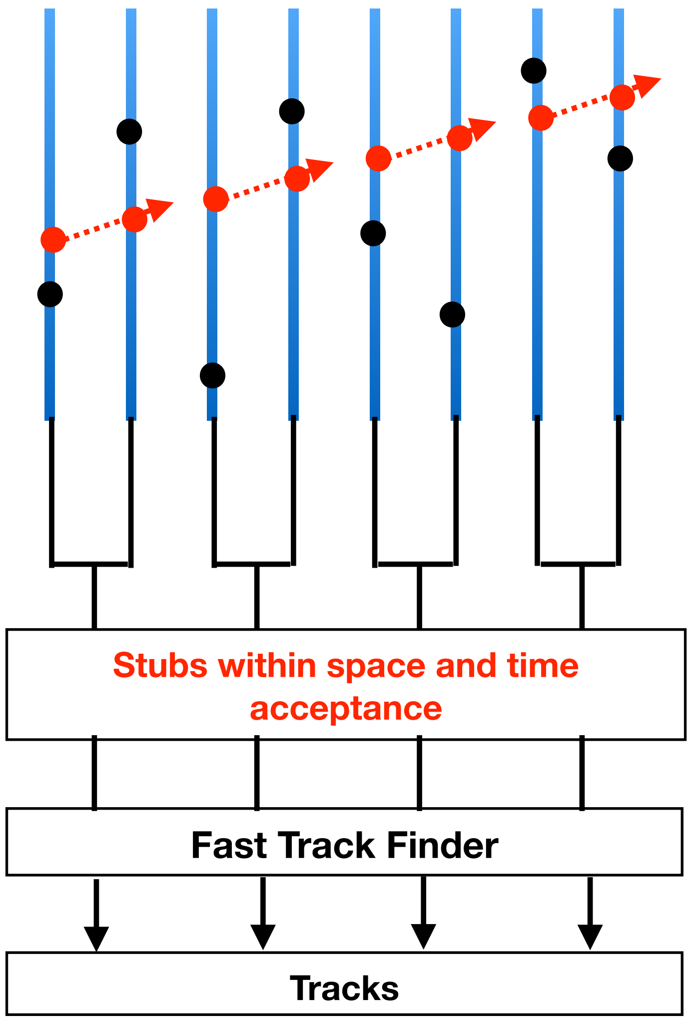
- **Parallel** tracking algorithm implemented in FPGA
- Highly parallel and **pipelined** architecture
- **Track** identified from cluster of stubs on reference plane



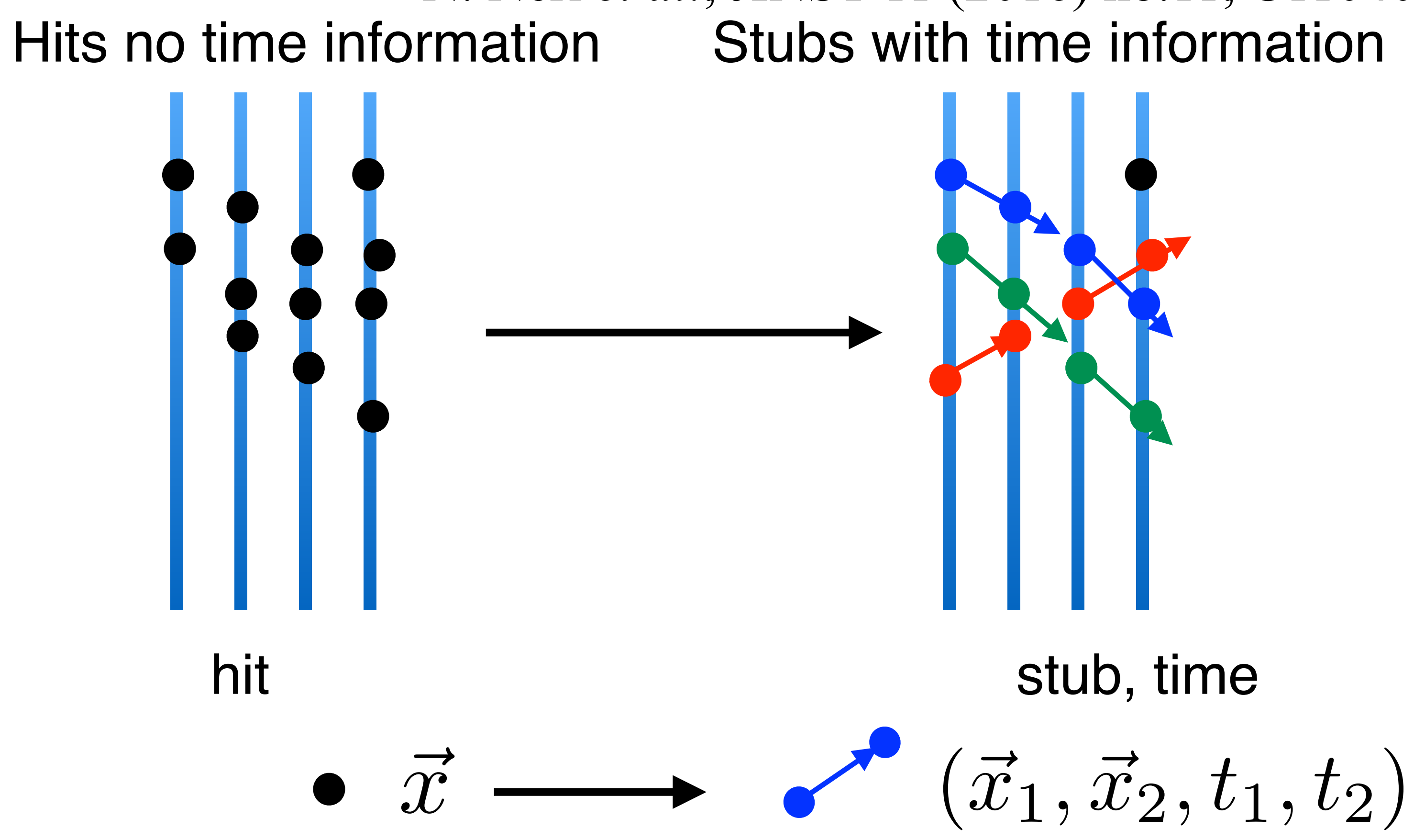


4D fast tracking

- Detector with embedded 4D tracking capabilities
- **Stub** based approach for **track** reconstruction: no assumption on particle origin

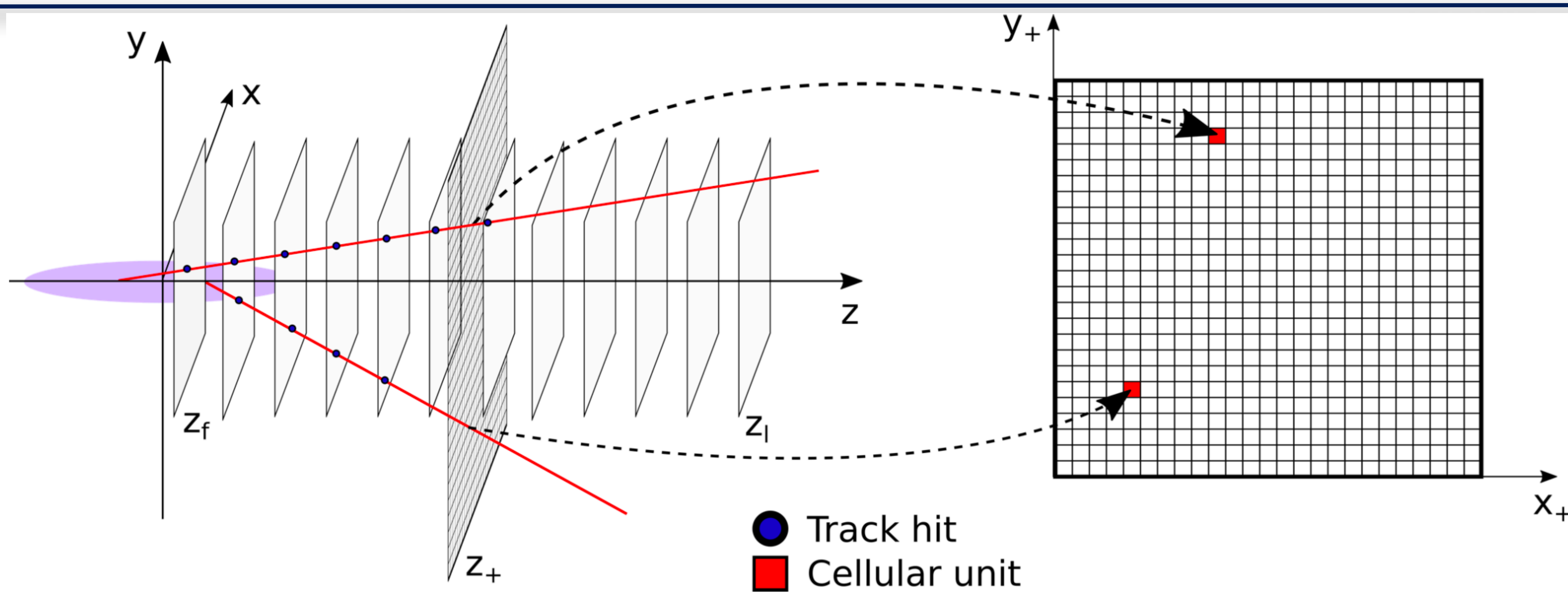


N. Neri *et al.*, JINST 11 (2016) no.11, C11040



- Stubs with **timing**
  - particle velocity compatible with speed of light
  - using timing for hit combinatoric and fake stub suppression

Stub based fast tracking approach



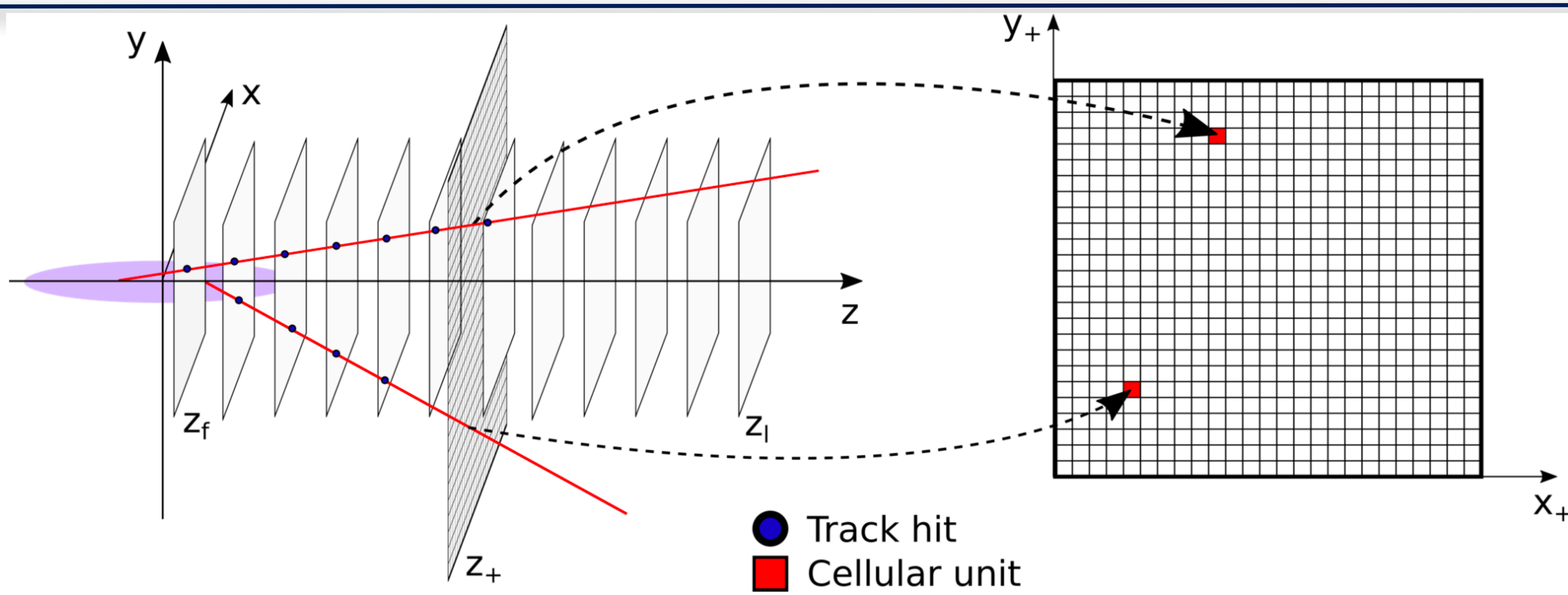
- Track identified by 5 parameters $(x_+, x_-, y_+, y_-, t_0)$ with $\vec{x}_\pm = \dfrac{\vec{x}_f \pm \vec{x}_l}{2}$ and $\vec{x}_f$ $(\vec{x}_l)$ hit coordinates at the first (last) tracking plane, t_0 track time at $z = 0$

- Stub velocity $v_{21} = \dfrac{|\vec{x}_2 - \vec{x}_1|}{t_2 - t_1}$ used to filter stub candidates

CERN-LHCb-PUB-026

- Stubs are projected at reference plane z_+ and cellular units at (x_+, y_+) evaluate a Gaussian response according to their distance wrt stub projections

Stub based fast tracking approach



- Gaussian response to a single stub evaluated by engines

$$W_{ijk} = N_{ijk} \cdot \exp\left(-\frac{s_{ijk}^2}{2\sigma^2}\right), \text{ with } N_{ijk} = \begin{cases} 1 & |s_{ijk}| \leq 2\Delta \\ 0 & \text{otherwise} \end{cases}$$

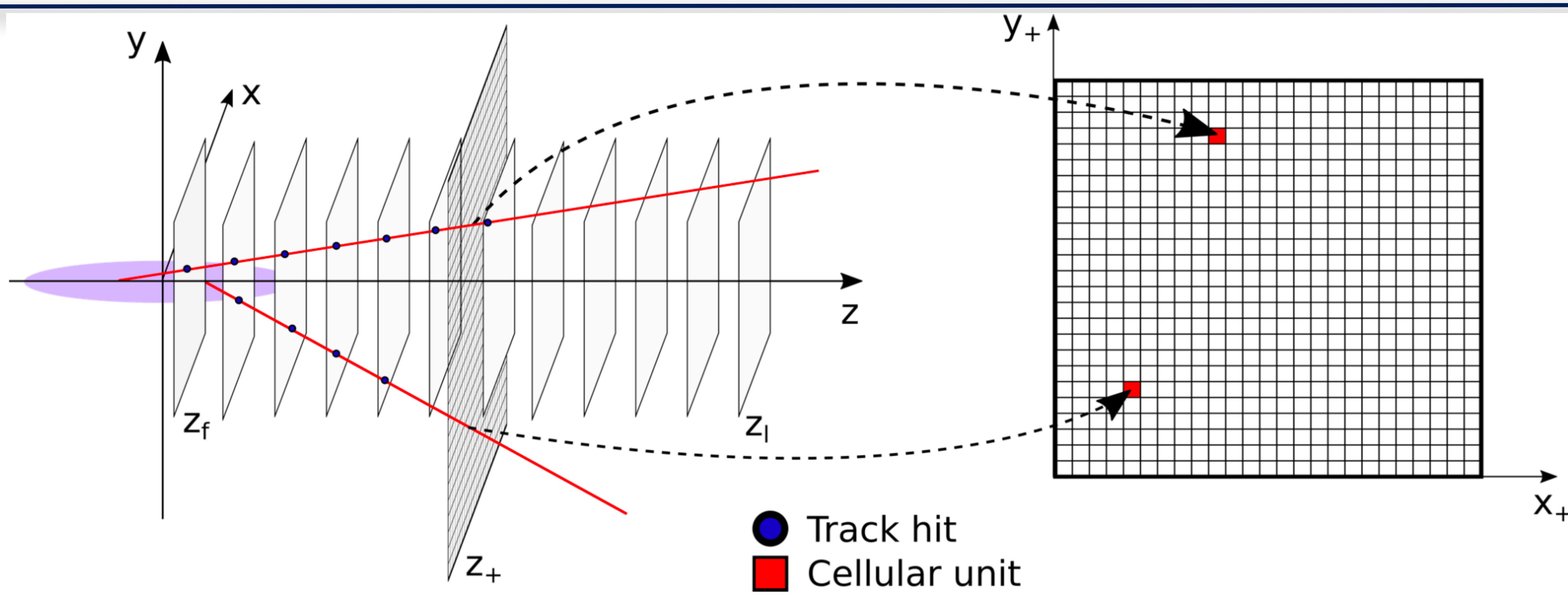
$s_{ijk}^2 = (x_{k+} - x_{i+})^2 + (y_{k+} - y_{j+})^2$ the squared distance, and Δ, σ to be adjusted for optimal response

- Weight function

$$W_{ij} = \frac{1}{N_{ij}} \sum_k W_{ijk}, \text{ where } N_{ij} = \sum_k N_{ijk}$$

if $N_{ij} > thr$ a track candidate is identified

Stub based fast tracking approach



- Track parameters via Gaussian interpolation

$$x_{+,\mathrm{rec}} = x_{+ij} + \frac{\Delta_{x_+}}{2}\frac{\ln(W_{i-1j}/W_{ij}) - \ln(W_{i+1j}/W_{ij})}{\ln(W_{i-1j}/W_{ij}) + \ln(W_{i+1j}/W_{ij})}$$

$$y_{+,\mathrm{rec}} = y_{+ij} + \frac{\Delta_{y_+}}{2}\frac{\ln(W_{ij-1}/W_{ij}) - \ln(W_{ij+1}/W_{ij})}{\ln(W_{ij-1}/W_{ij}) + \ln(W_{ij+1}/W_{ij})},$$

$$x_{-ij} = \frac{1}{N_{ij}}\sum_k x_{-ijk}$$

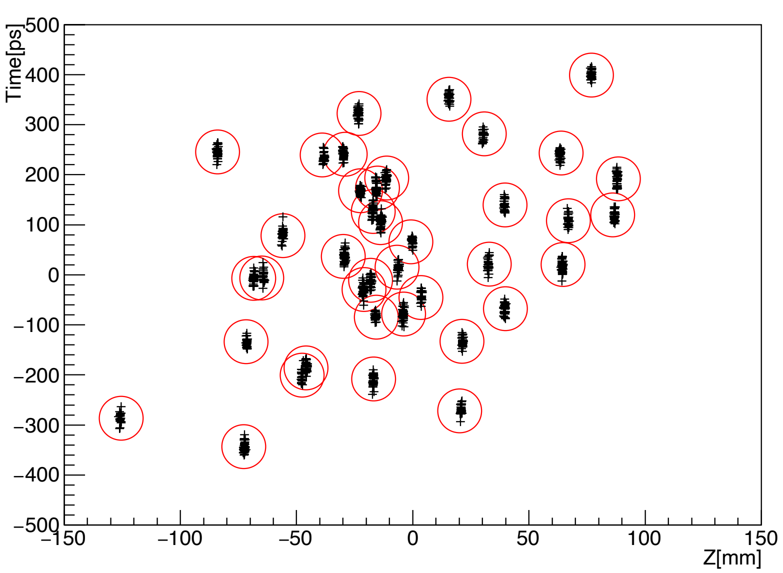
$$y_{-ij} = \frac{1}{N_{ij}}\sum_k y_{-ijk}$$

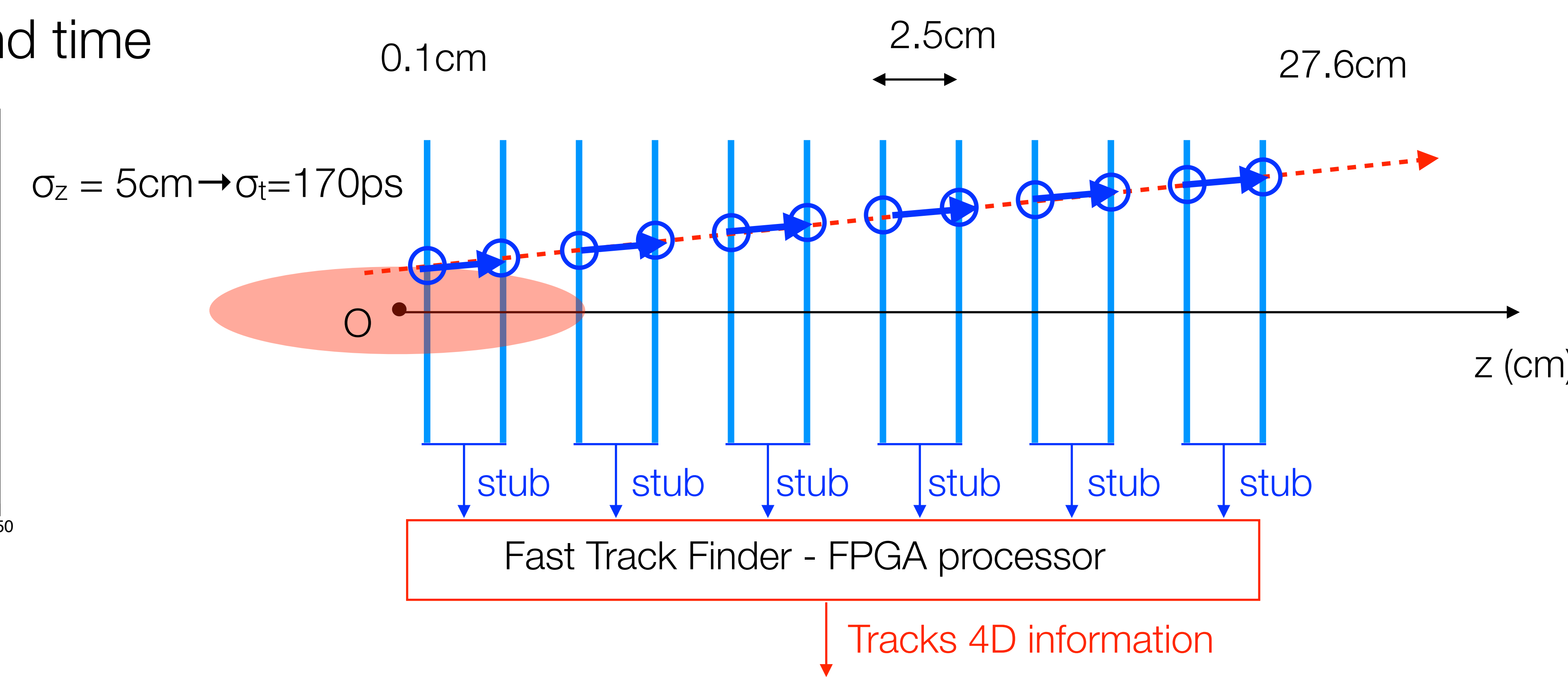
$$t_{0ij} = \frac{1}{N_{ij}}\sum_k t_{0ijk} \ ,$$

Simulations

- Simple case: 12 layer VELO-like detector
- At lumi=$10^{34}cm^{-2}s^{-1}$: pileup~40 and ~1200 tracks/event
- Sensor area = $6x6cm^2$, pixel size = $55x55\mu m^2$, thickness = 200 μm, time res σ_t=30 ps
- **360 000 cellular units** for track identification

PV distribution in space and time





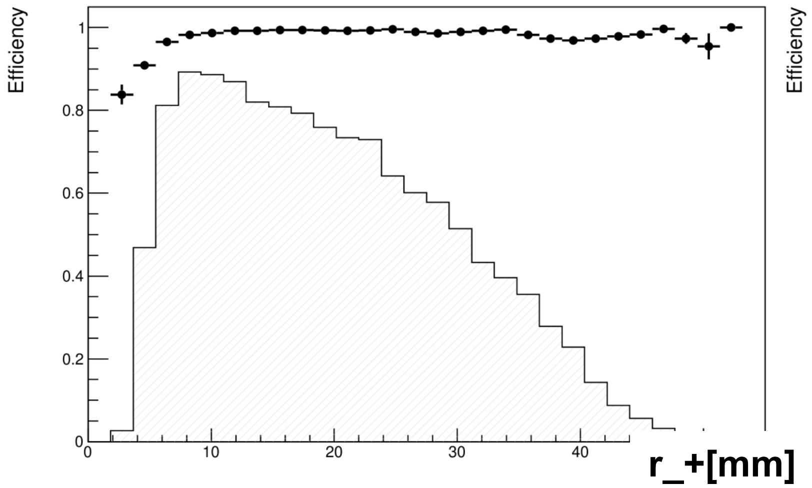
Efficiency

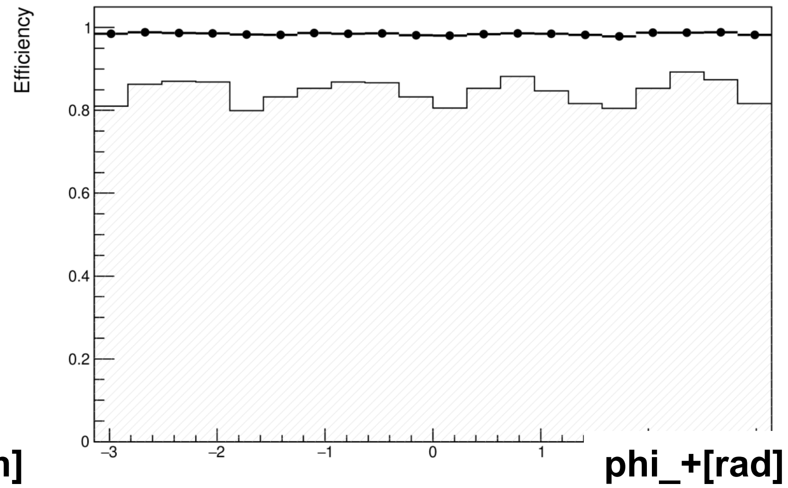
Track reco efficiency vs track parameters r_+, ϕ, d_0, z_0, η :

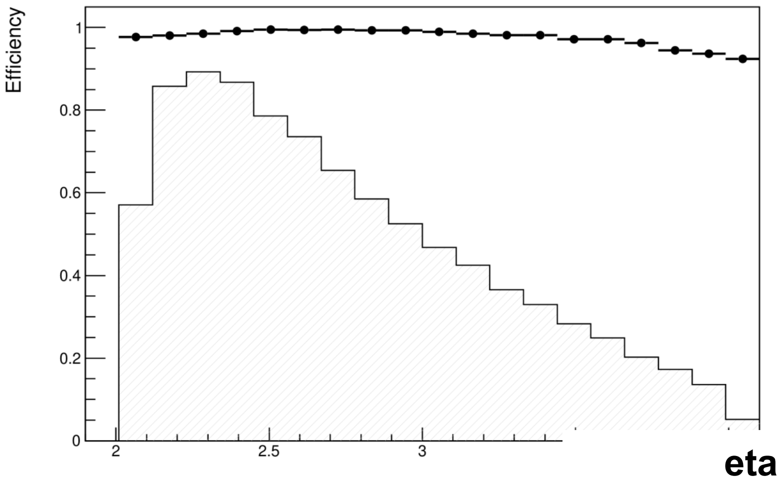
-track efficiency: ~98%

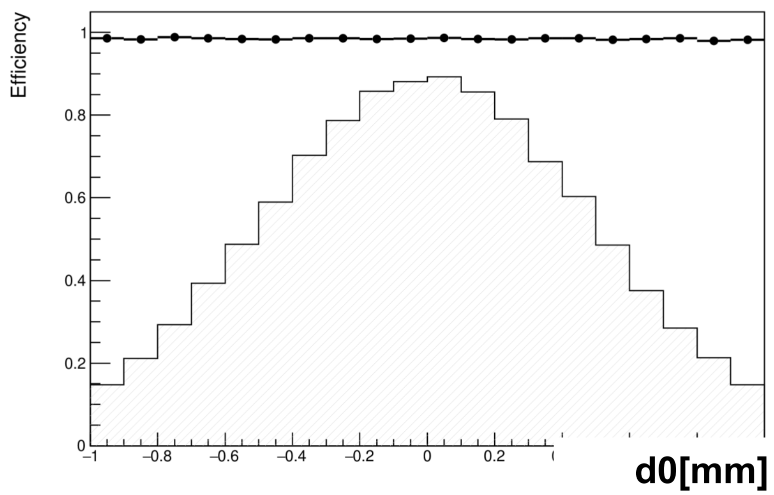
-track purity: 82% with 1200 tracks per event, using timing information

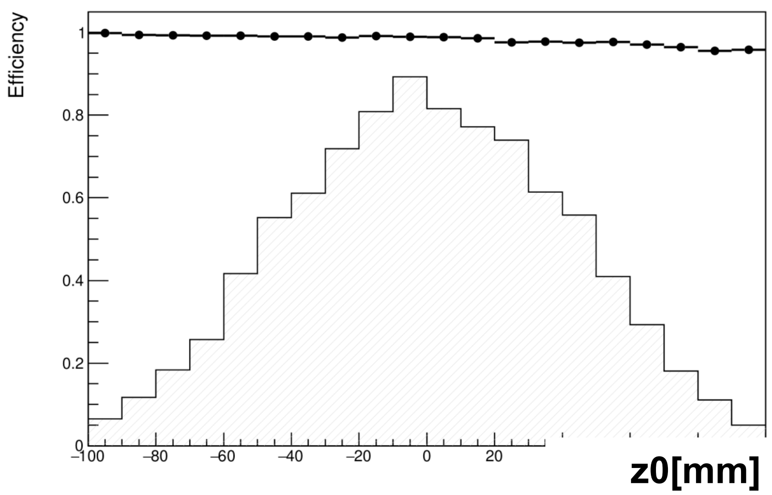
-track purity: 60 % without timing





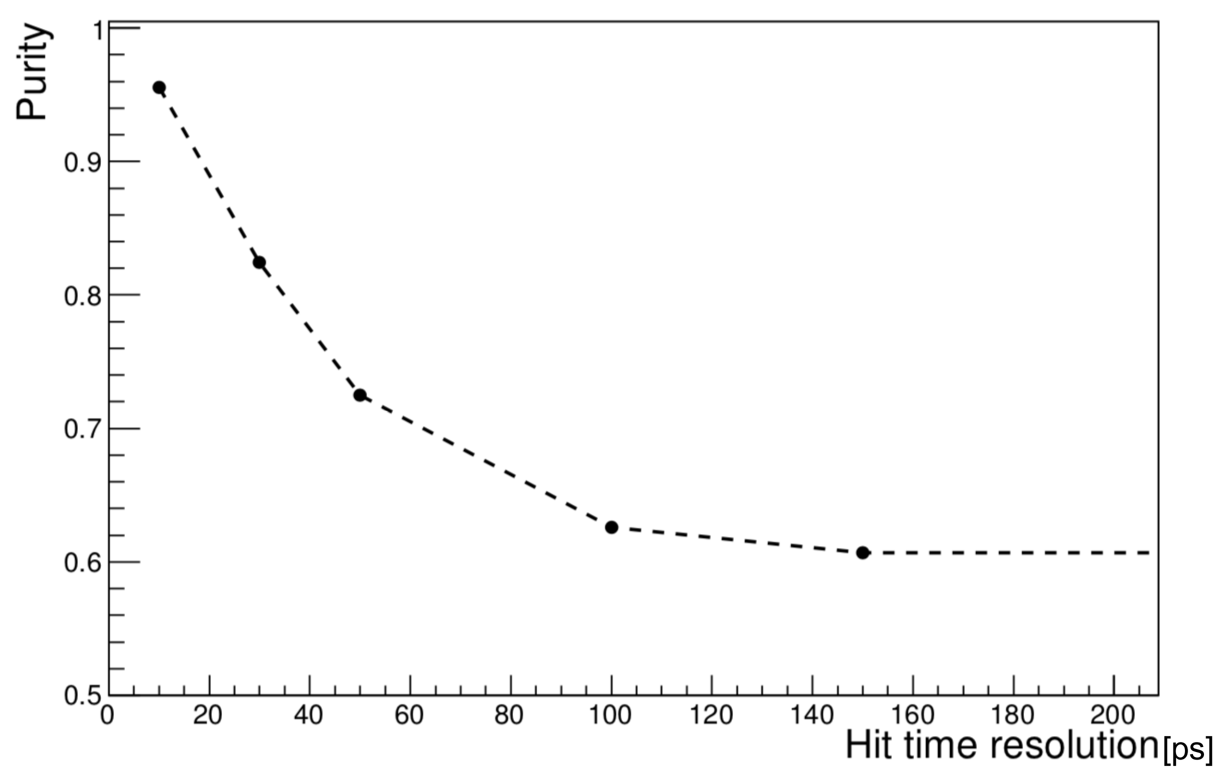


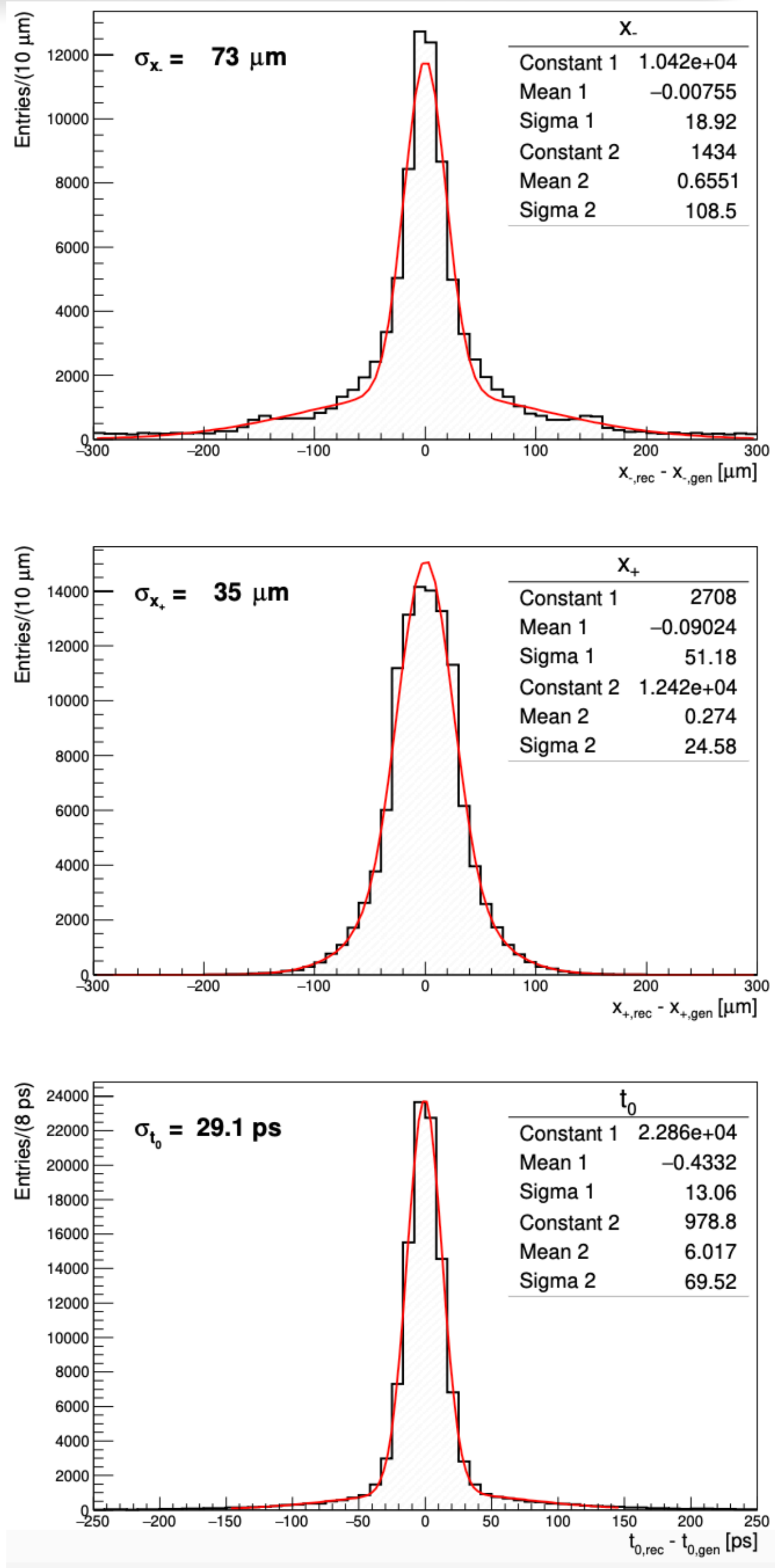




Performance vs timing

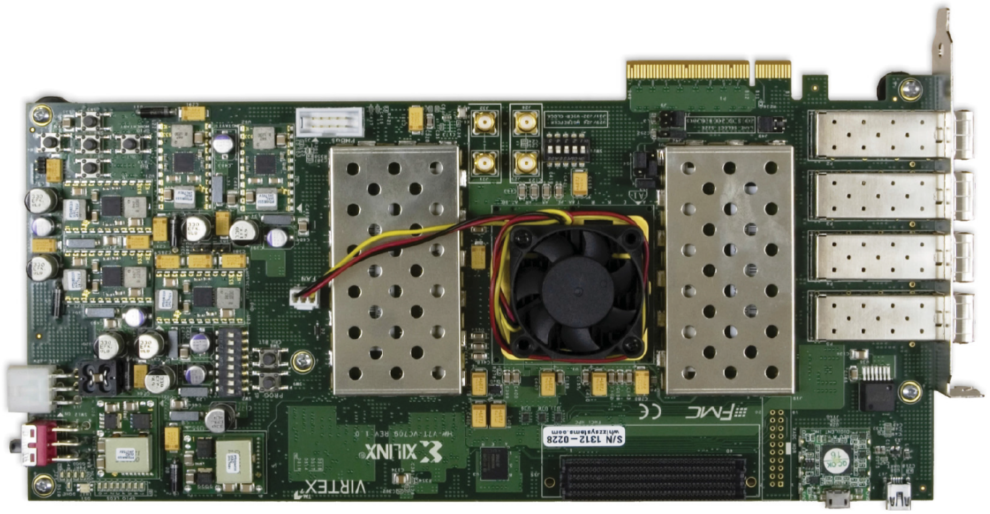
- Track **purity** improves with hit time resolution, i.e. 30 ps hit resolution very effective
- Track parameter **resolution** significantly improves with time resolution (backup slides)





Hardware implementation

Xilinx VC709 Evaluation board:



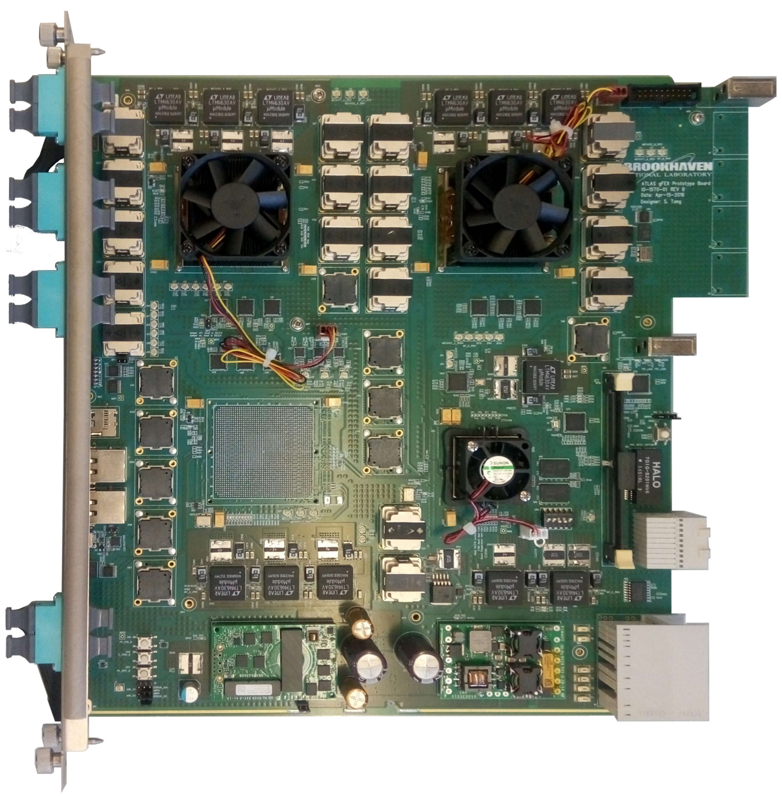
PCIe DMA, implemented using Nikhef **WUPPER** : up to 60 Gbps data transfer rate [https://redmine.nikhef.nl/et/projects/wupper]

Optical links based on GTH transceivers: 4 (up to 12) bi-directional links at **12.8 Gbps**

DDR3 RAM: 2x 4 GB banks, 100 Gbps max.read/write rate (per bank)

Stub Constructor on VC709

custom board



2 Xilinx Virtex Ultrascale FPGAs

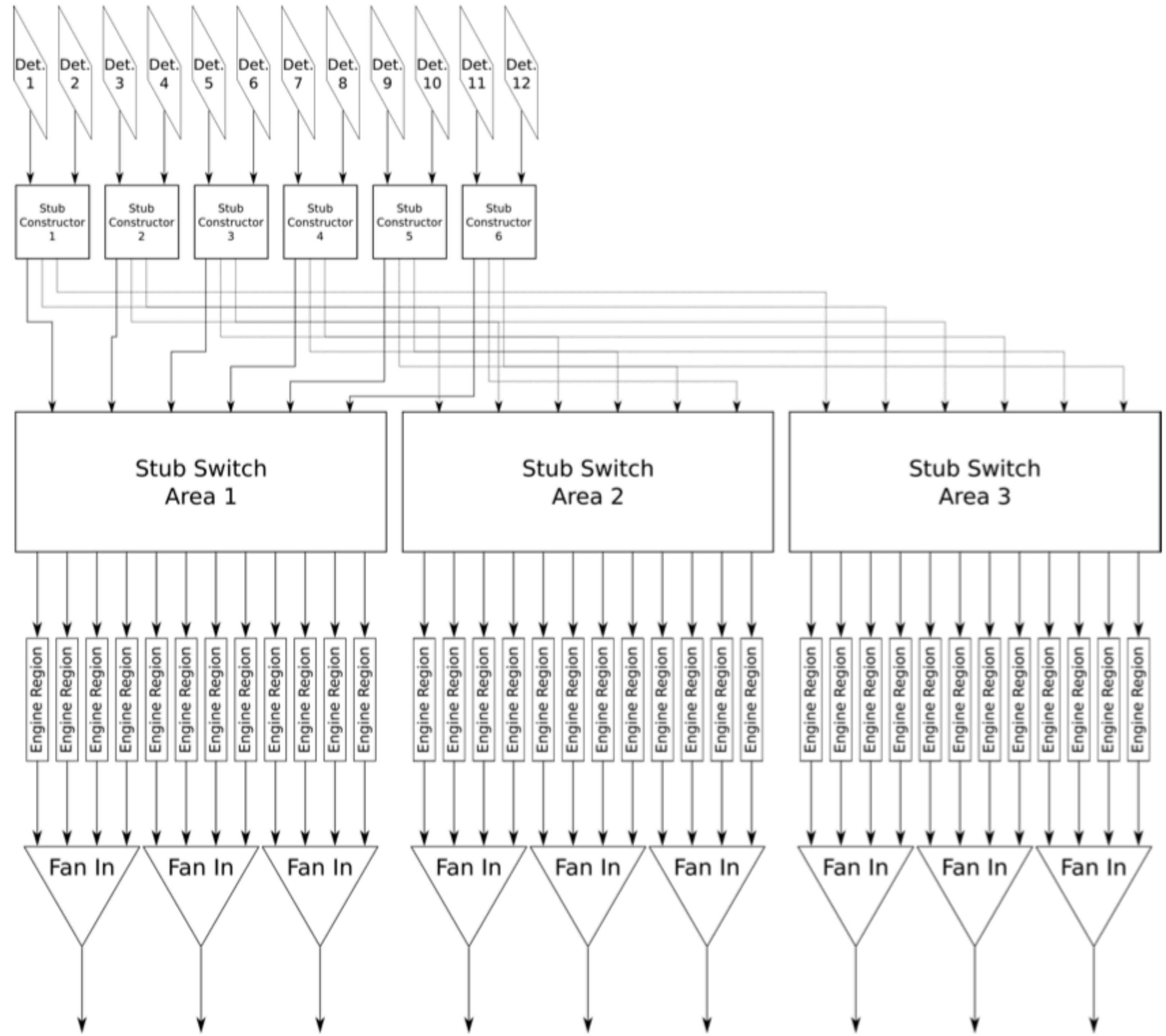
high-speed optical transceivers → **~1.6 Tbps input data rate**

one Xilinx Zynq FPGA

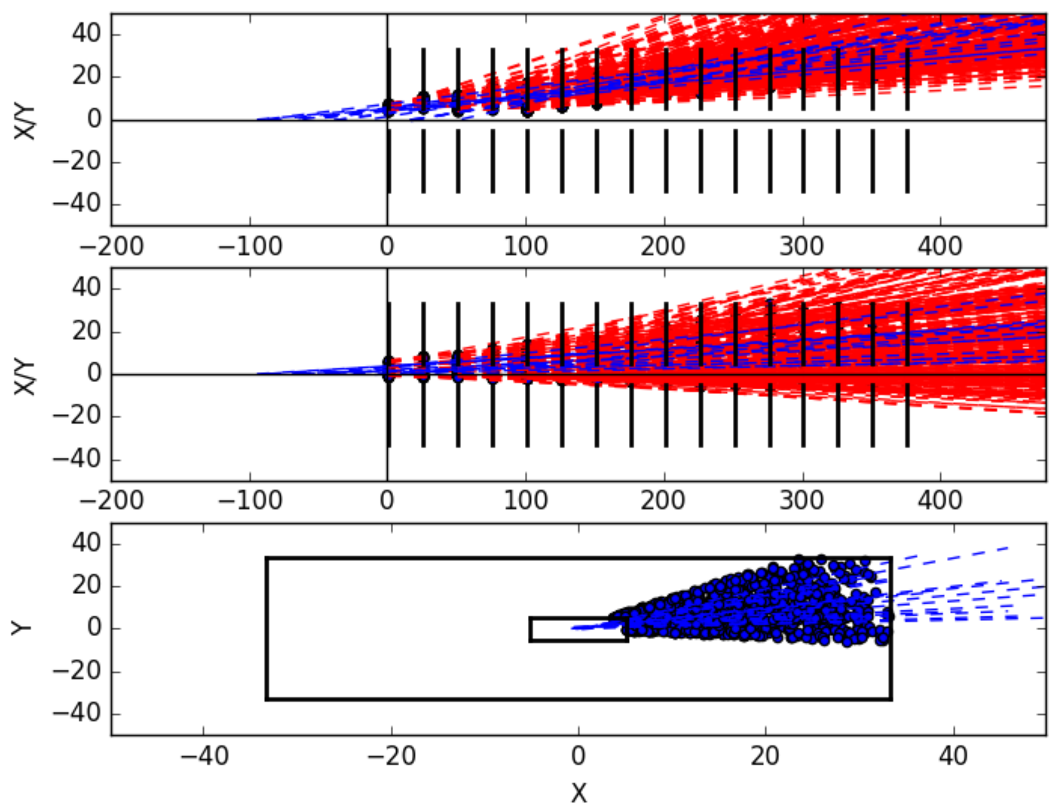
Switch + Engines + Fan In

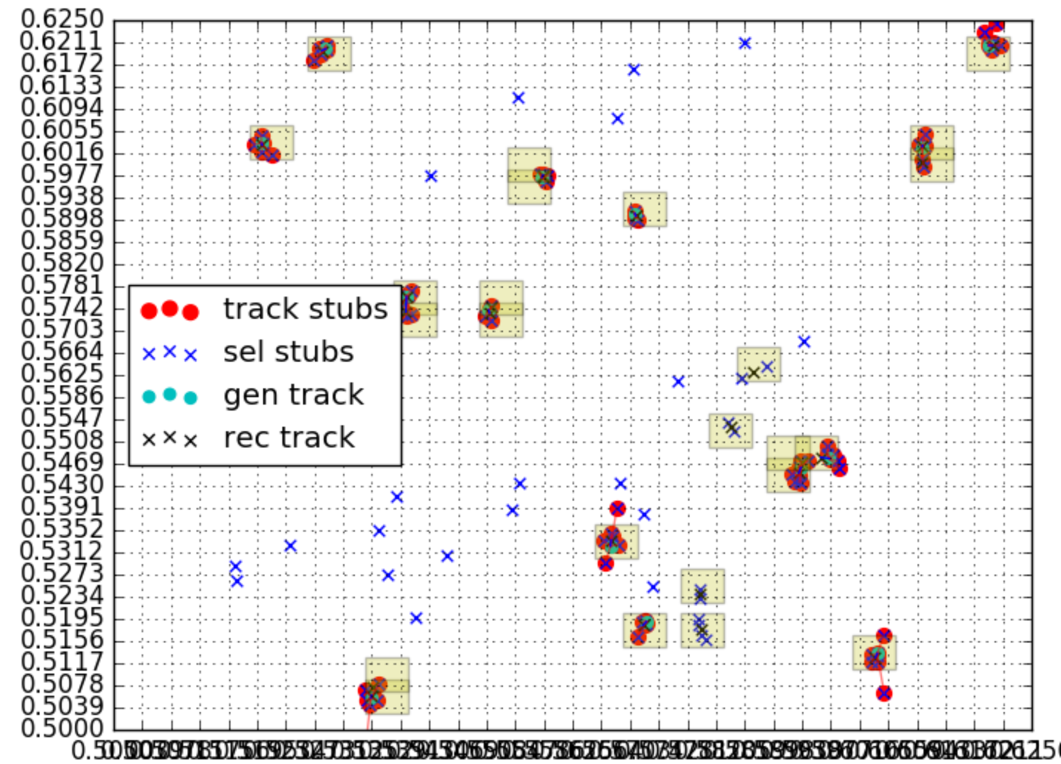
4D tracking device architecture

- Main modules :
  - stub constructor
  - Switch
  - Engines
- Hold Logic
  - prevent data losses when one module is busy



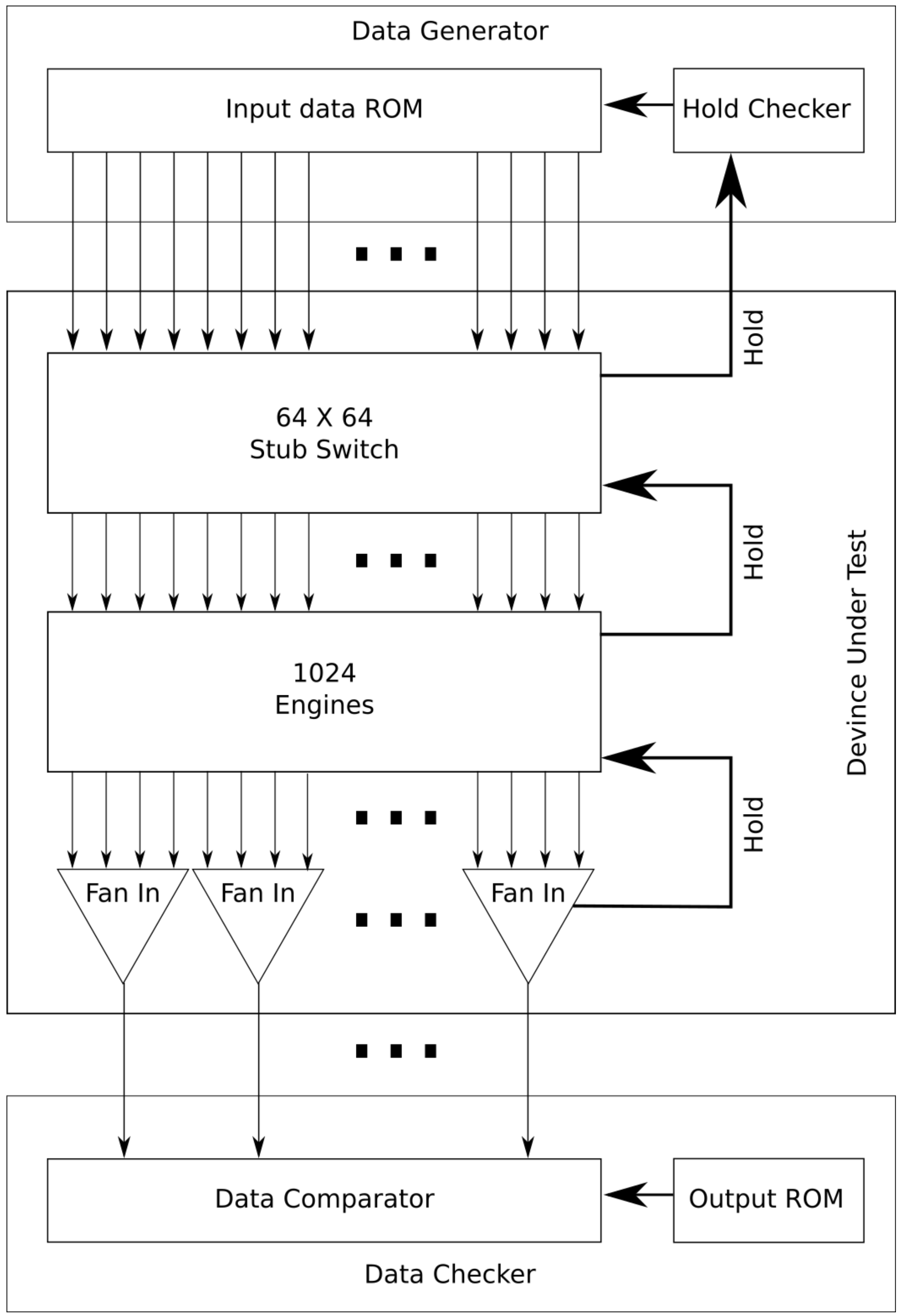
4D tracking demonstrator





- Used simulated data of 1/64 sector of the VELO-like detector: reconstruct stubs -> tracks. Evaluate rate, efficiency, latency
- System is modular and scalable: results can be extend e to full detector

Test results



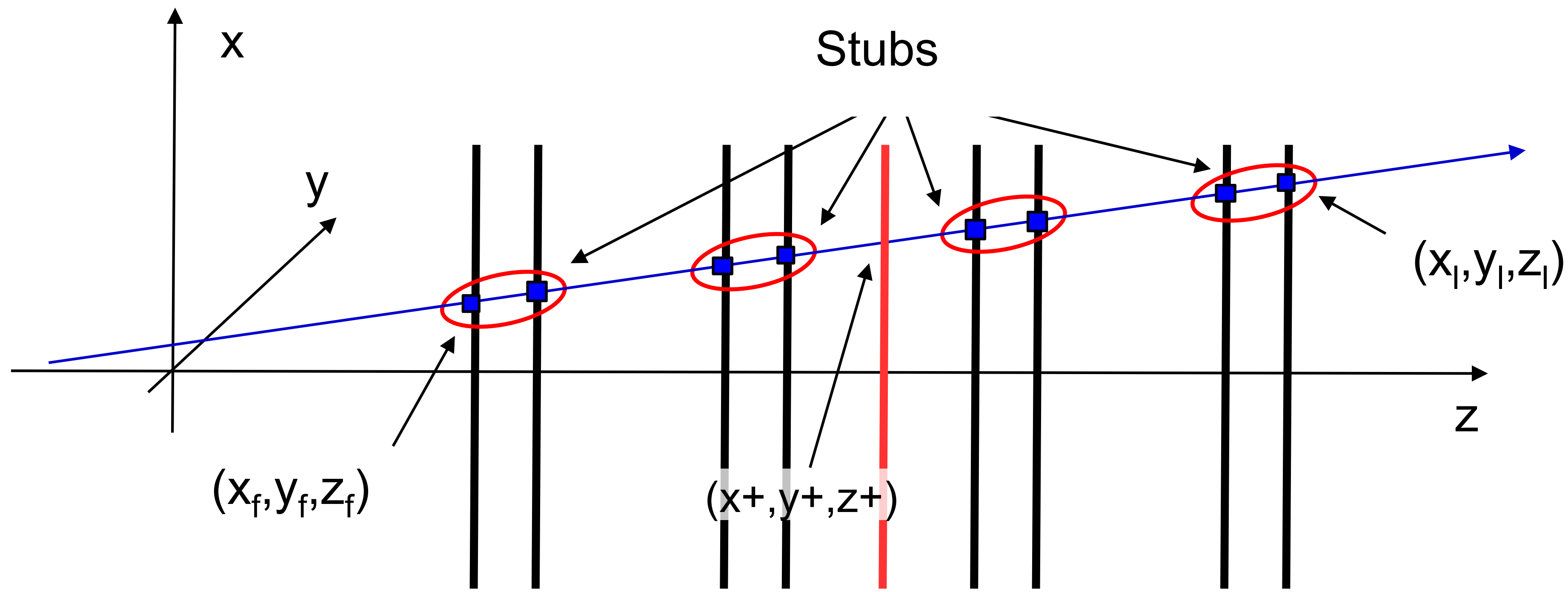
- **Fast tracking test** performed using gFEX board with 320 MHz clock
  - data generator
  - data checker
- Obtained event processing rate **40.9 MHz**
- Initial **stub maker** test on VC709 with 240 MHz clock
  - achieved 12 MHz event rate. Possibility to further parallelise the processing and achieve 40 MHz (e.g. increase number of Stub Constructors)

Summary and next steps

- A 4D fast tracking **device** for VELO-U2, simulated and implemented in FPGA, has been presented. Preliminary results are encouraging and show the viability of the solution
- **Next steps**:
  - improve **simulations** and performance studies
  - development of **clustering** algorithm in FPGA
  - upgrade from VC709 to Xilinx VCU128 **board** (1 Tb/s data rate)
  - complete the **demonstrator** test in laboratory using simulated data
  - organise a **testbed** using LHCb VELO data in collaboration with online group, possibly during Run3

Backup slides

Track parameter definitions



Coordinate system:

$(x_f, y_f, z_f), (x_l, y_l, z_l)$
: intersections of the track with first and last tracking plane

$$x_\pm = (x_f \pm x_l)/2$$

$$y_\pm = (y_f \pm y_l)/2$$

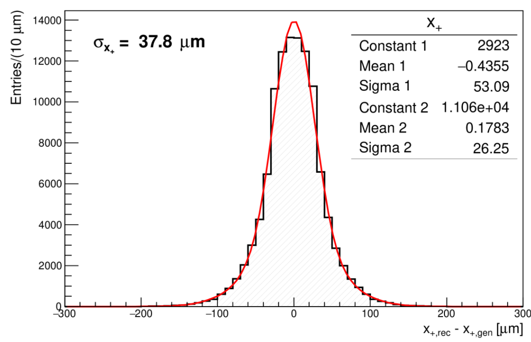
$$z_\pm = (z_f \pm z_l)/2$$

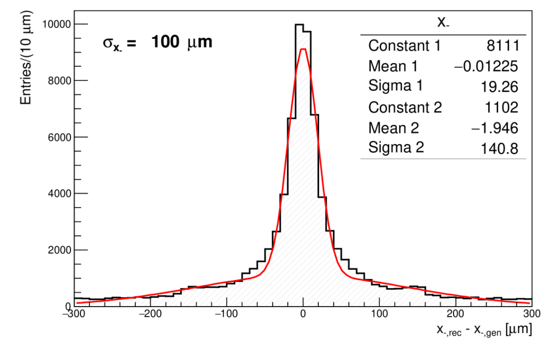
Stub parameters:

$$\begin{pmatrix} x_- \\ x_+ \\ y_- \\ y_+ \\ t \end{pmatrix}_{stub} = \begin{pmatrix} \frac{x_1 z_- - x_2 z_-}{z_1 - z_2} \\ \frac{x_1(z_+ - z_2) - x_2(z_+ - z_1)}{z_1 - z_2} \\ \frac{y_1 z_- - y_2 z_-}{z_1 - z_2} \\ \frac{y_1(z_+ - z_2) - y_2(z_+ - z_1)}{z_1 - z_2} \\ \frac{t_1 + t_2}{2} - \frac{z_1 + z_2}{2\, c\, \sqrt{1 + (x_-/z_-)^2 + (y_-/z_-)^2}} \end{pmatrix}$$

Resolution on track parameters

$\sigma_{x+/y+}$= 37.8 μm
$\sigma_{x-/y-}$= 100.0 μm

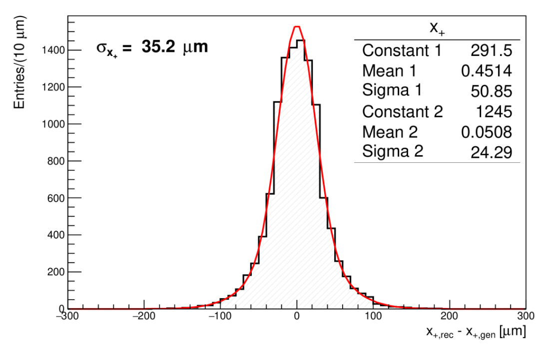


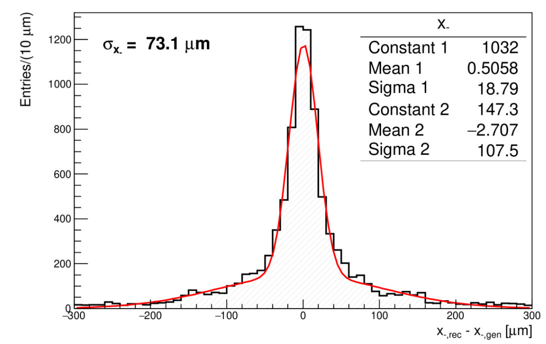


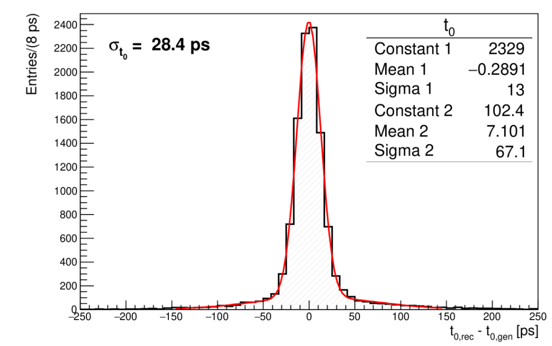
First row: resolution on track parameters (x+,x+-) **without** using the time information of the stubs
Second row: resolution on track parameters (x+,y+, t) **using the time information** of the stubs

Time

$\sigma_{x+/y+}$= 35.2 μm
$\sigma_{x-/y-}$= 73.1 μm
σ_t = 28.4 ps





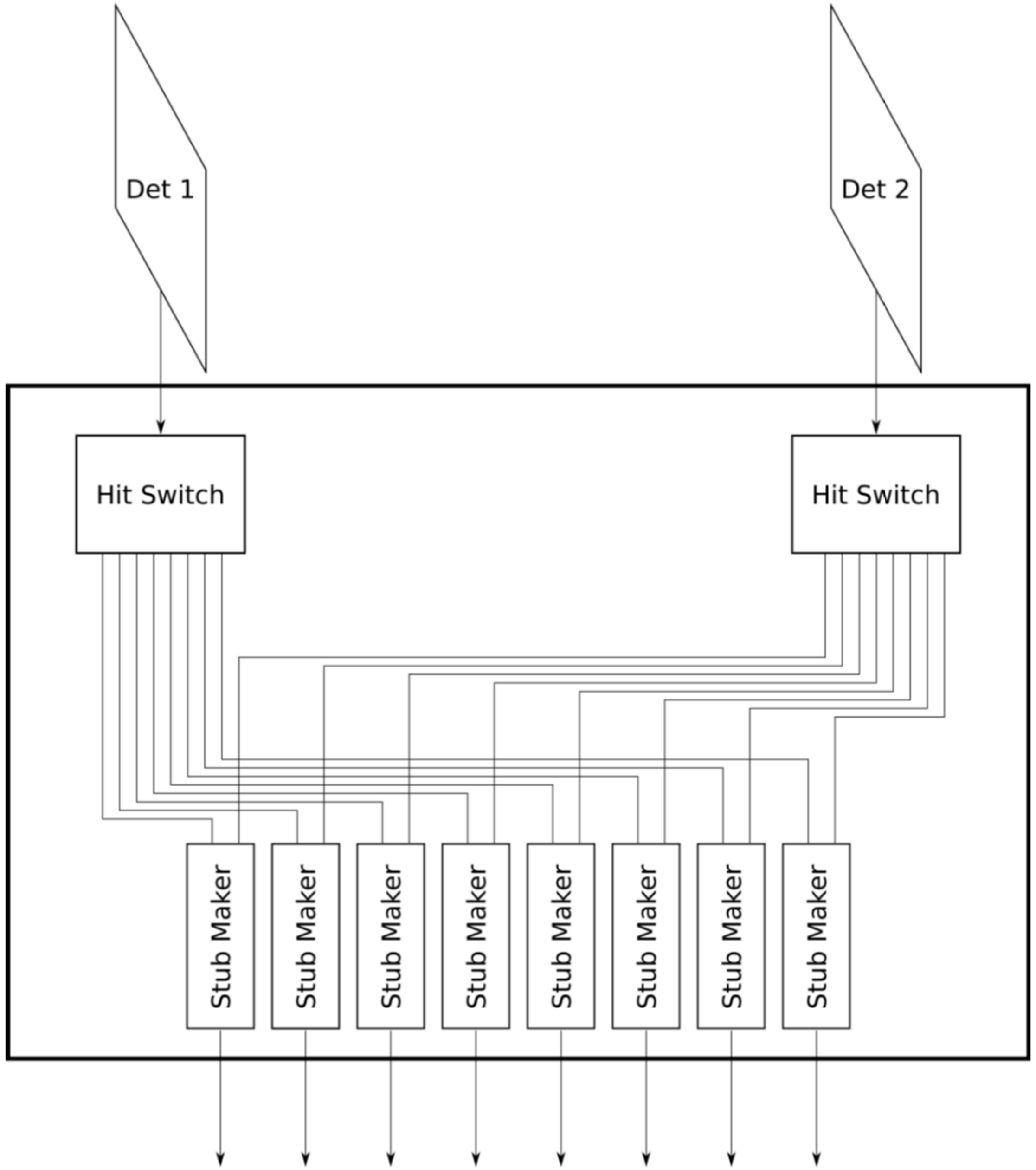


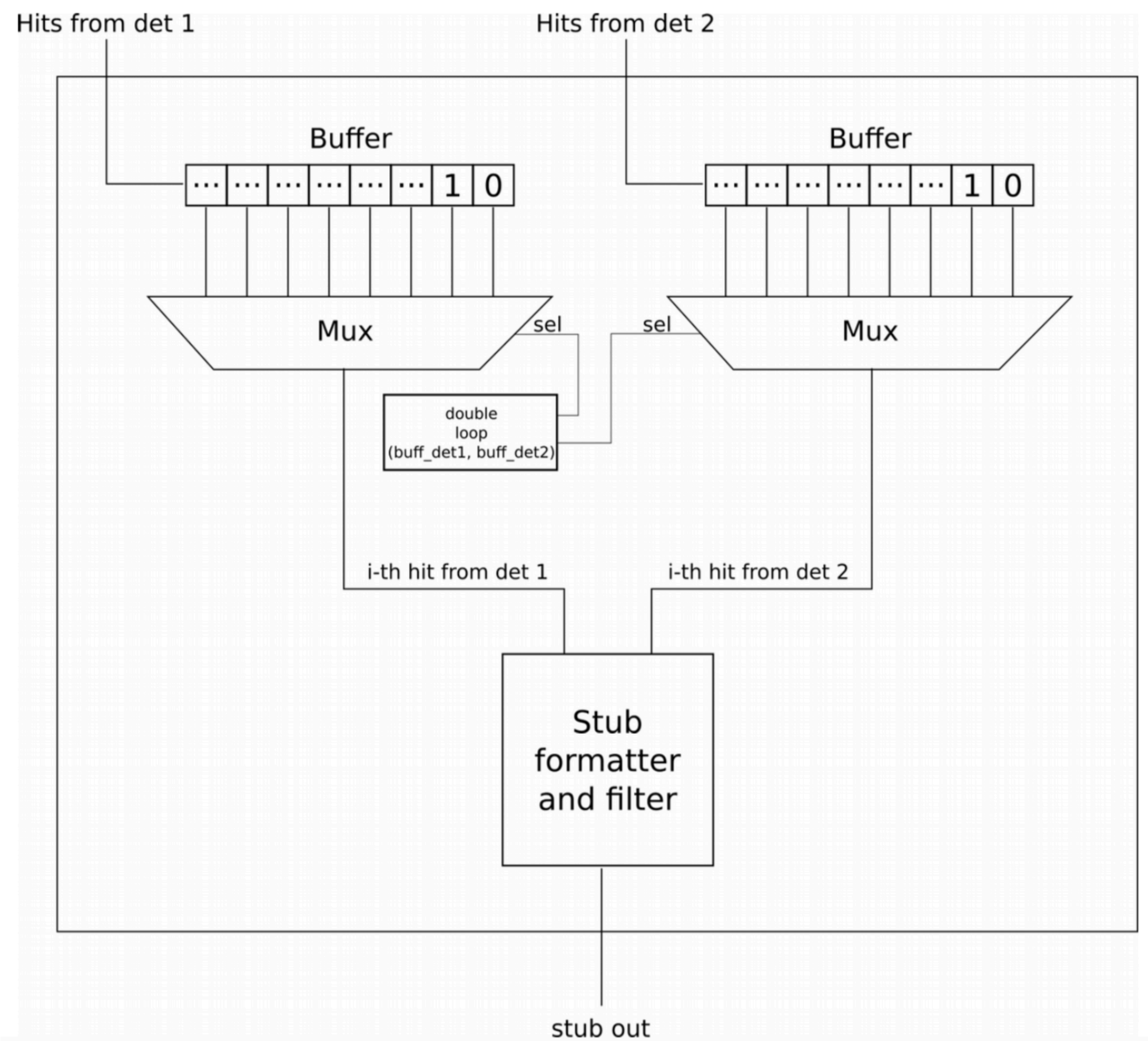
Time

- Events with 40 pp interactions, 1200 tracks per event
- 90’000 cellular units

Stub constructor

- Stub constructor module completed and tested





Stub constructor test

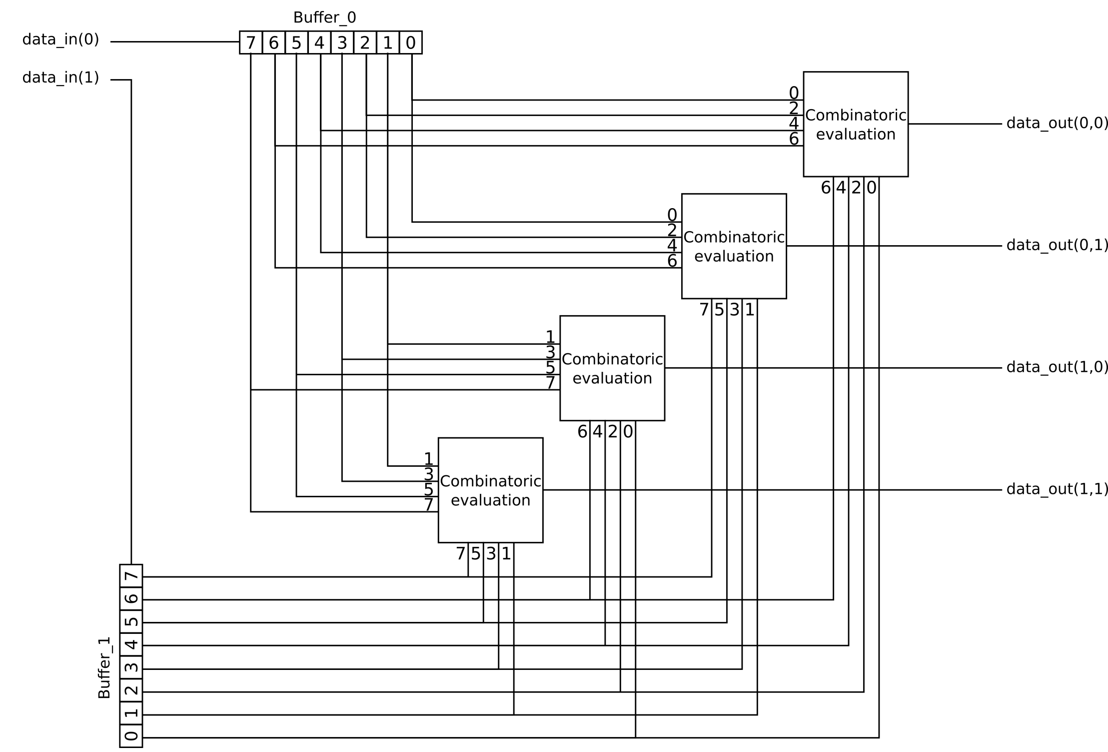
- In order to process events at 40 MHz rate in a VELO Upgrade II -like configuration, the following **equation need to be satisfied:**

$$\frac{1}{f} * Occ * N < \frac{1}{40MHz}$$

where:

  - **f = 200 MHz** is the processing clock,
  - **<Occ.> = 50%** is the fraction of Stub Makers processing data,
  - **<N> = 40** is the number of identified pre-stubs from each Stub Maker

- With this number the relation is not satisfied, and **we obtain a processing rate of 10 MHz**
  - a simple way to satisfy the relation is to **increase the number of combinatoric processes** within the Stub Makers **by a factor 4** (see fig.)



- Comment:
  - the estimation is based on a processing clock f=200MHz, this value could also be increased to enhance the acceptable event rate