# UPGRADE OF BPM SYSTEM FOR PS MULTI-TURN EXTRACTION IN TT2-TT10

BI day 2011

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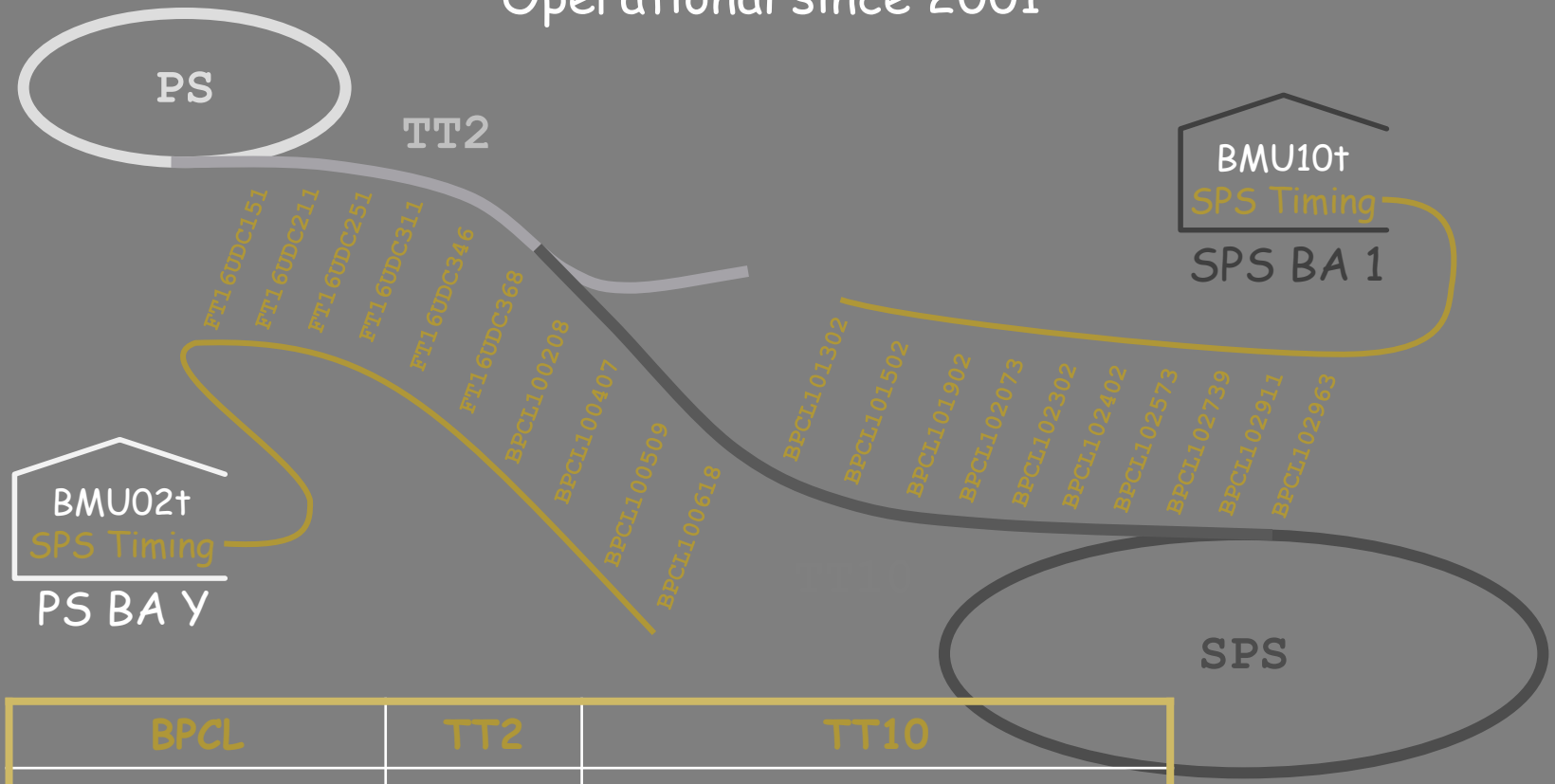
# Outline

- ✓ Overview to the TTpos system
- ✓ Proposed technical solution
- ✓ Performance of the system
  - Lab test
  - Beam test
- ✓ Planning for 2012
- ✓ Conclusions

# From PS to SPS: Today

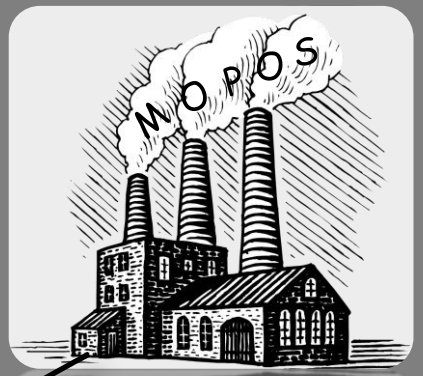
Operational since 2001

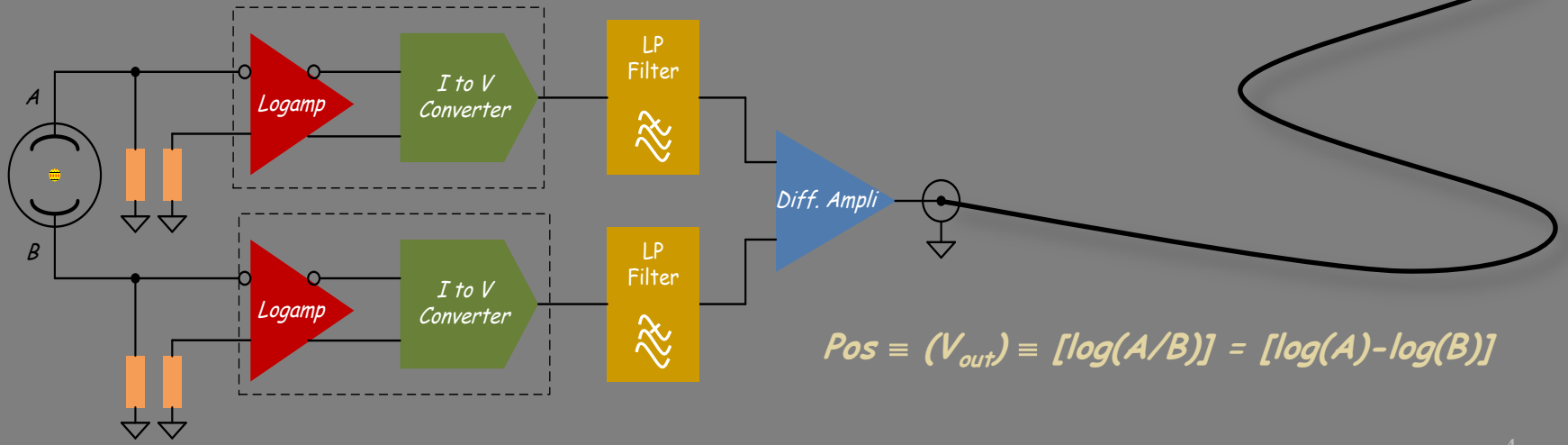



| BPCL | TT2 | TT10 |
|---|---|---|
| 2 planes 66,5mm | 6 | 14 |
| Cables length | 90 ⇨ 430 m | 160 ⇨ 620 m |
| Control | SPS | |

# Old TT2/10 BPM Electronics

- ✓ *LogAmp signals (BW < 4 MHz) are sent to the auxiliary buildings, via coaxial cables*
- ✓ *A modified version of MOPOS (SPS Position & Orbit) digitizer, with integrator and 14 bit ADC*
- ✓ *To improve S/N ratio two integration times were implemented (100 ns and 1 µs)*
- ✓ *Acquisition is identical to MOPOS system (VME power PC & PMC mezzanine)*




$$Pos \equiv (V_{out}) \equiv [\log(A/B)] = [\log(A) - \log(B)]$$

# Old TT2/10 BPM Electronics

- ✓ *BPM electronic provides one position for each SPS user*
- ✓ *Timing Issues*
  - ✓ *Logamp does not offer auto-trigger capability*
  - ✓ *Based on digital delay units individual for each BPMs*
  - ✓ *Beam and Calibration timing are different*
  - ✓ *Complex timing system*
    - *Generation of gate for integrator*

    *TTpos LSD VME Card (25nS Clock)*
    - *Fast timing ( SPS injection pre-pulses, revolution frequency) for ADC*

    *MOPOS VME Sequencer Card (100nS clock)*
    - *Slow timing (SPS GMT) to initialize elementary cycle settings*

    *BE/CO TG8 VME Timing Card (1mS clock)*

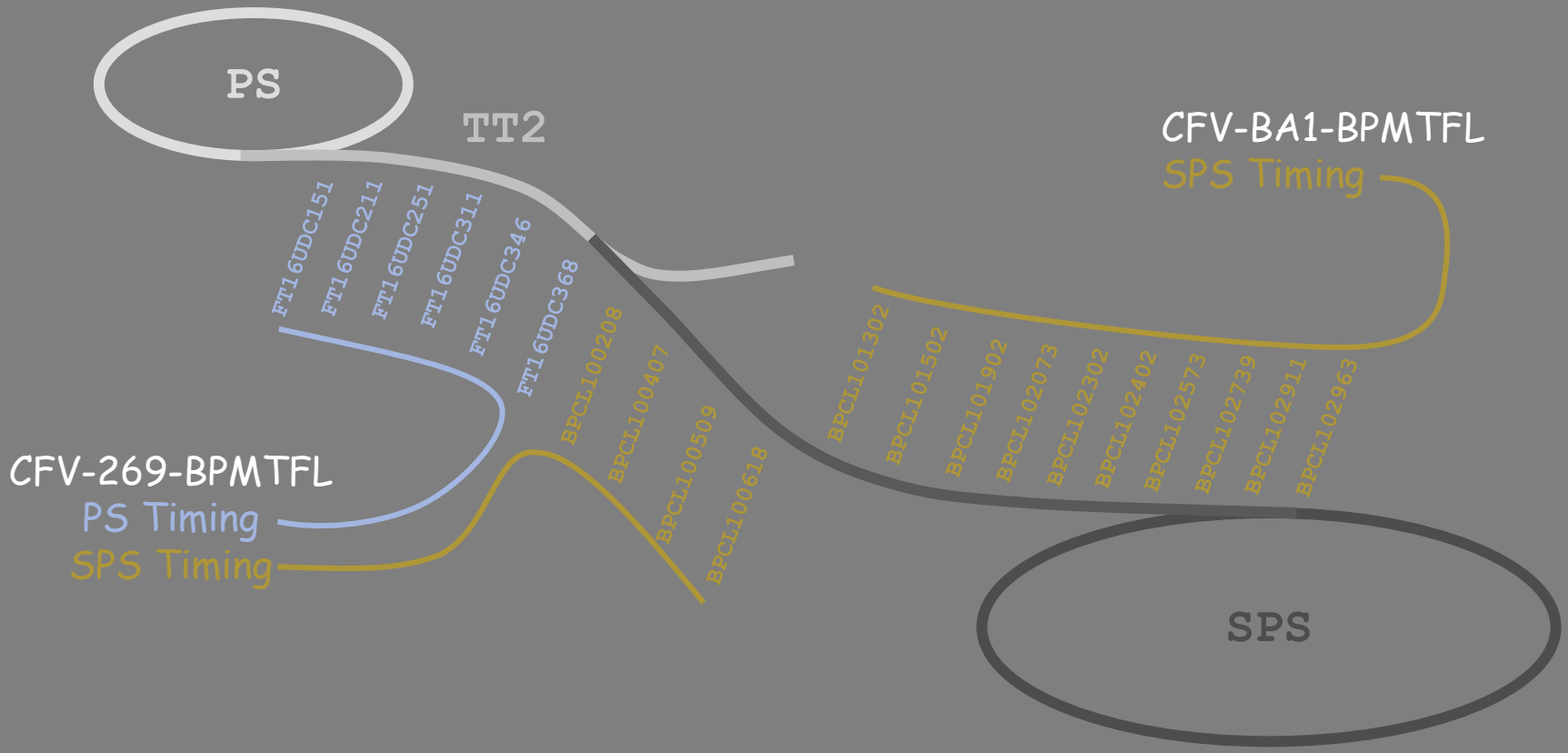
# Specifications for PS Multi-Turn Extraction

- ✓ With PS to SPS MTE extraction, we must acquire position for the five PS turns long Batch (5x2μS)

→ *New front-end electronics with a internal sequencer and a multi gate acquisition.*

- ✓ For other bunched beam only one gate acquisition is available.
- ✓ Actually, all TT2/10 monitors are on the SPS timing. Steering optimization requires that the 6 monitors in TT2 line to be put on the PS timing and controlled by the CPS crew

# From PS to SPS: New system

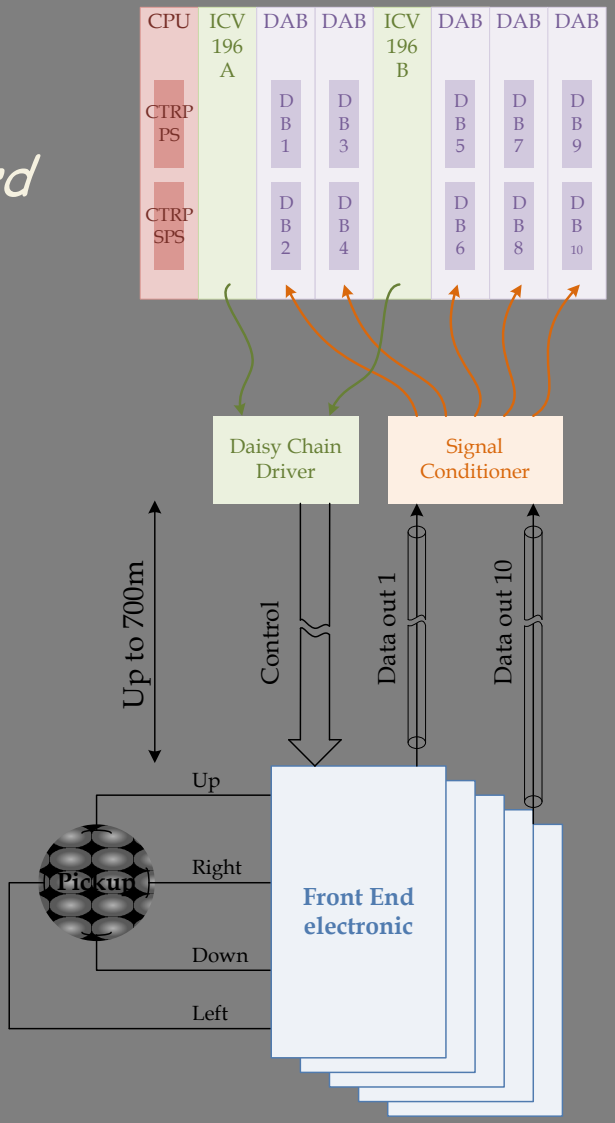



✓ Few new cables (daisy chain splitting and coax to moved the electronics away from the BPM to avoid de radiation damages)

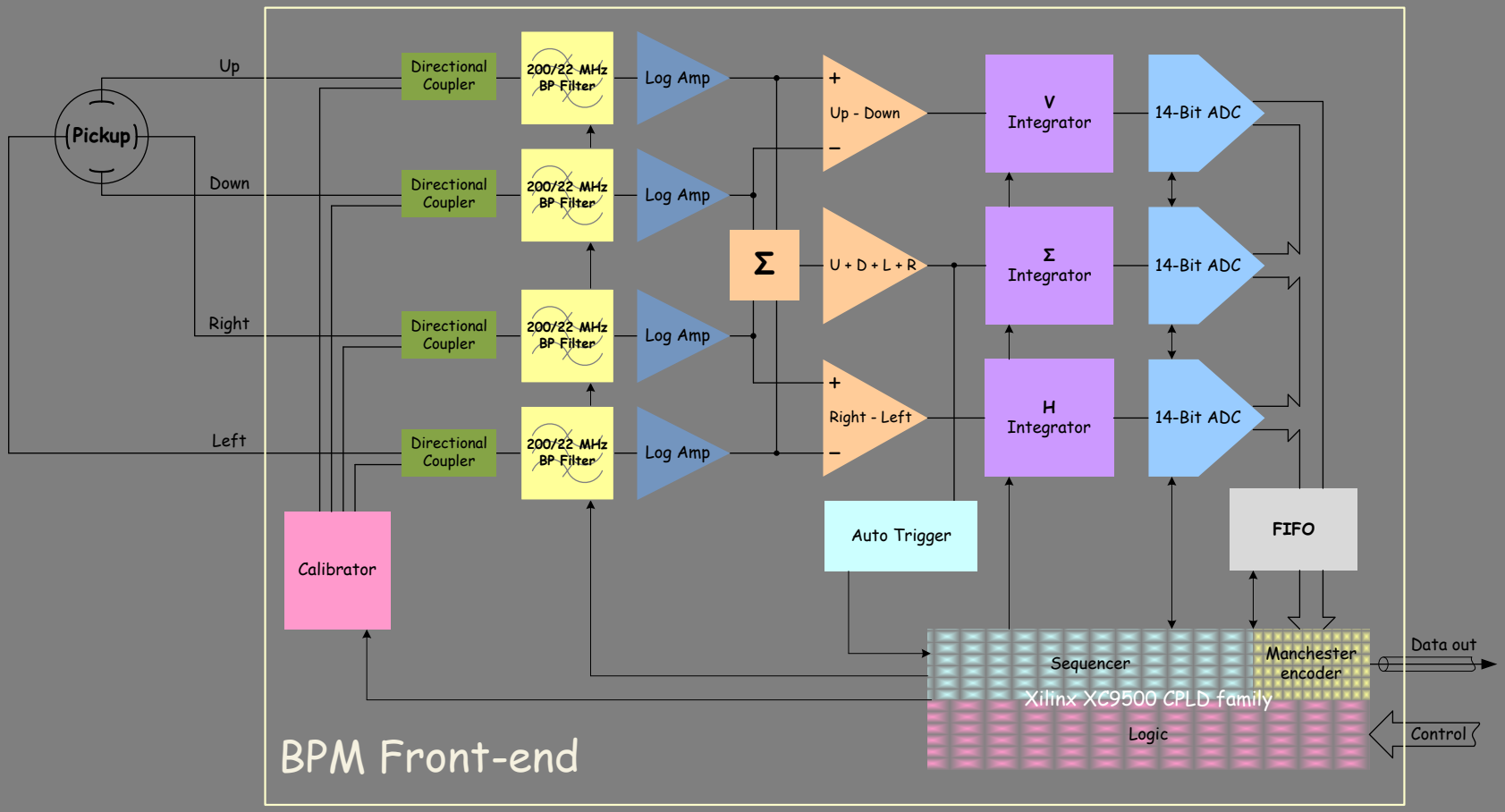
✓ Individual control and MTG timing for CPS and SPS operation

# New TT2/10 BPM Electronics

- ✓ **Acquisition System**
  - *VME 64x Digital Acquisition Board LHC DAB64x*
- ✓ **Mezzanine Card**
  - *performs Manchester decoding*
  - *Xilinx FPGA treats data to give correct input for DAB64x*
- ✓ **Final Configuration**
  - *2 VME Crates*
  - *2x5 DABs with 2x10 Mezzanines*
    *2 monitors per DAB*
  - *processing data from 20 PUs*



# New TT2/10 BPM Electronics



# New electronic Card

- ✓ Position and Intensity available
  - Large dynamic range without requiring gain switching
  - Two integration times are implemented (200 ns and 1 μs)
- ✓ Auto-triggered
  - No requirement for external timing in the tunnel
- ✓ Calibrator
  - Remotely triggered
  - Single or 40 MHz LHC bunch simulation
  - It offers 0 dB (center) and ± 5 dB ratio (slope)
- ✓ Analog to digital conversion
  - Manchester encoded data between BPM and auxiliary buildings
  - Only 1 coax cable per pick-up

# Logarithmic Normalization

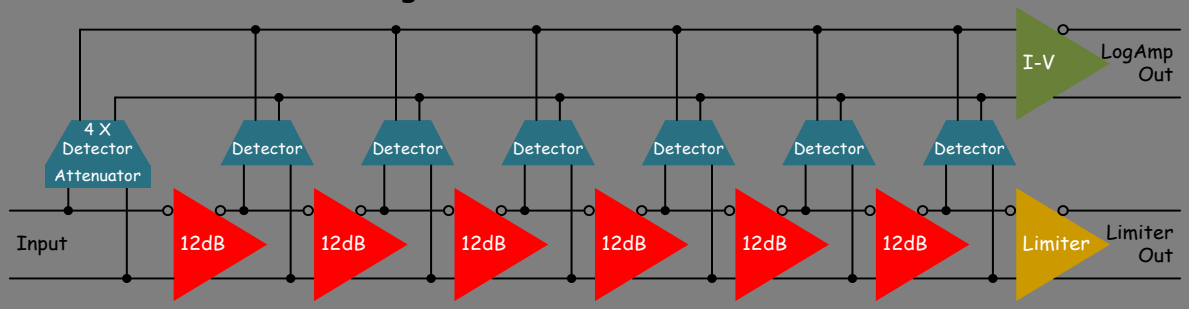
- ✓ *Each signal is compressed by a logarithmic amplifier, filtered and applied to a differential amplifier.*
- ✓ *The position response is:*

$$Pos \equiv [\log(A/B)] = [\log(A) - \log(B)] \equiv (V_{out})$$

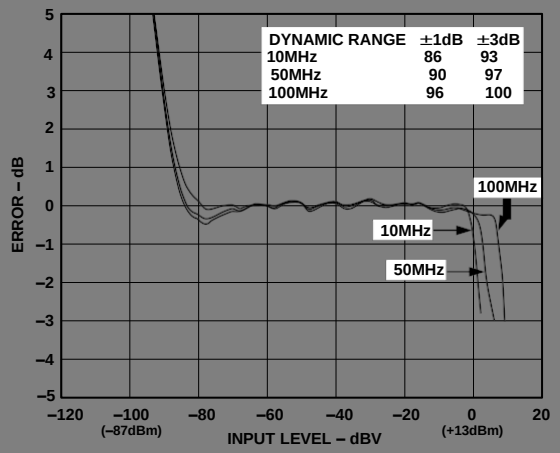
- ✓ *where $V_{out}$ is the voltage difference between the log-amp outputs.*

# Log-Amp performance

Functional Block Diagram for AD8306




Full Wave rms detectors are applied among each stage, by summing theirs output signals, a good approximation to logarithmic transfer function is obtained.




Log Linearity of RSSI Output vs. Input Level, at $T_A$ = +25°C, for Frequencies of 10 MHz, 50 MHz and 100 MHz

- ✓ Complete, Fully Calibrated Log-Limiting IF Amplifier
- ✓ 100 dB Dynamic Range: –91 dBV to +9 dBV
- ✓ ±0.4 dB RSSI Linearity up to 200 MHz
- ✓ Stable RSSI Scaling: 20 mV/dB Slope
- ✓ Input noise: < 1.5 nV/√Hz


We need less than 70dB dynamic in your application
Already used in the TT40/41 (CNGS) line

# Five 1μS gate on CNGS Beam

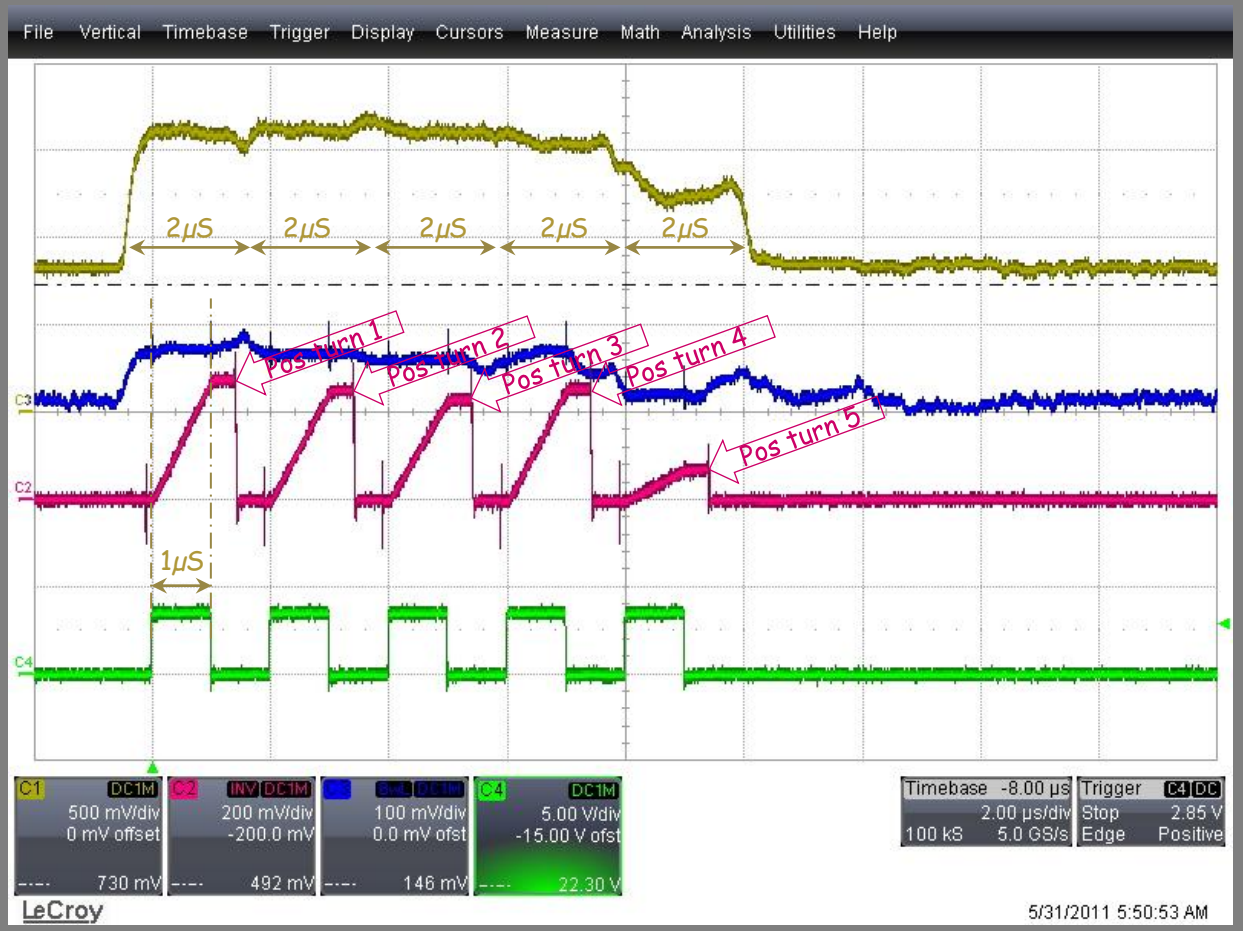
CNGS MTE 10 μS Batch (2.2E13)
2000 bunches
spaced by 5 ns

Log A

Pos ≈ Log A- Log B

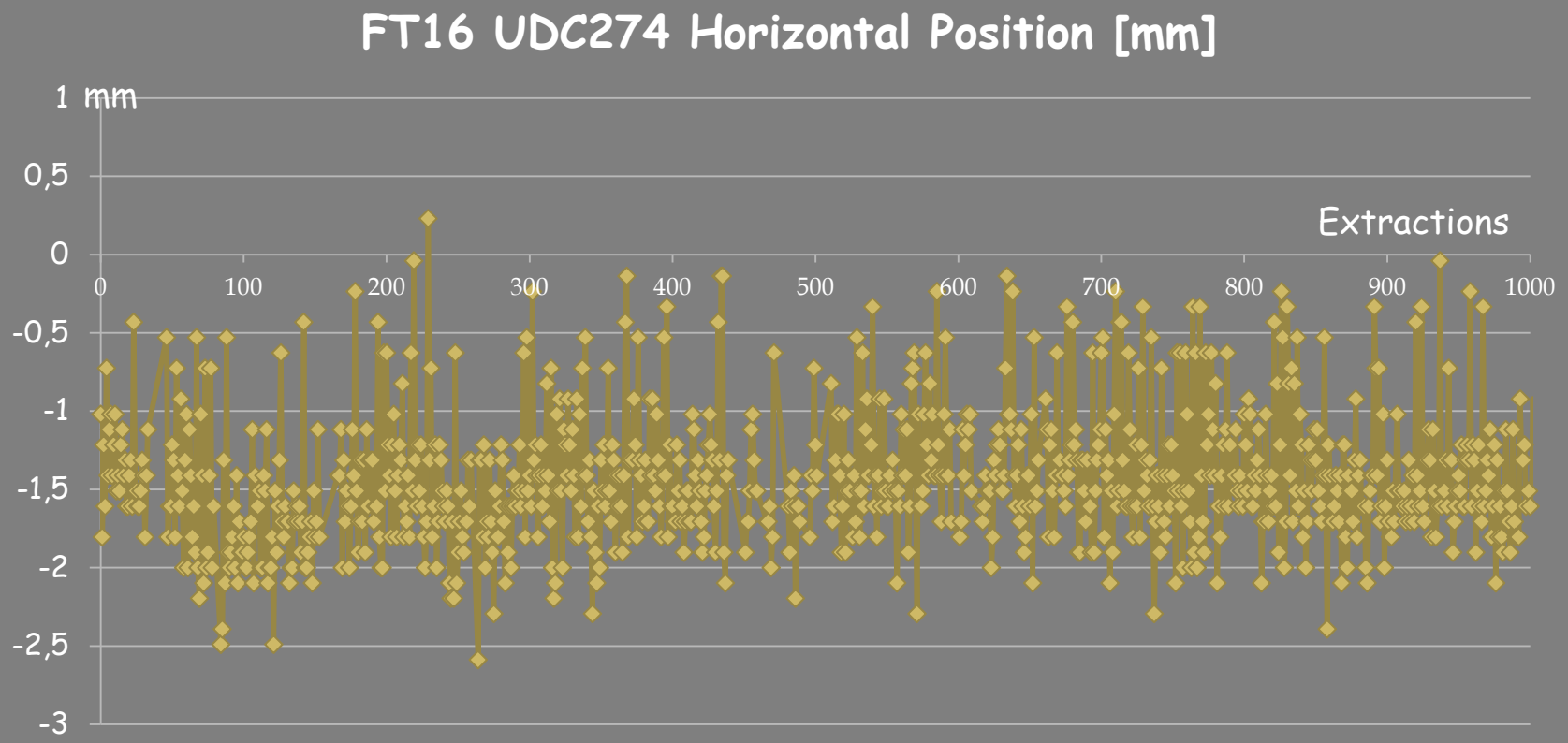
Integrator Out

Integrator Gate



# Test on heavy ions

1000 extractions with PB54 ions beam



# Conclusion and perspectives

- ✓ Electronic productions not yet done (expected to be ready by Xmas)
- ✓ Installation, test, coaxial cables & NE48 daisy chain modifications during winter stop
- ✓ Schedule: TT2/10 line will be put into operation after 2011/12 "shut-down"

# Thanks for your attention

Special thanks to : Lars Jensen, Philippe Lavanchy, CPS & SPS OP team

# Test on heavy ions

2 PB54 bunches (2x1.3E10) spaced by 200 nS

Integrator Gate

Pos ≈ Log A- Log B

LHC Ion PB54

Log A