

# Optimising Cryogenic Wiring for Superconducting Qubit Processors in a Dilution Refrigerator

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Quantum computers require high-precision control and must be strongly isolated from their environment and spurious noise. Superconducting qubits must be operated at cryogenic temperature where the local thermal energy is far below the typical 4-8 GHz qubit transitions to protect their fragile information. Optimising the cryogenic wiring which connects the devices to their microwave control electronics at room temperature is an important ongoing challenge, as large quantum processors require many control lines, and these lines provide an open channel for noise and heat to propagate directly to the qubits [1]. This creates competing demands on both heat loads and input noise, addressed primarily through attenuation and filters. This becomes an increasingly delicate balance as we approach the finite spatial and cooling capacities of dilution refrigerators, especially as device noise floors improve. With processors scaling to hundreds and thousands of qubits and control lines, this is quickly becoming an important factor for maximising the computational power of industry-scale superconducting quantum computers [1]. Importantly, even small gains in refrigerator and qubit capacities result in exponential increases in a platform's quantum computing power.

In this work, we built a comprehensive numerical model of a full cryogenic wiring setup to simulate these effects and identify optimal wiring configurations for different heat, noise, and operational constraints (Fig. 1 a,b). This model allowed us to evaluate and compare many different configurations (see, e.g., Fig. 1 c,d), giving optimised solutions that suggest several opportunities to improve designs informed by the conventional rules of thumb and heuristics commonly employed in the community. We studied this model primarily in the context of dilution refrigerators designed to run custom, modest-scale circuit QED devices, but also discuss broader contexts relevant to industry processors and identify potential avenues for improving large-scale refrigerator capacities.

[1] S. Krinner et al., EPJ Quantum Technology 6 (2019)

Fig. 1: a) Optimised cryogenic wiring design, developed using numerical modelling. b) Heat loads on each stage from the design in a). c) Noise current at the device flux current input, for different attenuator values on the 4K and 50K. d) Noise photons at the device drive input, for different splits of 60dB across the MXC, CP, and 4K.

