Device design for detecting topological signatures in quantum wires

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In recent years enthusiasm has grown for quantum hardware that can host topological states, useful for robust quantum computing and dissipationless electronics as well as more fundamental physics. Quantum wires with spin-orbit and superconductivity that could host bound Majorana zero modes and p-wave superconductivity are an attractive platform to study as the quantum states are easily manipulated with gate voltages, similar to ordinary transistors. However reproducible fabrication of 1D systems, and consequently reproducible topological behaviour, has been an ongoing challenge. Furthermore, there has been a substantial gap in our understanding of how lithographic gate design maps to the electrostatic landscape inside quantum wires, restricting our ability overcome the problems of low reproducibility and low visibility of topological signatures that are often masked by interaction effects and disorder.

Our approach uses quantum point contacts (QPCs) – lithographically defined quantum wires that we can accurately tune to achieve highly reproducible conductance with specific spin-orbit properties. In our theory/experiment collaboration, our real devices are numerically simulated to understand how gate design and fabrication imperfections manifest in measured conductance. We are for the first time able to carefully design devices with known electrostatic confinement dimensions, providing a pathway to scalable topological quantum hardware.