# RD50-MPW3: Design and initial laboratory evaluation

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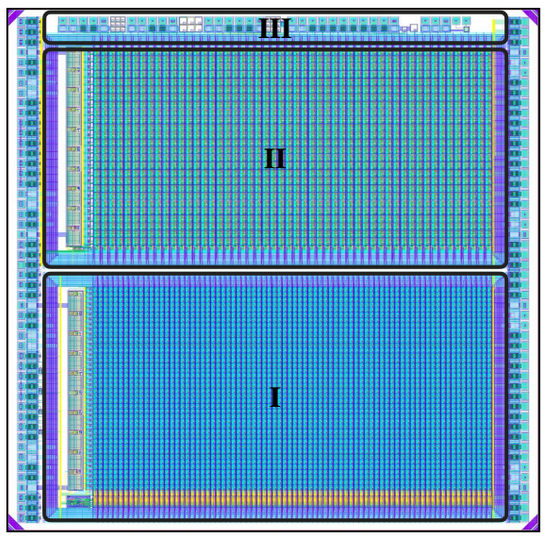
# Introduction

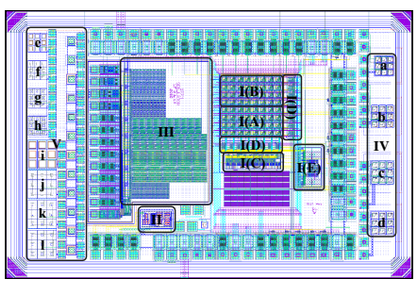
- **CERN-RD50 CMOS Working Group** make efforts in:
  - ASIC design;
  - TCAD simulations;
  - DAQ development;
  - Chip performance evaluation.
- Currently involves 17 institutes.
- A series of HV-CMOS prototypes have been developed using LFoundry 150 nm HV-CMOS process.

# RD50 HV-CMOS Prototypes

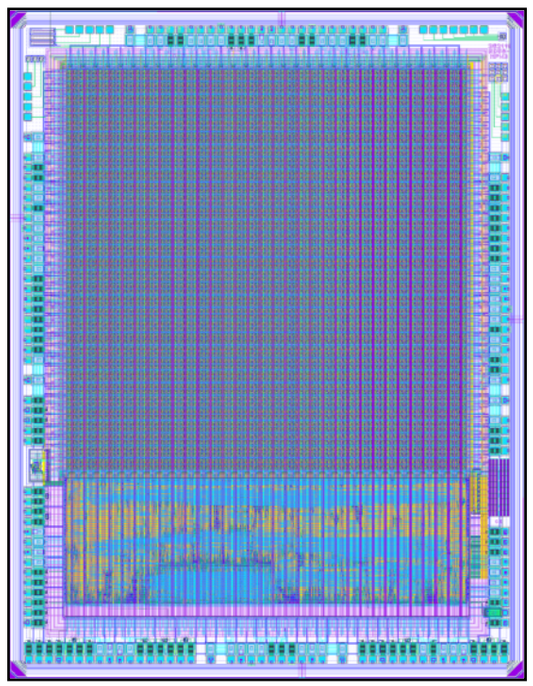
**RD50-MPW1**
received in Apr. 2018




**RD50-MPW2**
received in Feb. 2020



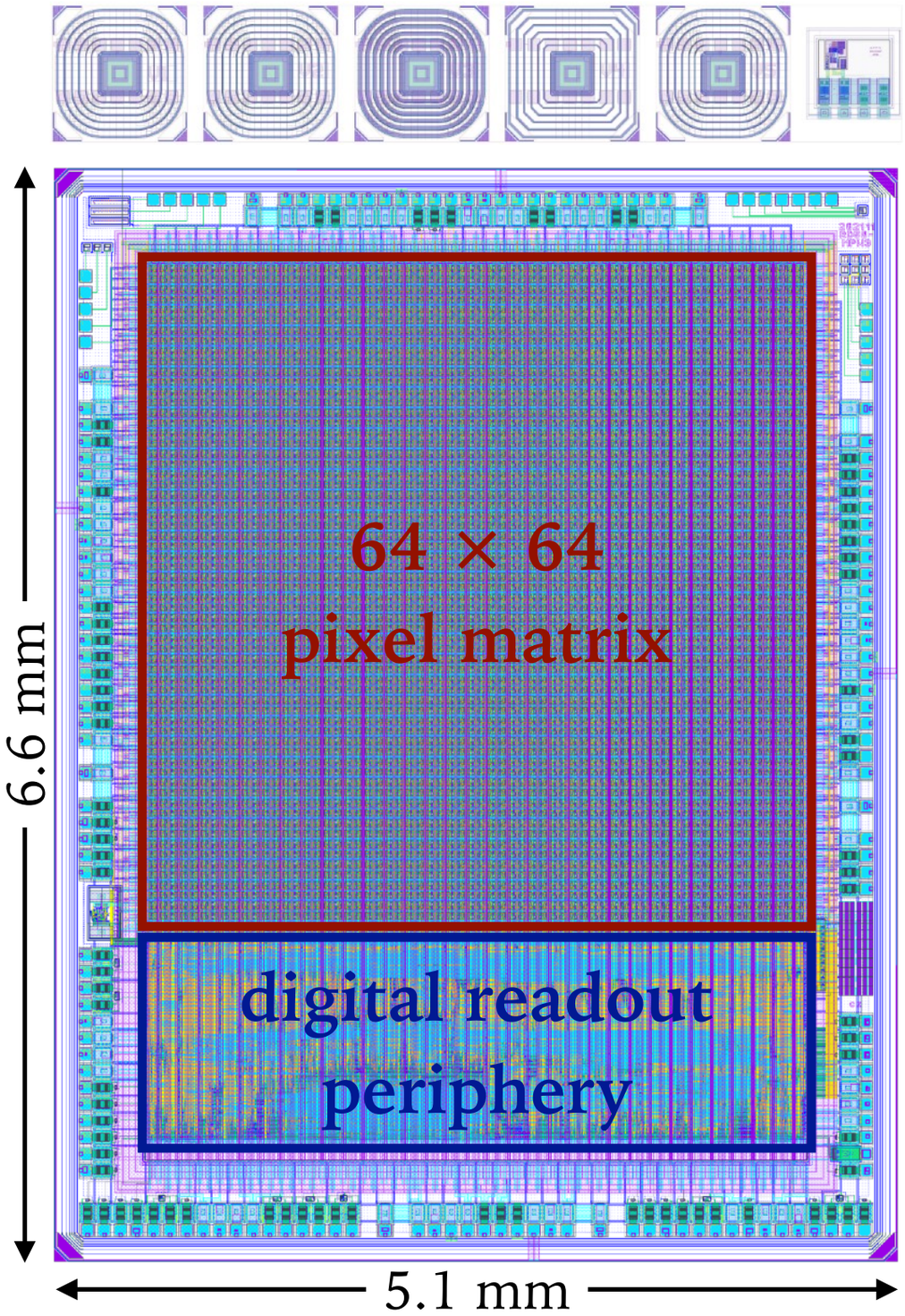

**RD50-MPW3**
received in Aug. 2022



- **RD50-MPW1**: test the LF150 process, low $V_{BD}$ (55 V) and high $I_{Leak}$ (~ $\mu$A).
- **RD50-MPW2**: high $V_{BD}$ (130 V), low $I_{Leak}$ (~ nA) and fast analog front-end.
  Small pixel matrix (8×8), no in-pixel digital readout, no digital readout periphery.
- **RD50-MPW3**: larger pixel matrix (64×64) with in-pixel digital readout and advanced peripheral readout.
- This talk gives an overview description of RD50-MPW3 and presents its initial laboratory evaluation results.

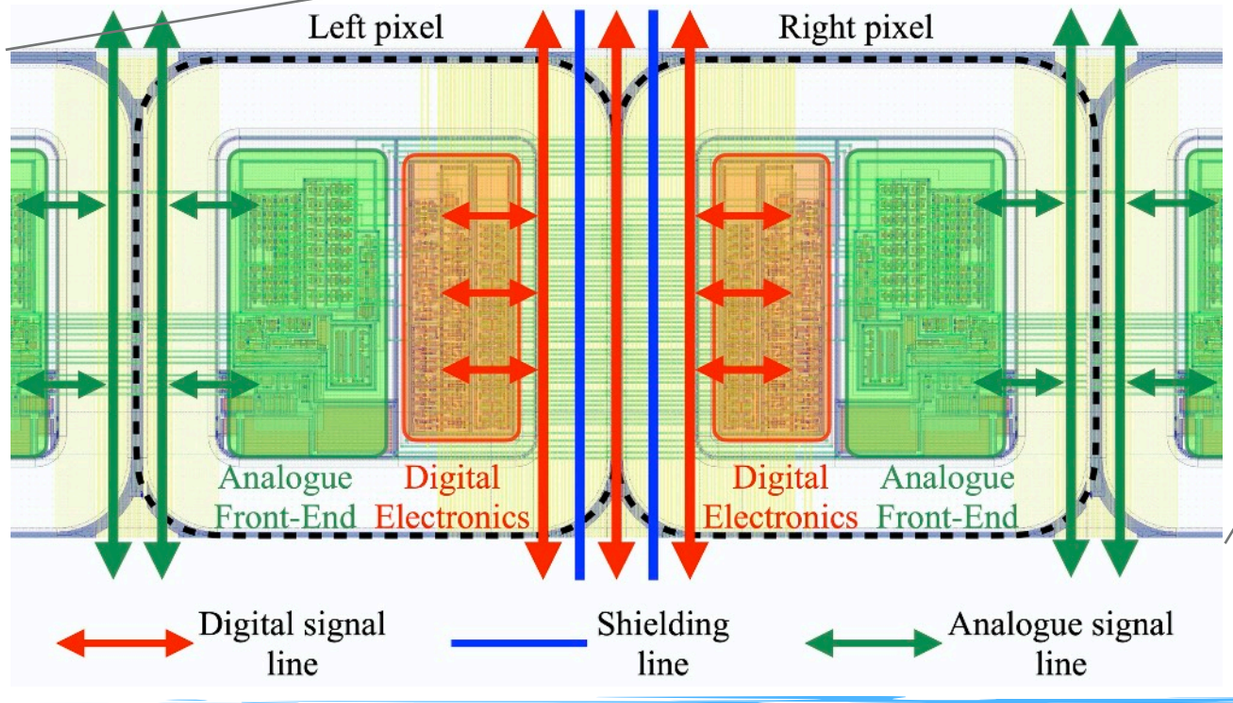
# General details of RD50-MPW3

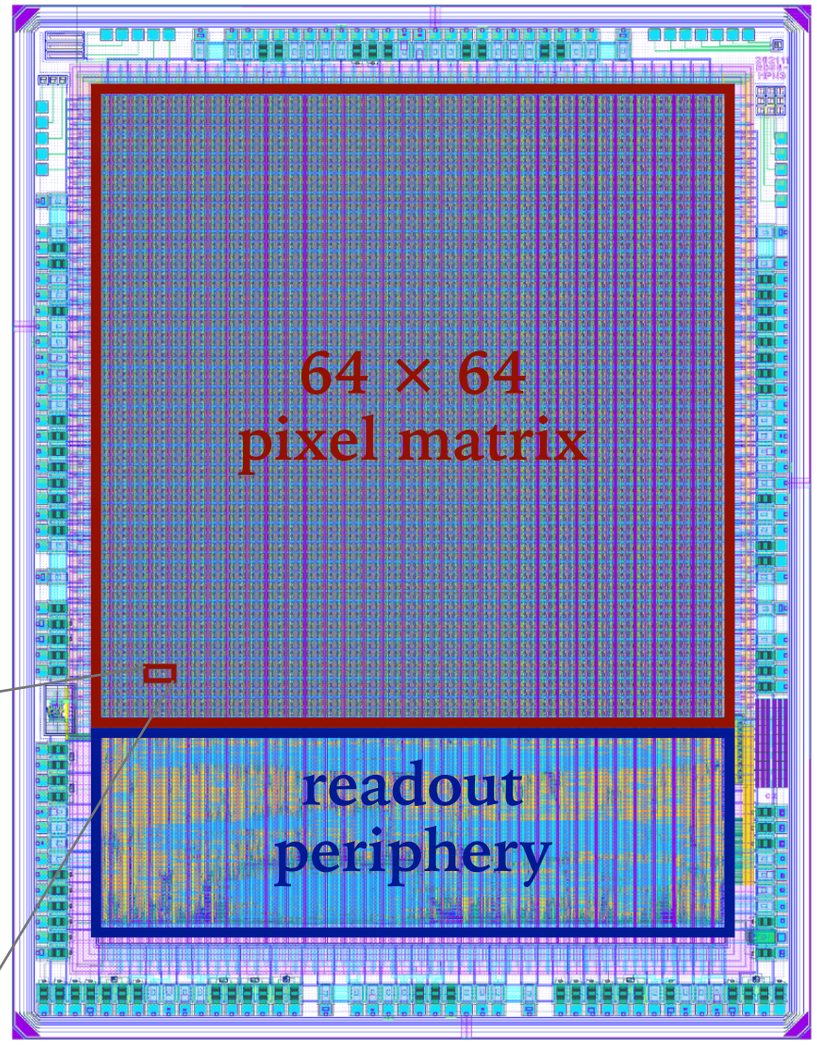
- **RD50-MPW3** is designed based on lessons learnt from the previous two chips:
  - ➤ same chip ring for high $V_{BD}$; low $I_{Leak}$;
  - ➤ fast analog front-end.
- Mainly composed of a pixel matrix, a digital readout periphery and test structures.
- Wafers with different resistivity (3 × 1.9 kΩ·cm, 1 × 3 kΩ·cm and 1 × 10 Ω·cm).
- New features in RD50-MPW3:
  - ➤ double-column architecture;
  - ➤ FE-I3 style digital readout circuits;
  - ➤ optimised digital periphery for effective chip configuration and fast data transmission.
- **RD50-MPW3** was submitted for fabrication in Dec. 2021, and was received in Aug. 2022.



# Pixel Matrix

- 64 columns are organised into 32 double columns.
- To save area and avoid crosstalk between digital and analog signals:
  - ➤ Digital signal lines are placed in the middle of each double column;
  - ➤ Analog lines are placed between double columns;
  - ➤ Shielding lines (grounded) are inserted between digital signal lines to minimise coupling.
- A power grid using Metal 5 and Metal 6 is used to minimise IR voltage drop.

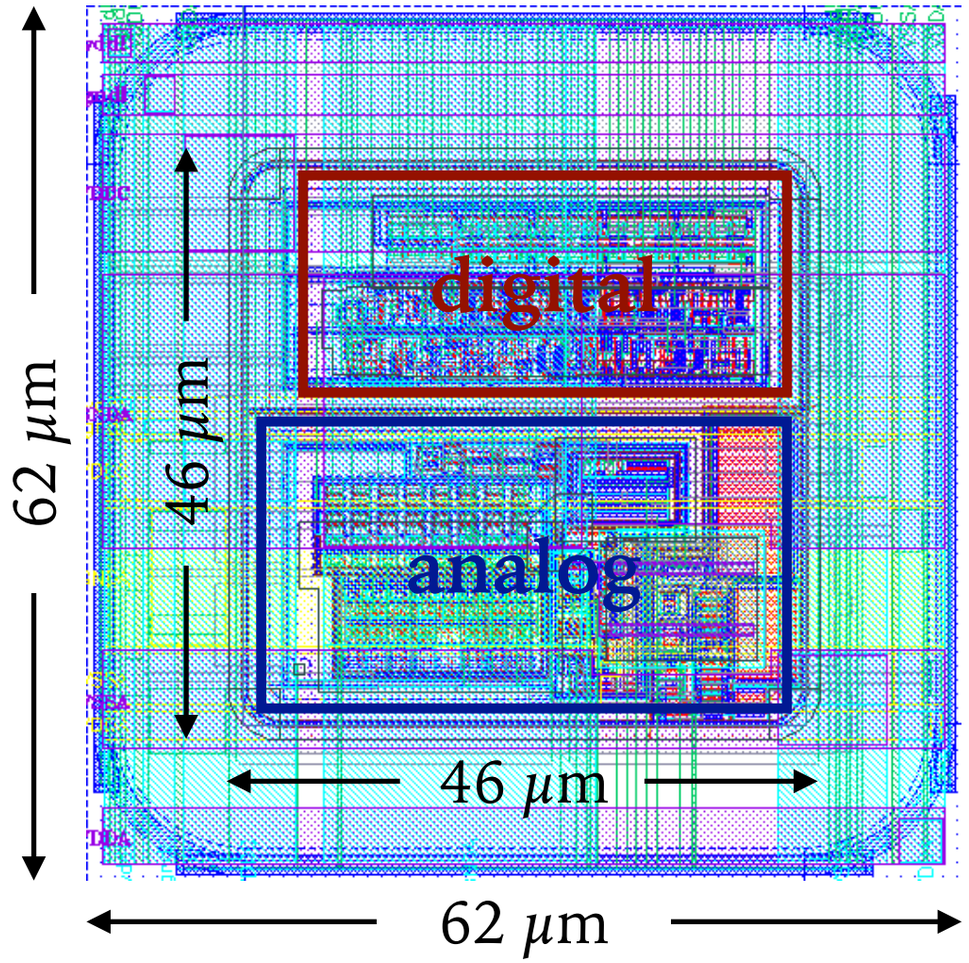


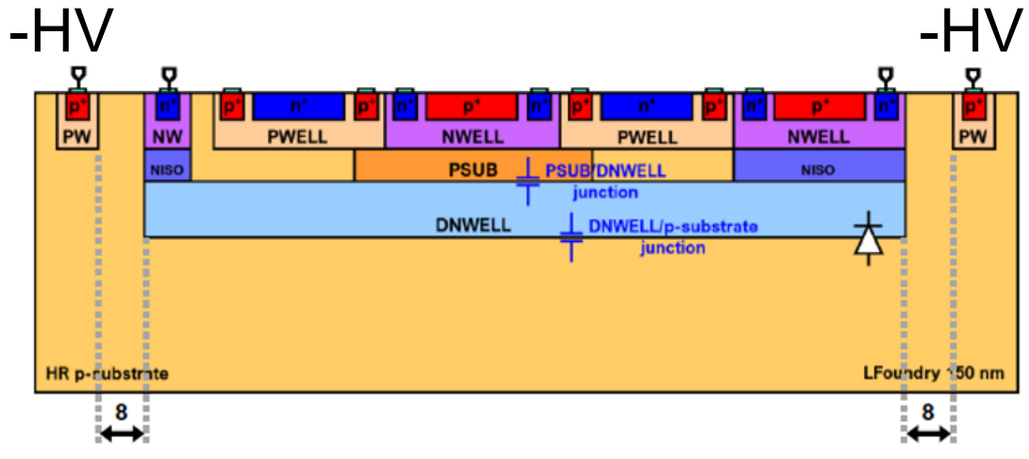




- Time stamps of the rising and trailing edges are recorded for Time of Arrival (ToA) and Time over Threshold (ToT).
- More details in **Chenfan's talk in 40th RD50 workshop**.

# Pixel

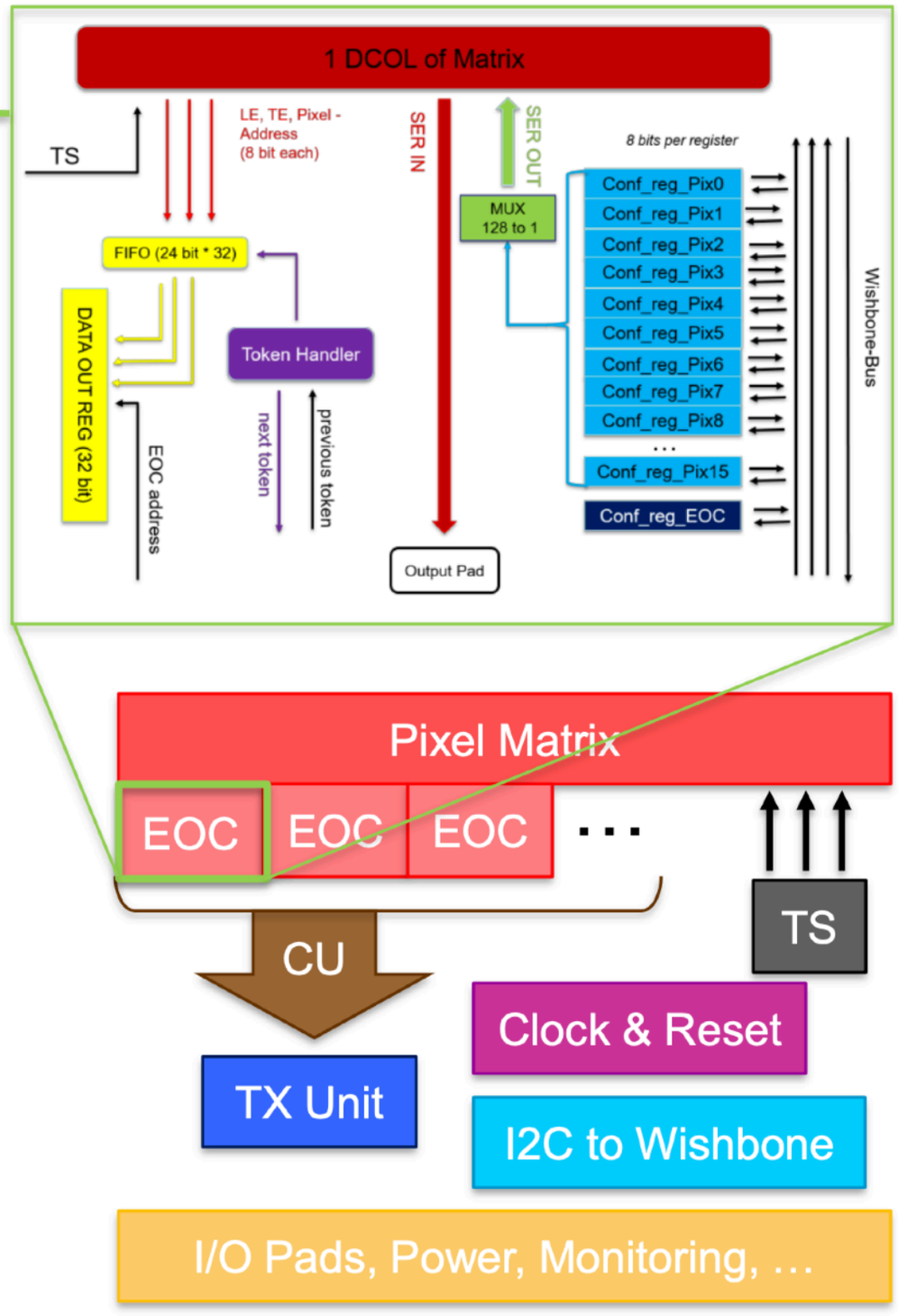
- Both analog and digital electronics are included inside each pixel.
- Analog and digital circuits are placed into separate deep p-wells and have different power lines to minimise crosstalk noise.
- Substrate is biased to high voltage from the front side.



# Readout Periphery

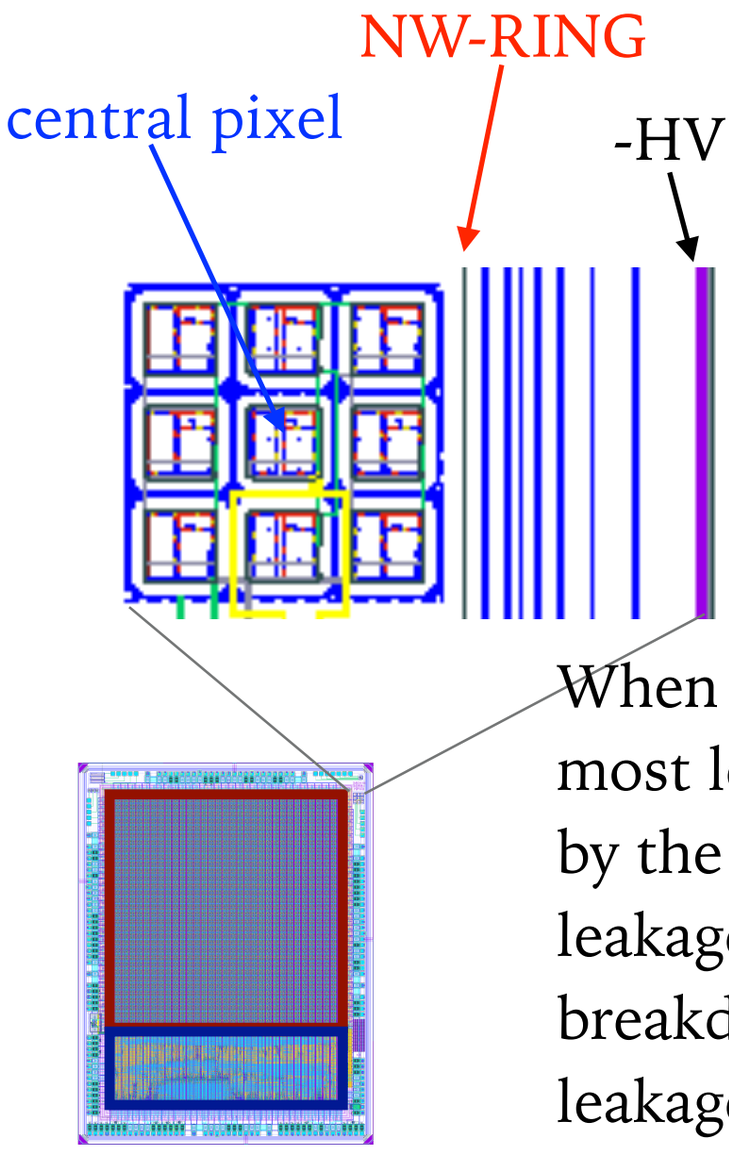
- One End-Of-Column (EOC) per DCOL
  - Configuration of pixels
  - Pixel data readout + 32 words deep buffer
- Transmission Unit (TX Unit) for data transmission
  - 128 words deep buffer (FIFO)
  - Framing
  - Encoding (Aurora 8bit-10bit)
  - Serialization (Serial stream at 640MHz)
- Control Unit (CU) for reading out EOC buffers
  - Controls data propagation from EOCs to TX Unit
- Global Timestamp (TS) Generator
  - 8bit, running at 40MHz
  - Gray-encoded to minimize activity on bus
- Clock and Reset Generator
  - Dividing a fast (640MHz) clock into a 40MHz clock
  - Clock multiplexer for optional external 40MHz
  - Synchronizing the 2 external reset signals with both clock domains
- I2C to wishbone module
  - Converts external I2C signals to internal wishbone control signals



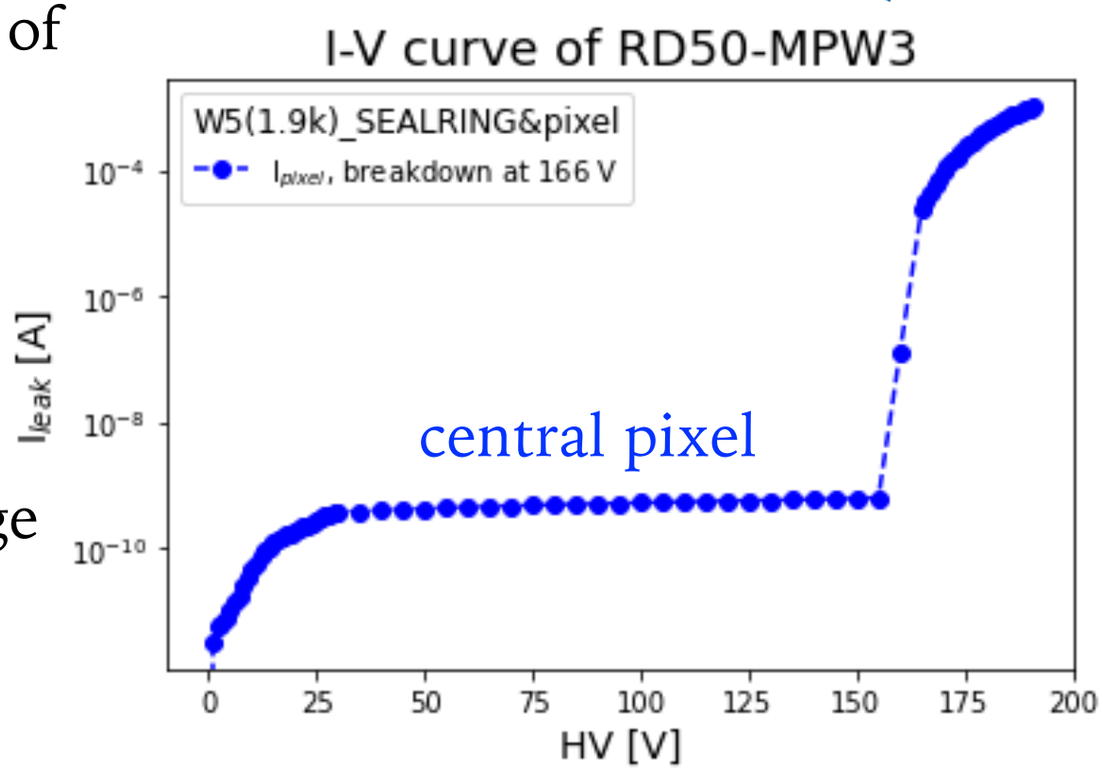

(by Patrick Sieberer, more details in **Patrick's talk in 40th RD50 workshop**)

# Initial IV

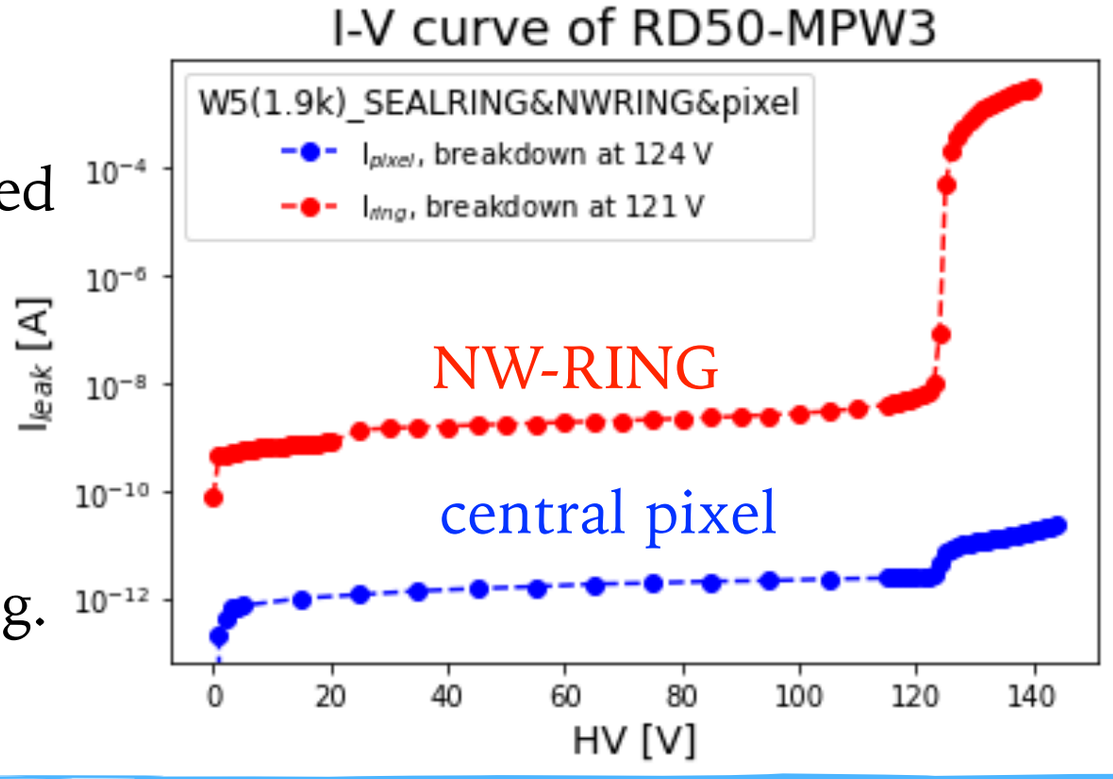
- Use test structure: measure leakage currents of the central pixel and ring.




When only central pixel is biased: leakage current ~ nA and breakdown ~ 160 V.

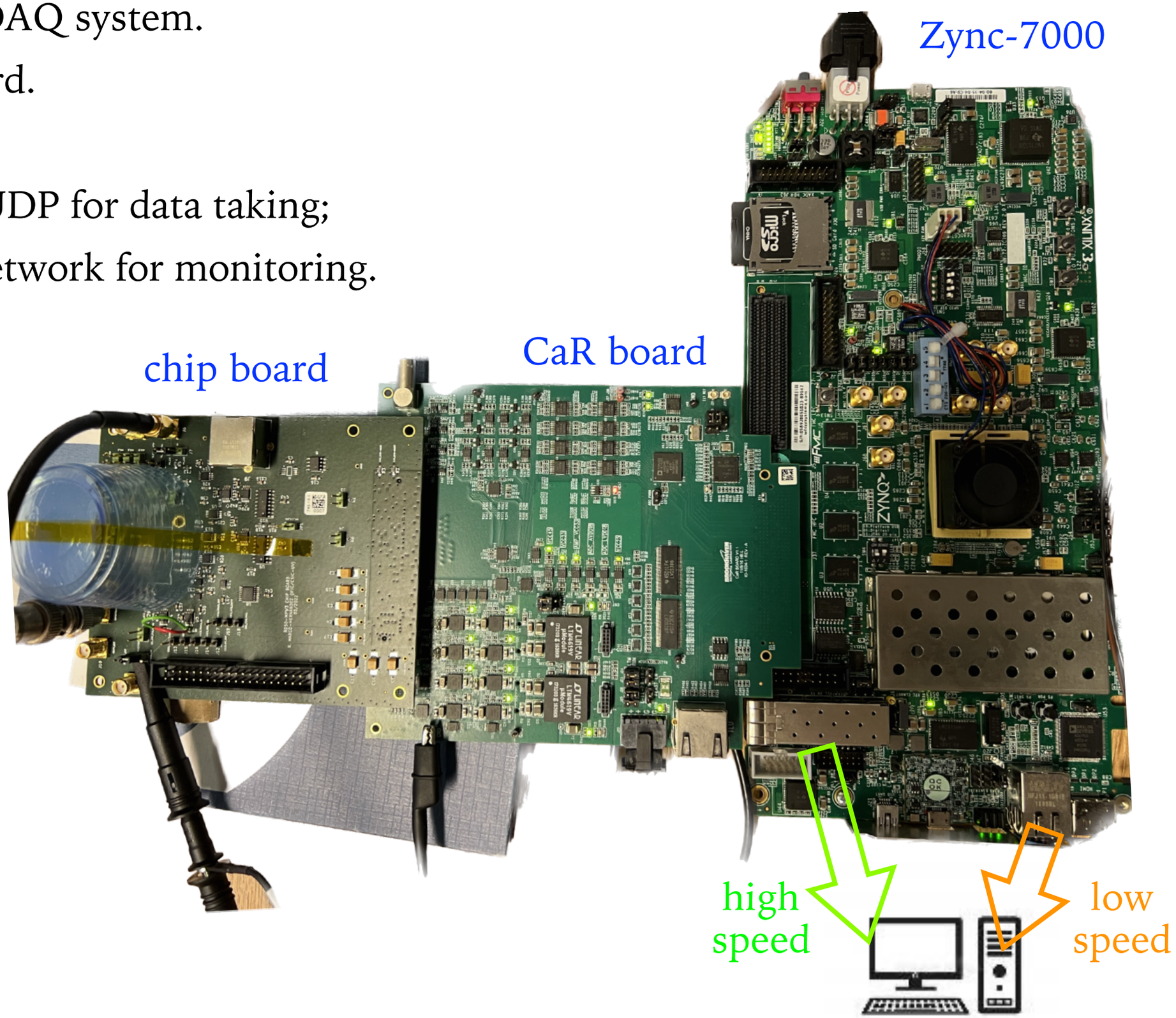



When NW-Ring is also biased: most leakage current is collected by the NW-Ring. NW-Ring leakage current ~ nA and breakdown ~ 120 V. pixel leakage current ~ pA and has higher breakdown than the ring.



# DAQ System

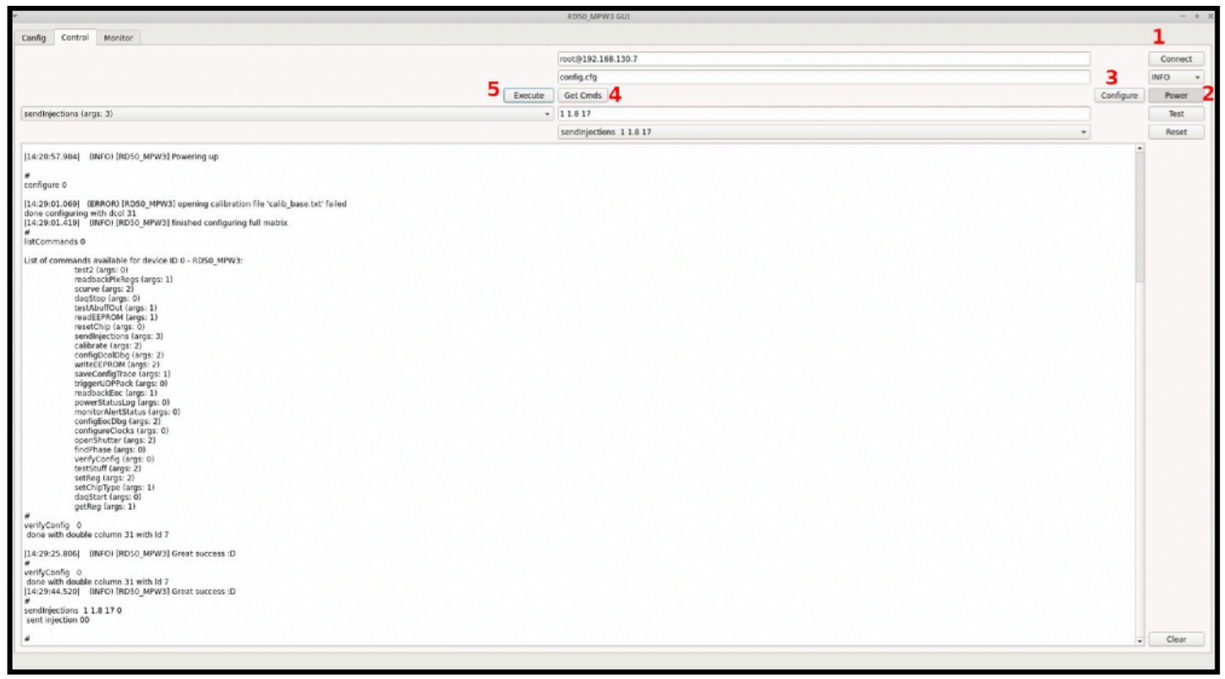
- Based on Caribou DAQ system.
- Dedicated chip board.
- 2 data paths:
  - ➤ high speed via UDP for data taking;
  - ➤ low speed via network for monitoring.



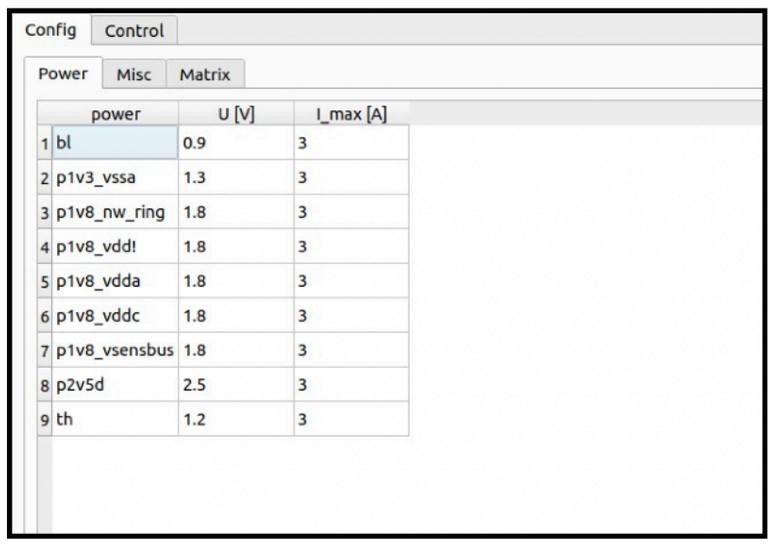
# GUI

- Based on a customised firmware.
- Software is based on Peary from Caribou.
  - ➤ DAQ configuration.
  - ➤ Chip configuration.
  - ➤ Execute commands to run the chip.

Control Tab




Power Tab



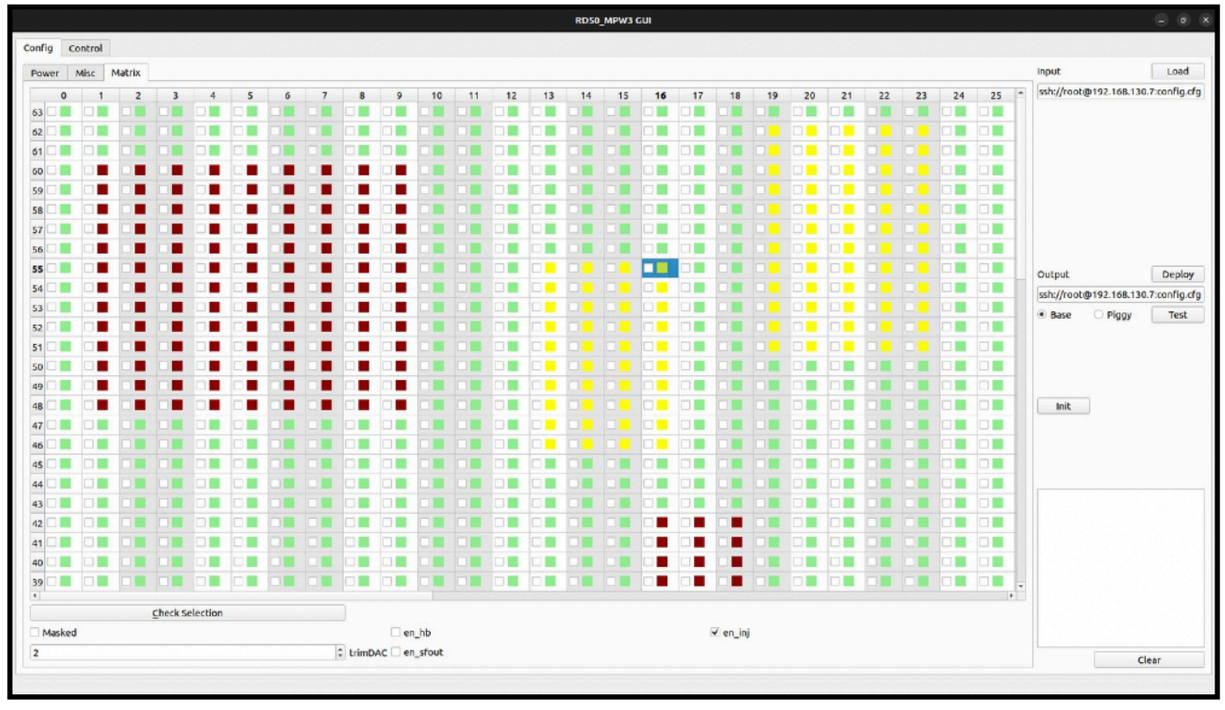
Config | Control

Power | Misc | Matrix

| | power | U [V] | I_max [A] |
|---|---|---|---|
| 1 | bl | 0.9 | 3 |
| 2 | p1v3_vssa | 1.3 | 3 |
| 3 | p1v8_nw_ring | 1.8 | 3 |
| 4 | p1v8_vdd! | 1.8 | 3 |
| 5 | p1v8_vdda | 1.8 | 3 |
| 6 | p1v8_vddc | 1.8 | 3 |
| 7 | p1v8_vsensbus | 1.8 | 3 |
| 8 | p2v5d | 2.5 | 3 |
| 9 | th | 1.2 | 3 |

- ➤ Set bias and supply voltages.

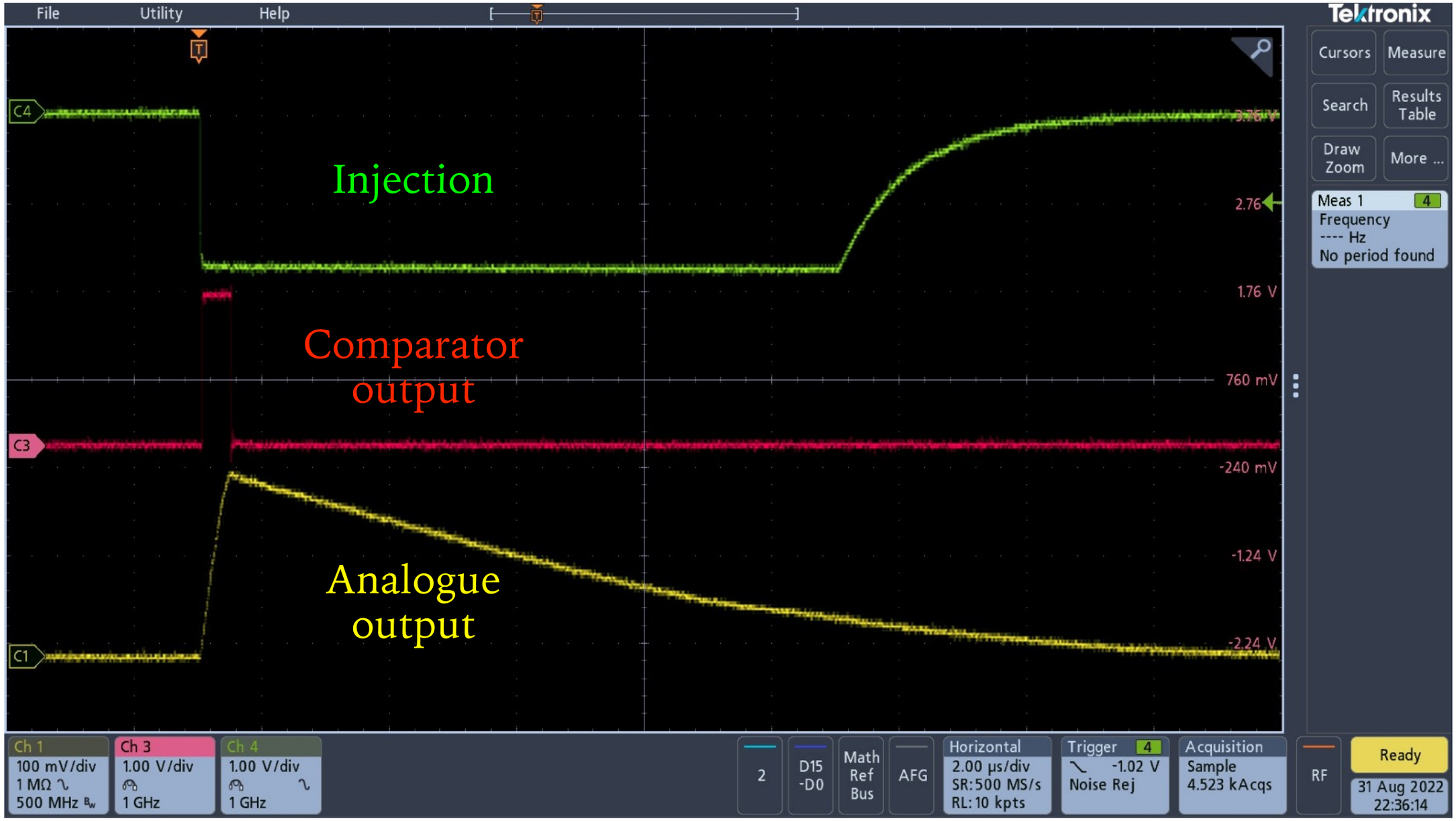
Matrix Config. Tab




- ➤ Select pixels for configuration.

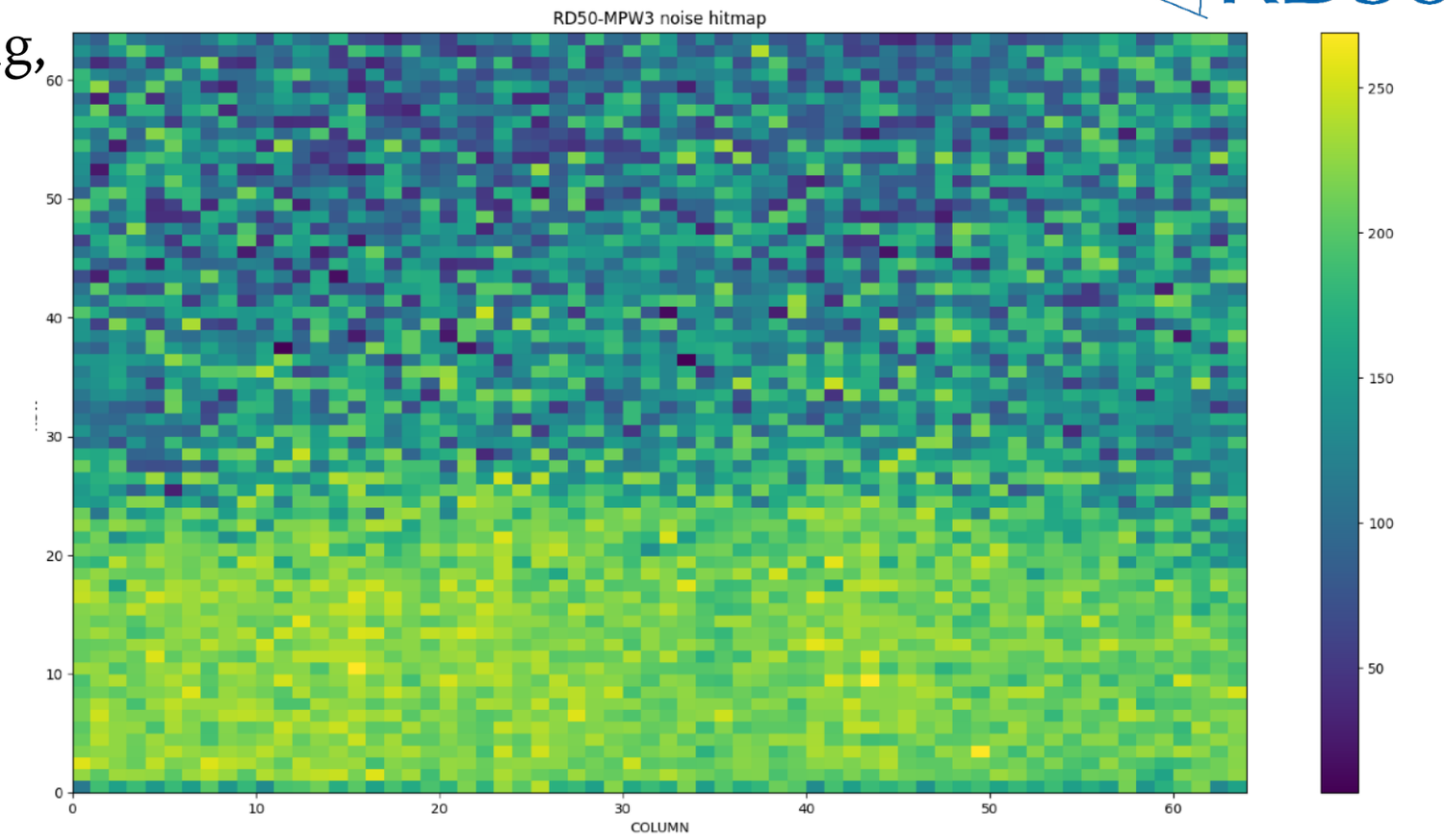
# First Response

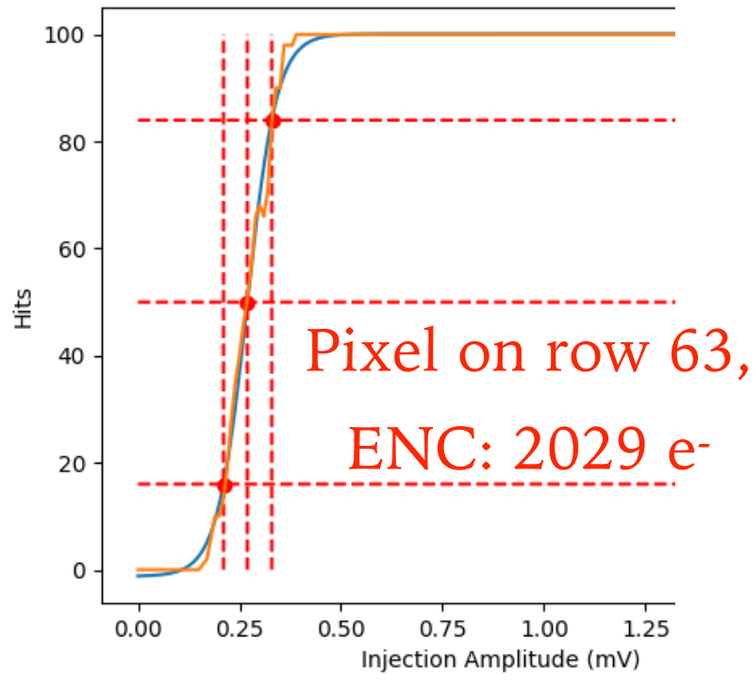
- Send injection signal into pixel.
- Chip, DAQ and GUI are functioning.



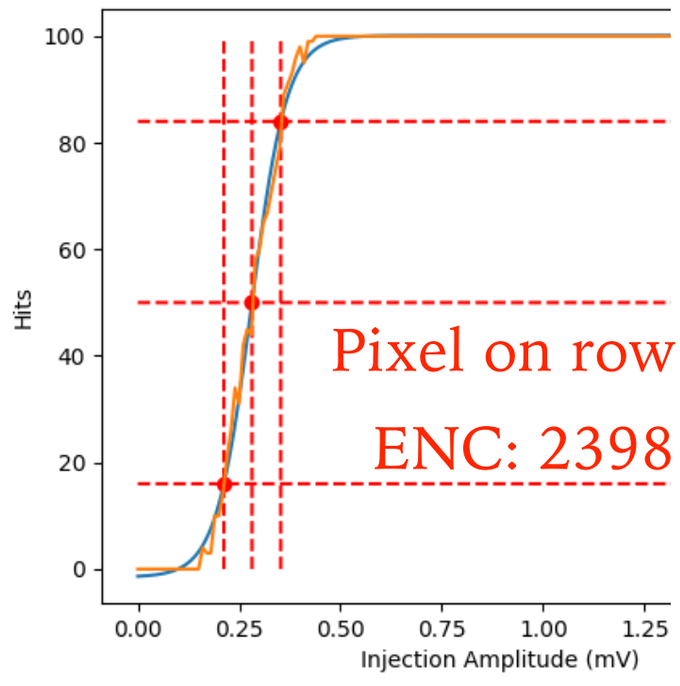
# High Noise

- When set the chip open-running, hits are recorded due to noise.
- Threshold = 300 mV above baseline voltage.
- Shutter window = 2 s.
- Bottom part of the matrix is more noisy. -> (noise might be from the digital periphery)
- S-curve shows pixel on the top (row 63) has noise of ENC = 2029 $e^-$, pixel in the middle (row 33) has ENC = 2398 $e^-$.
- Investigating the high noise…




Pixel on row 63,
ENC: 2029 $e^-$




Pixel on row 33,
ENC: 2398 $e^-$

# Current Status and Future Plan

- Need to slow down the clock to allow pull-down to work properly.
- Need to understand the high noise issue.
- More sophisticated lab measurements are on-going…
- Beam test has been taken at CERN SPS in October 2022, details will be presented in the following talk by Patrick.
- In the future potential submission:
  - ➤ Fix the issues found in RD50-MPW3;
  - ➤ Try thinning and backside processing.