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*Chinese Academy of Sciences*



**University of  
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# Irradiation studies of p-Si using Schottky diode and PN junction

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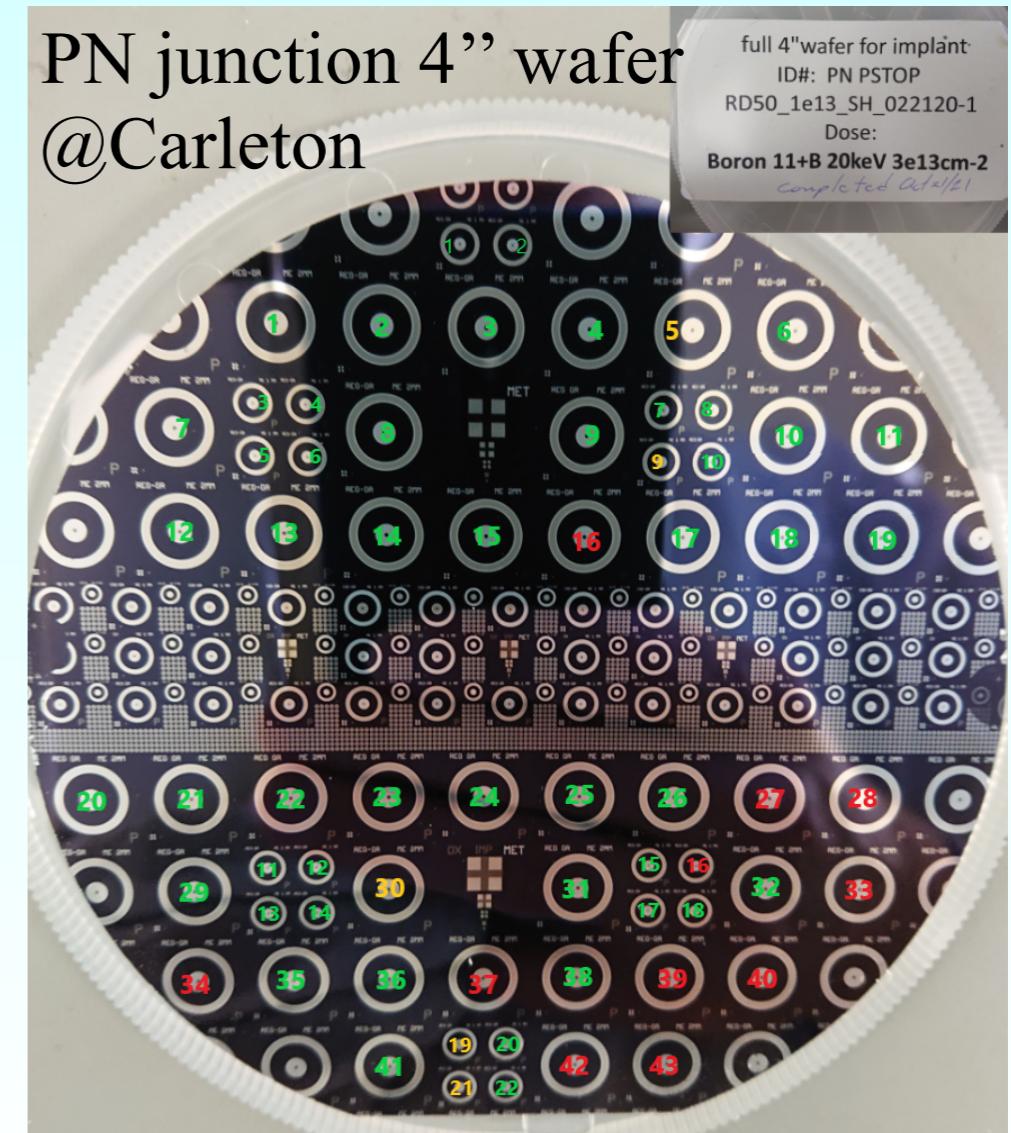
# Introduction

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- p-type silicon is and going to be used on hybrid and MAPS silicon detectors, ATLAS, CMS, ALICE, etc,
- Understanding of radiation damage is crucial for proper operation and evaluation of detectors in harsh radiation environment,
- Schottky diodes and PN junctions have been designed and fabricated on p-type epitaxial silicon wafers,
- Aim to gain reliable TCAD models for the radiation damage of p-type silicon,
- Updates on Charge Collection Efficiency(CCE) and Defect characteristics will be presented.

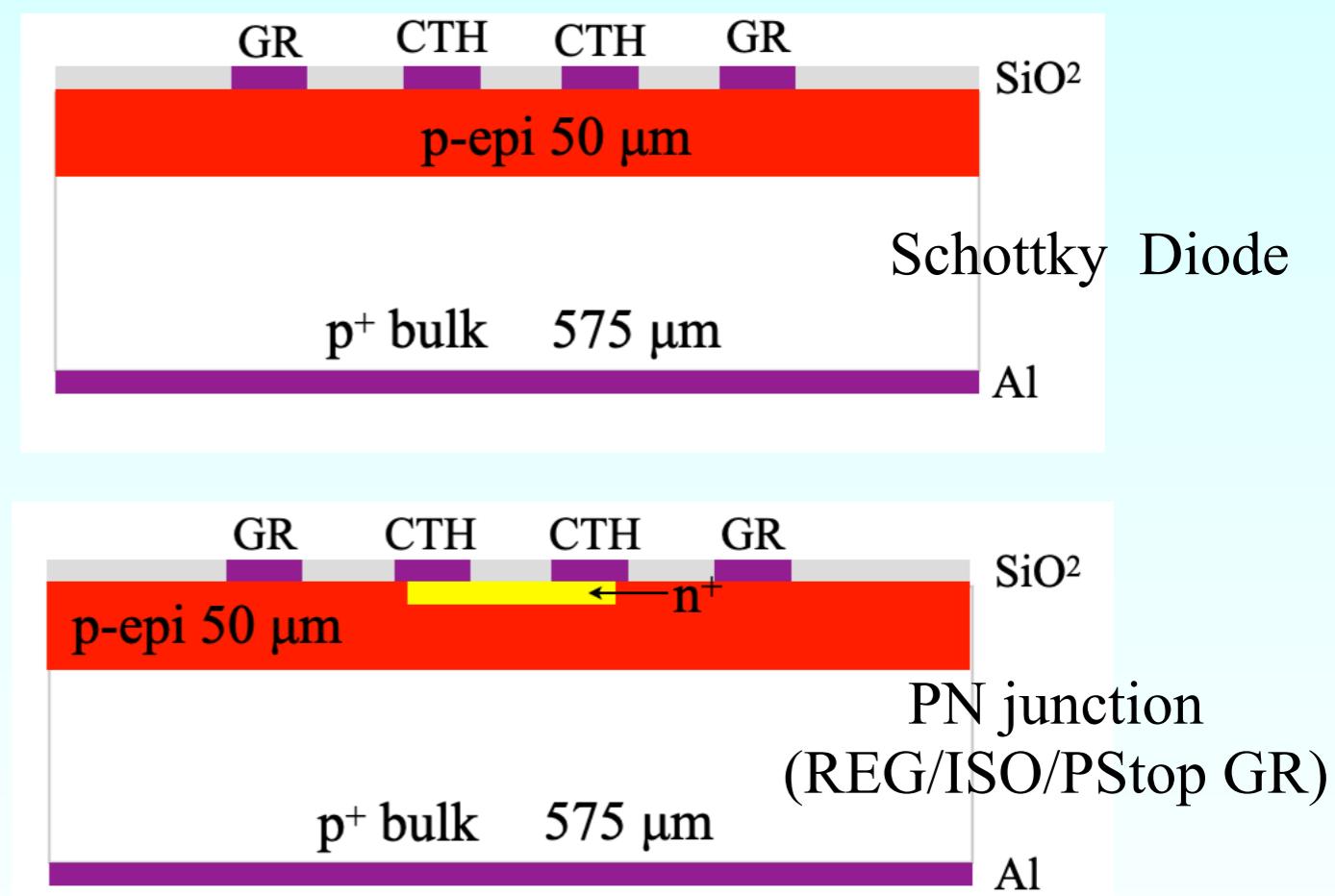
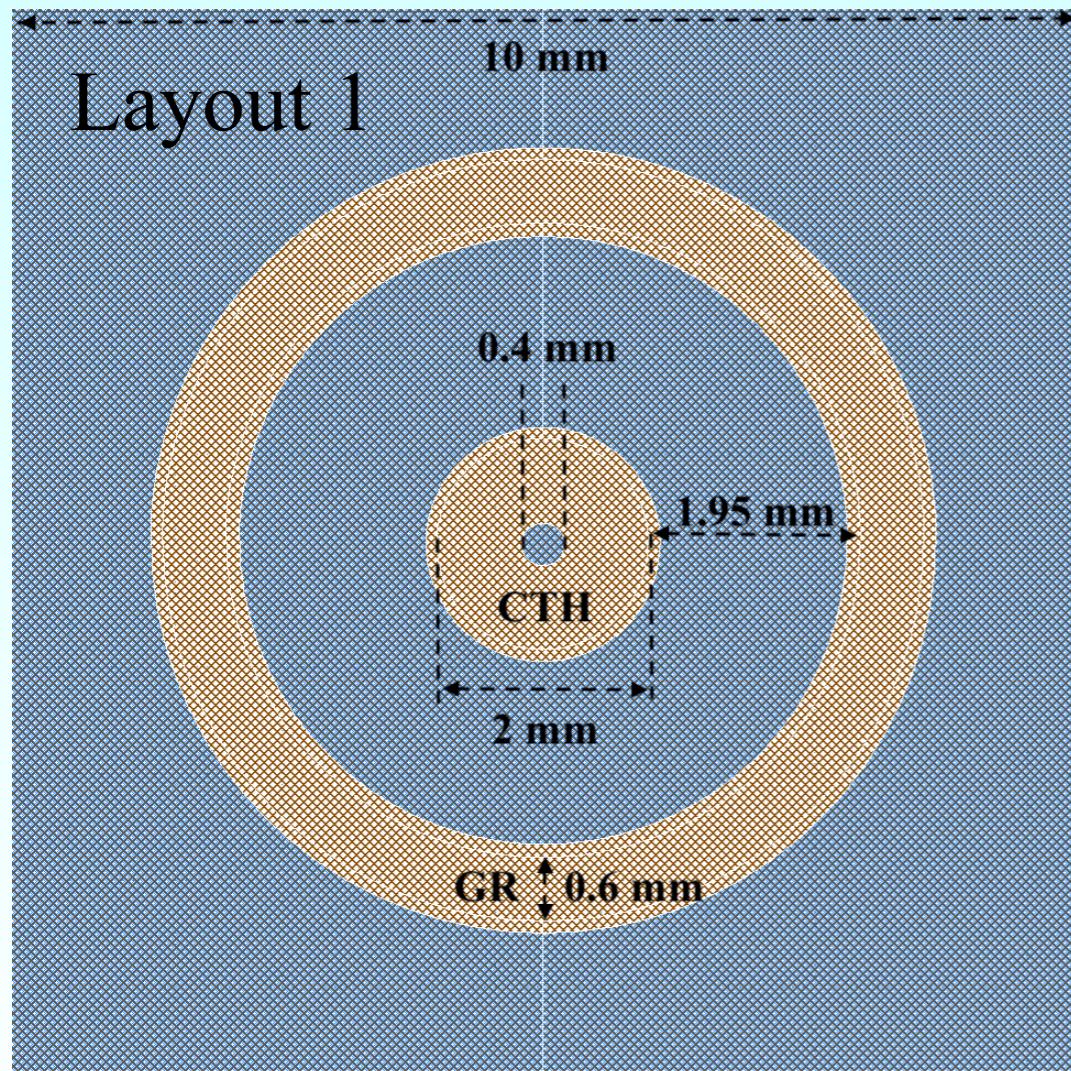
# Wafer and device layout

- Schottky diodes fabricated on 6-inch wafer, PN junctions on 4-inch wafer,
- 4 layouts for both Schottky diodes and PN junctions,
- More details in [Giulio's report](#) at 36th RD50 Workshop.

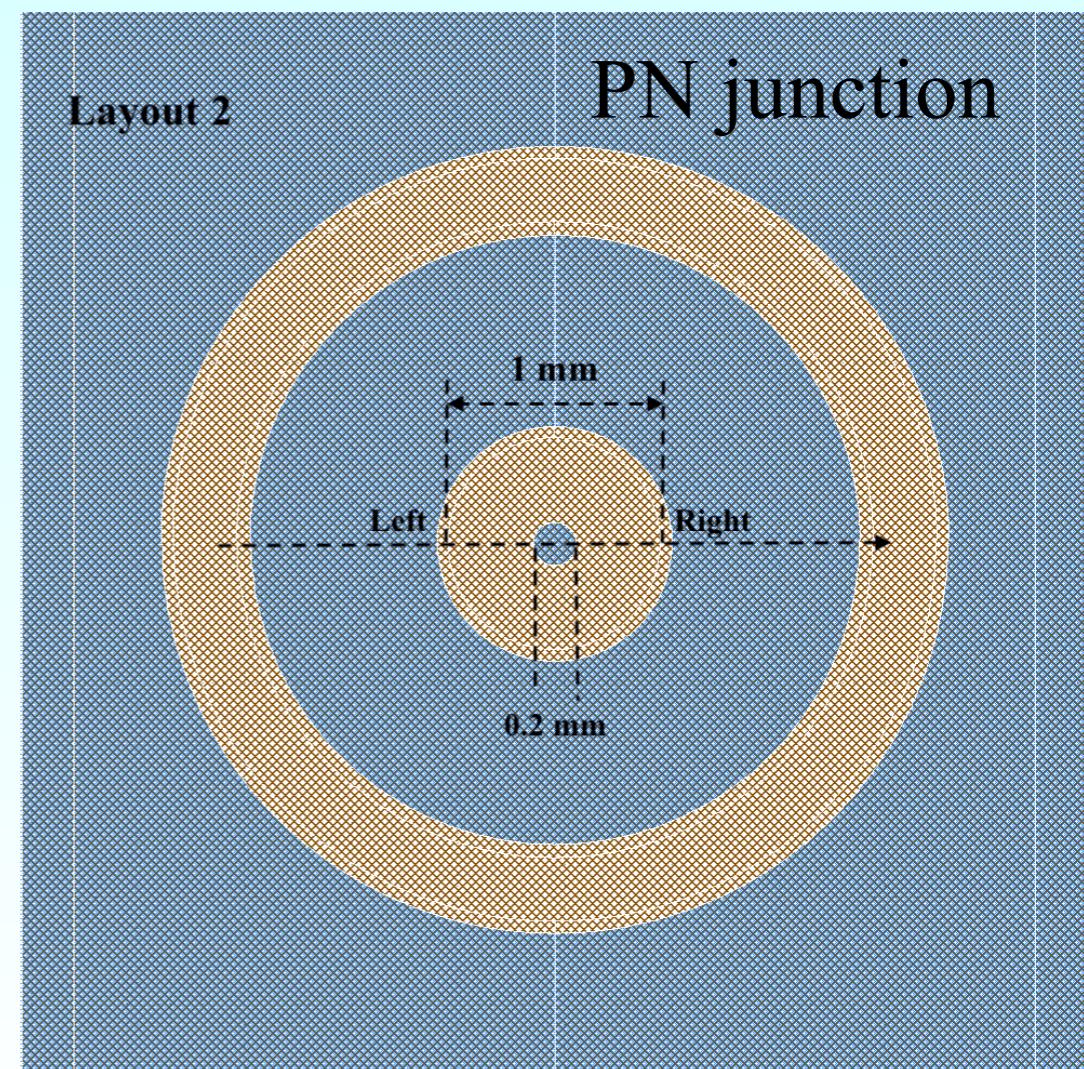
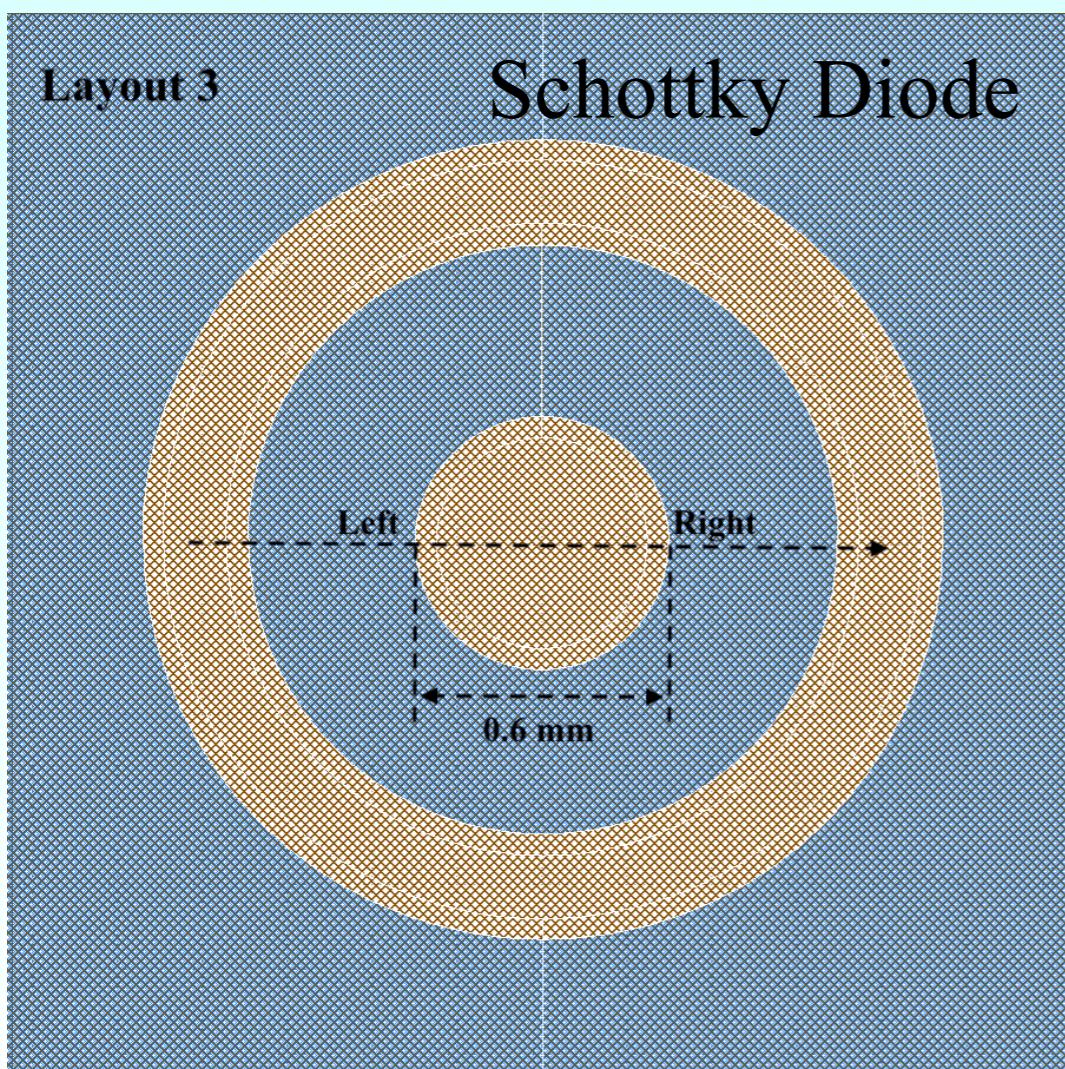


# Wafer and device layout

	Layout 1	Layout 2	Layout 3	Layout 4
Cathode Ø [mm]	2	1	0.5	0.1
Guard Ring width [mm]	0.6	0.30	0.15	0.03
Central hole Ø [mm]	0.4	0.2	N.A.	N.A.

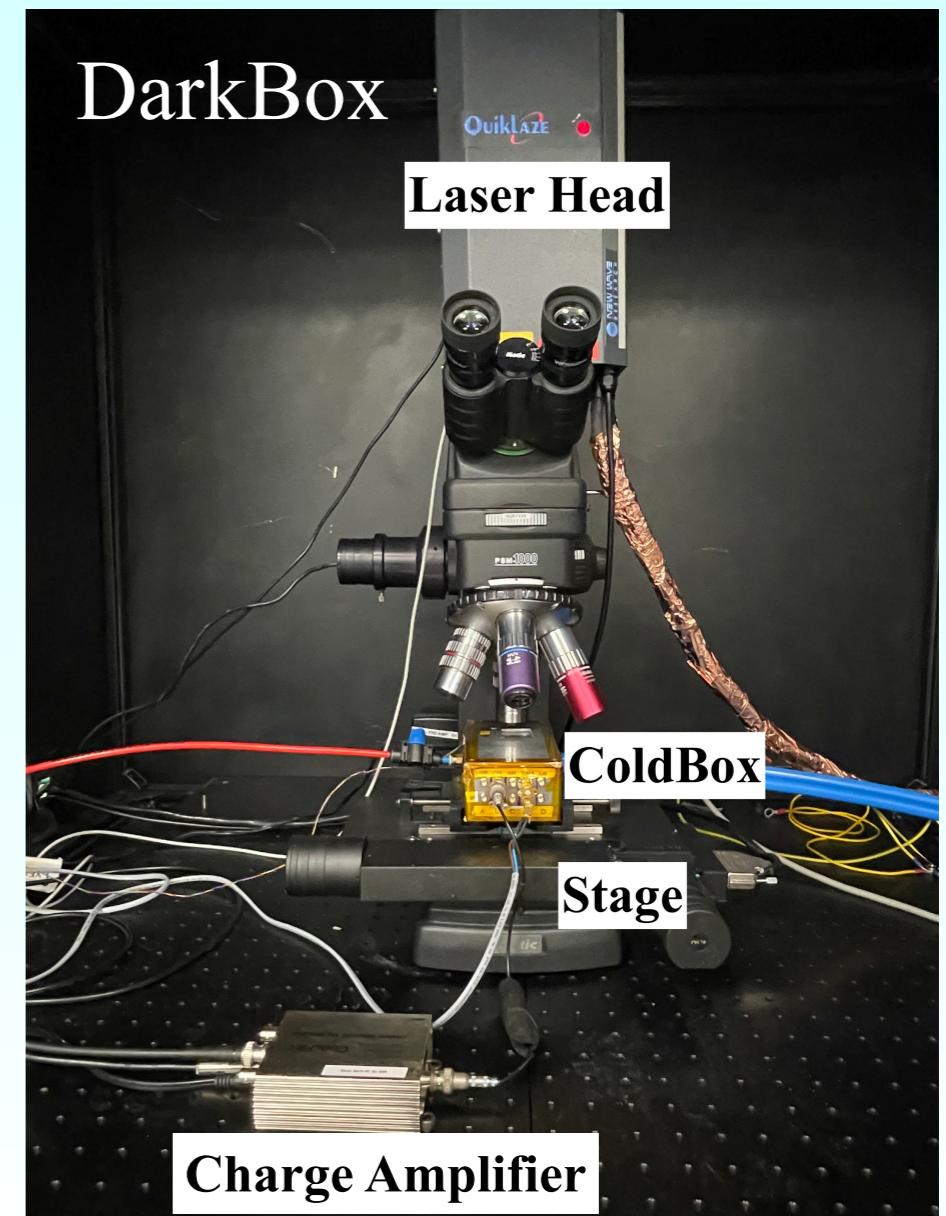
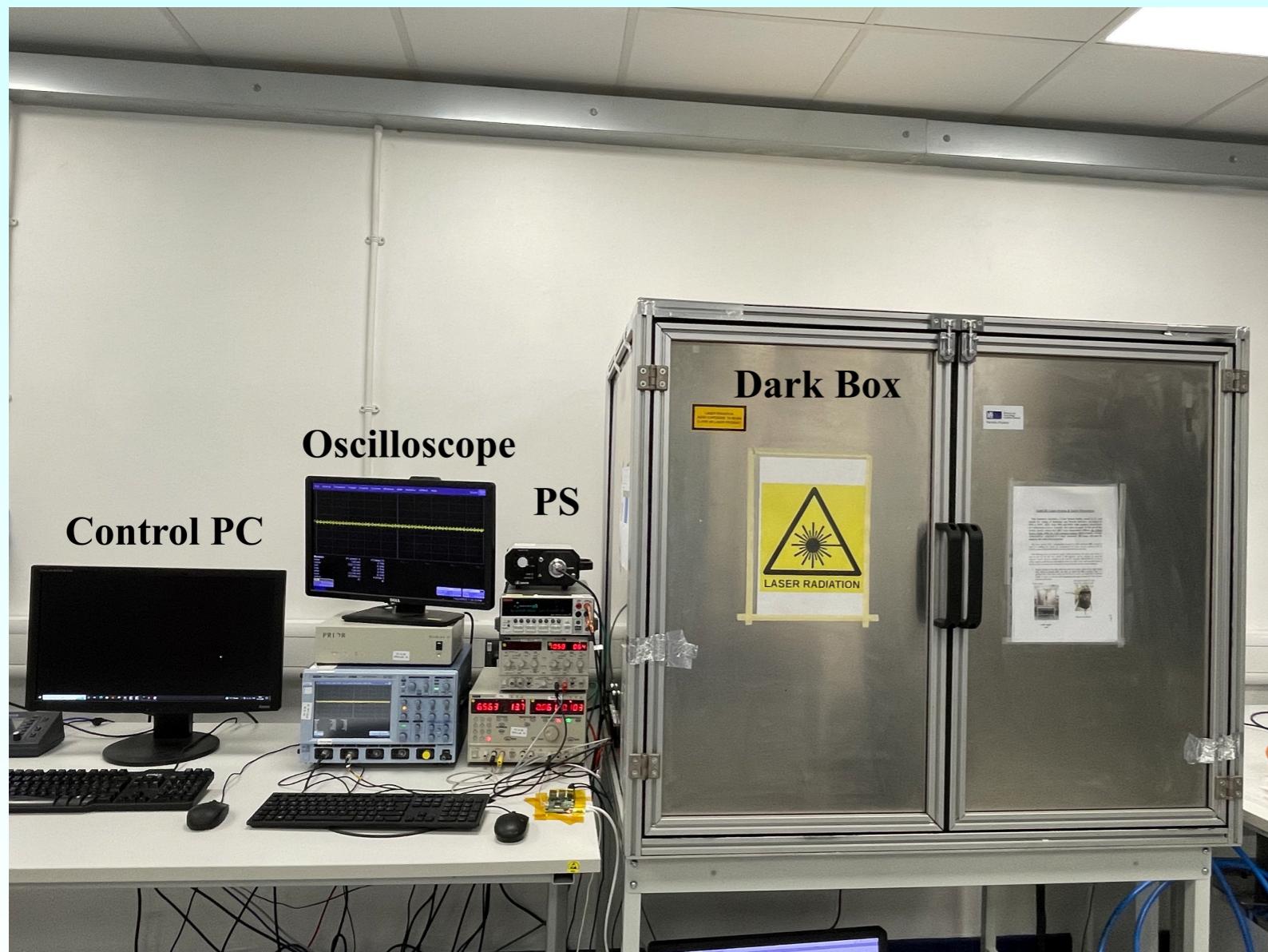


# Charge Collection Efficiency



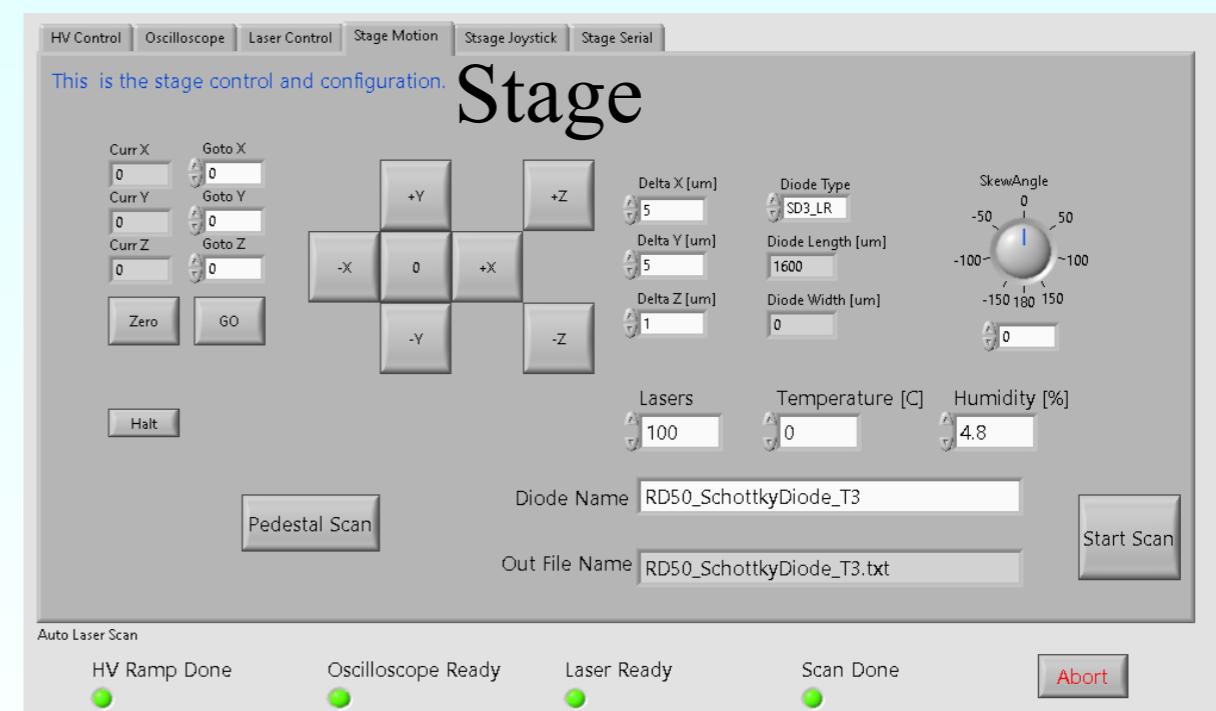
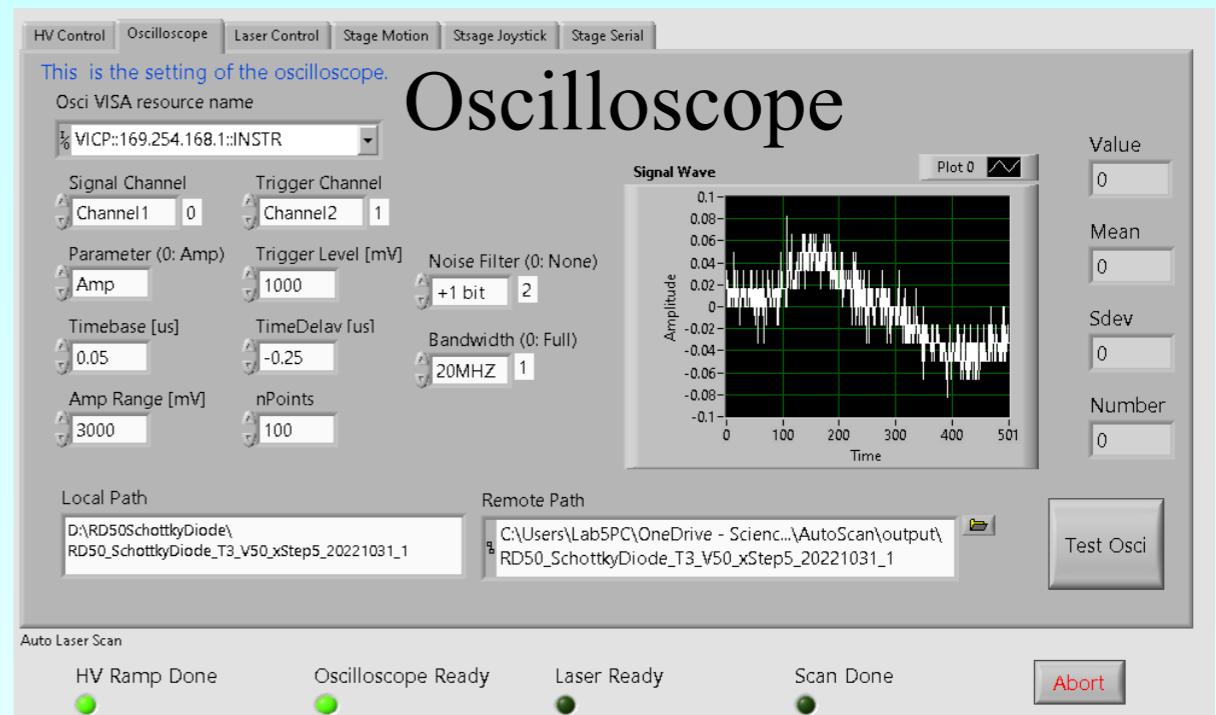
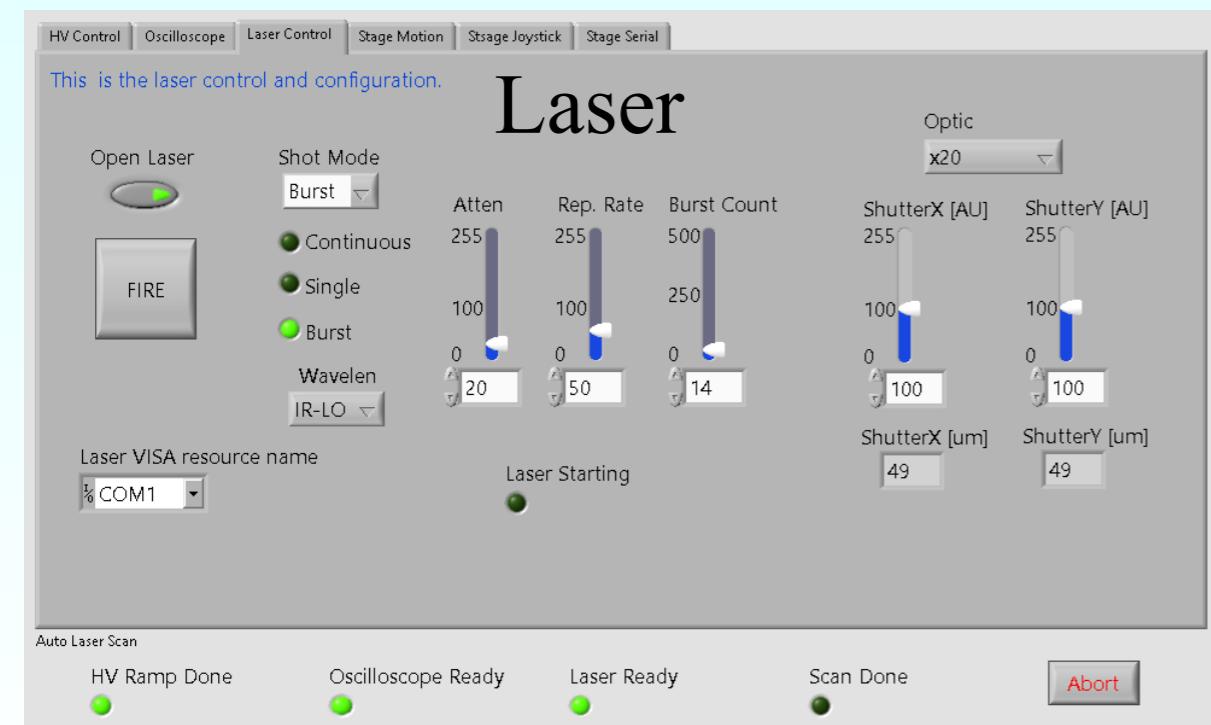
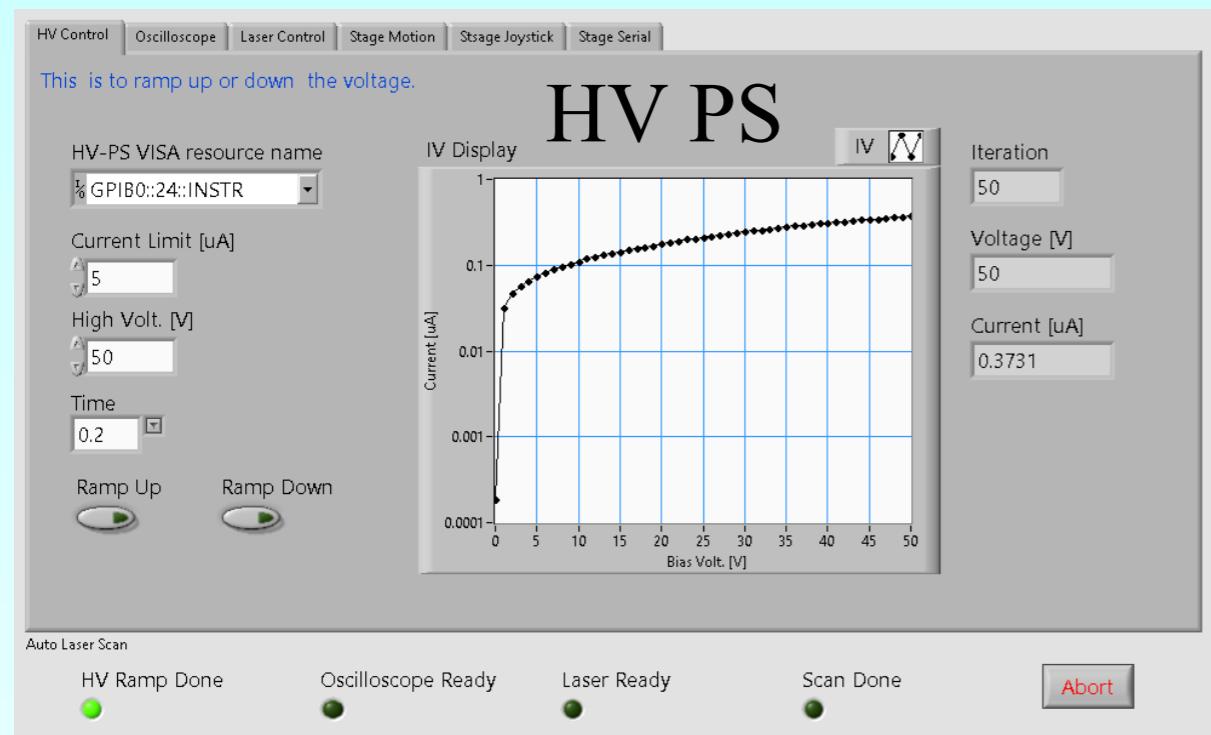
# Setup for Charge Collection Efficiency

- Laser: IR(1064 nm),  $5 \mu\text{m} \times 50 \mu\text{m}$ ,  $23.44 \pm 0.2 \text{ pJ}$
- Stage: move step of  $5 \mu\text{m}$
- Temperature:  $20 - -20^\circ\text{C}$
- More details in [Matt's report](#) at 40th RD50 Workshop.



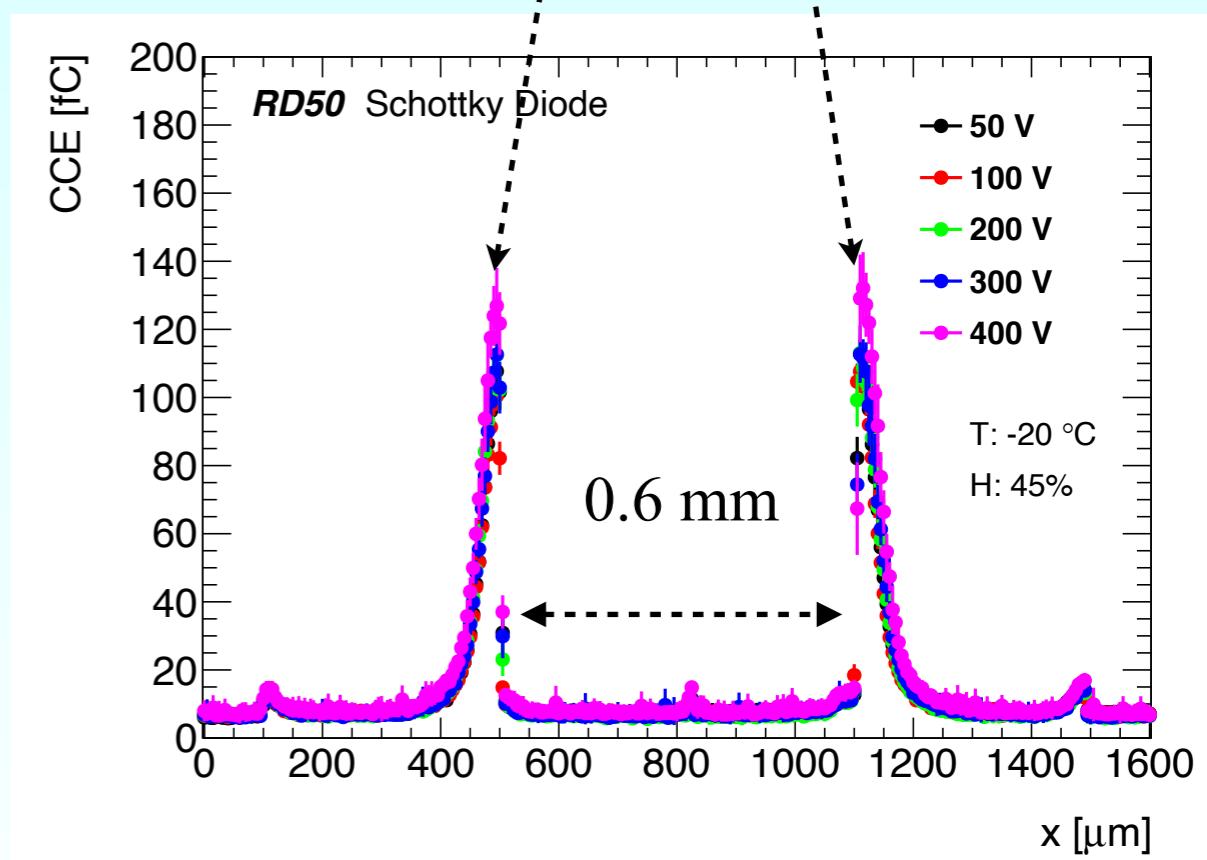
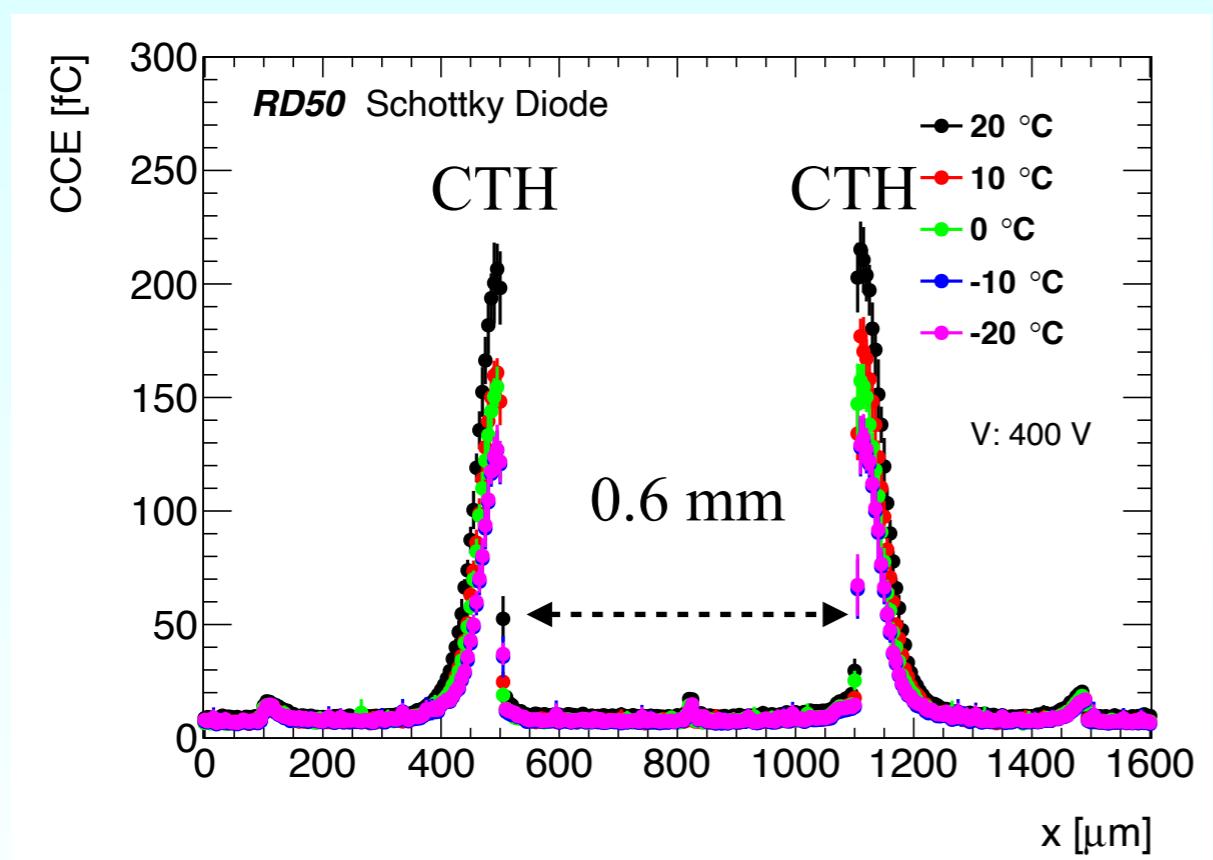
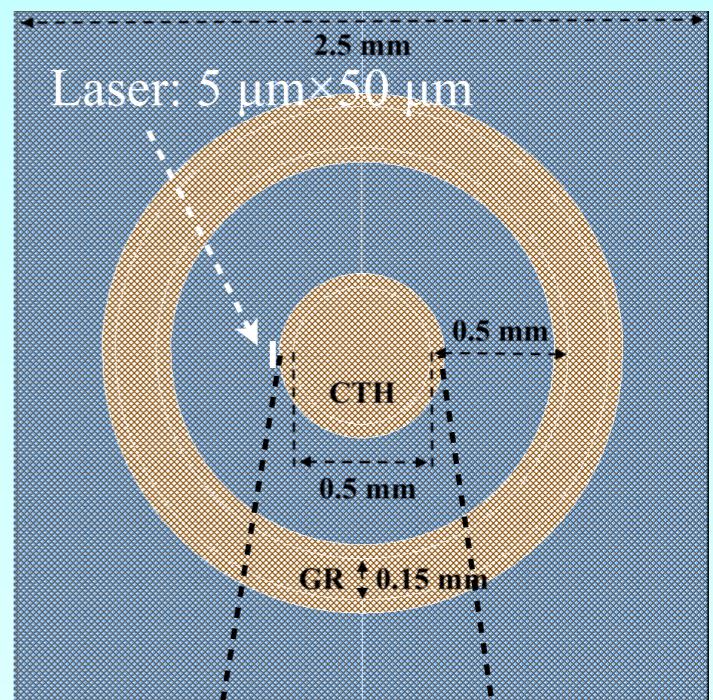
# Setup for Charge collection efficiency

- Automatic scanning program developed in LabVIEW.



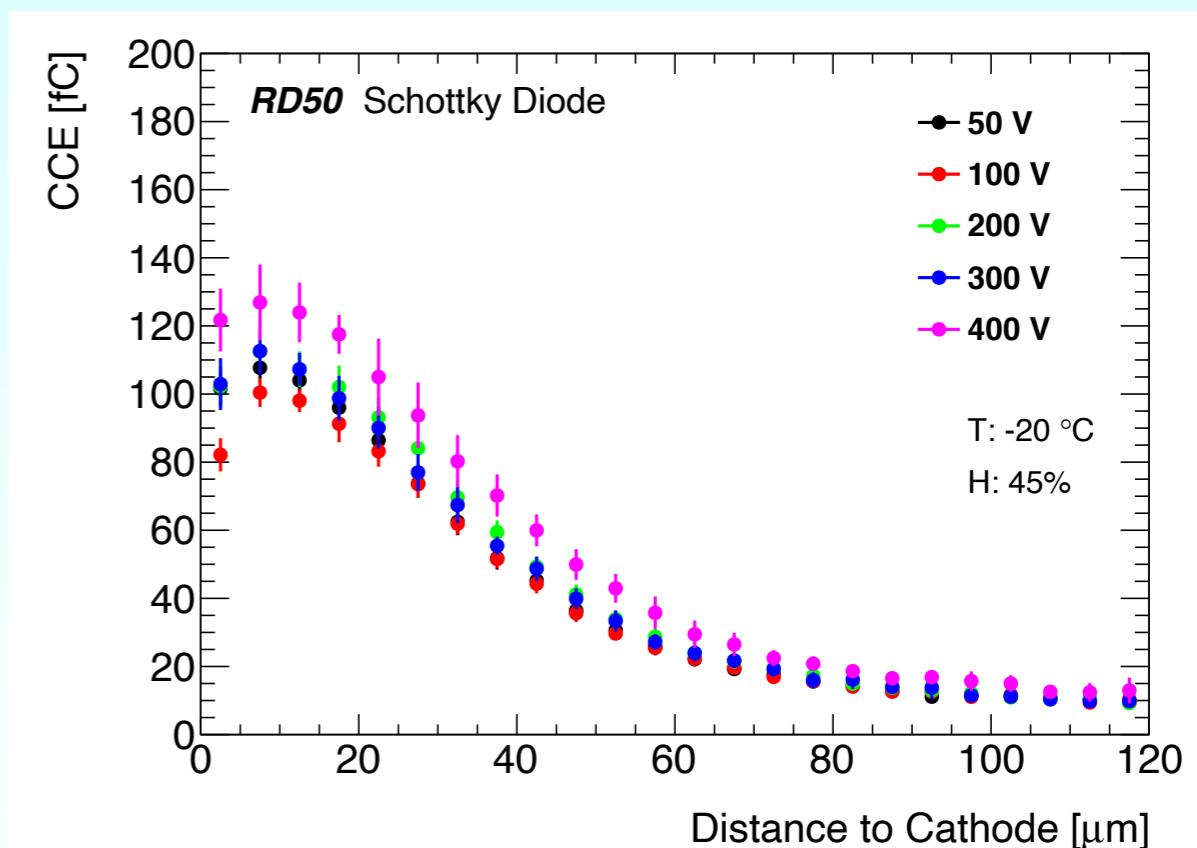
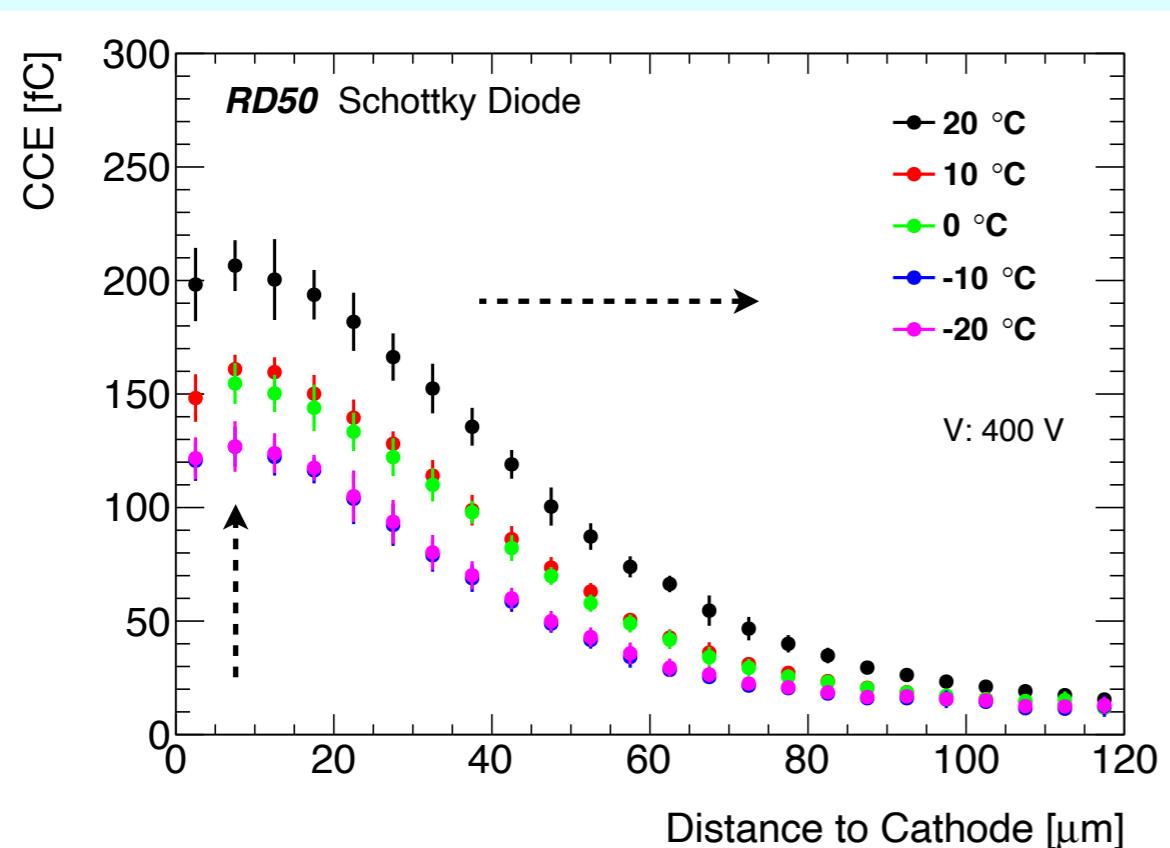
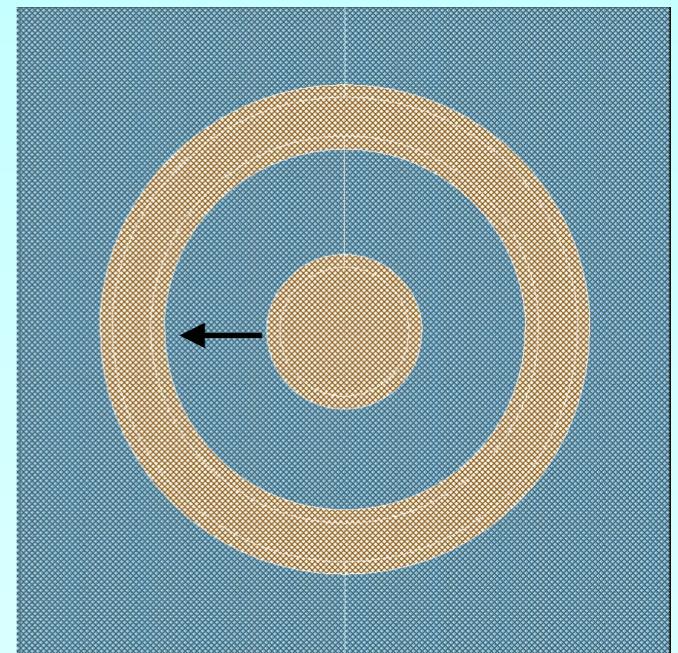
# CCE of un-irradiated Schottky diode

- T3 Schottky diode with no central laser hole
- Bias Voltages: 50, 100, 200, 300, 400 V
- Temperatures: 20, 10, 0, -10, -20 °C



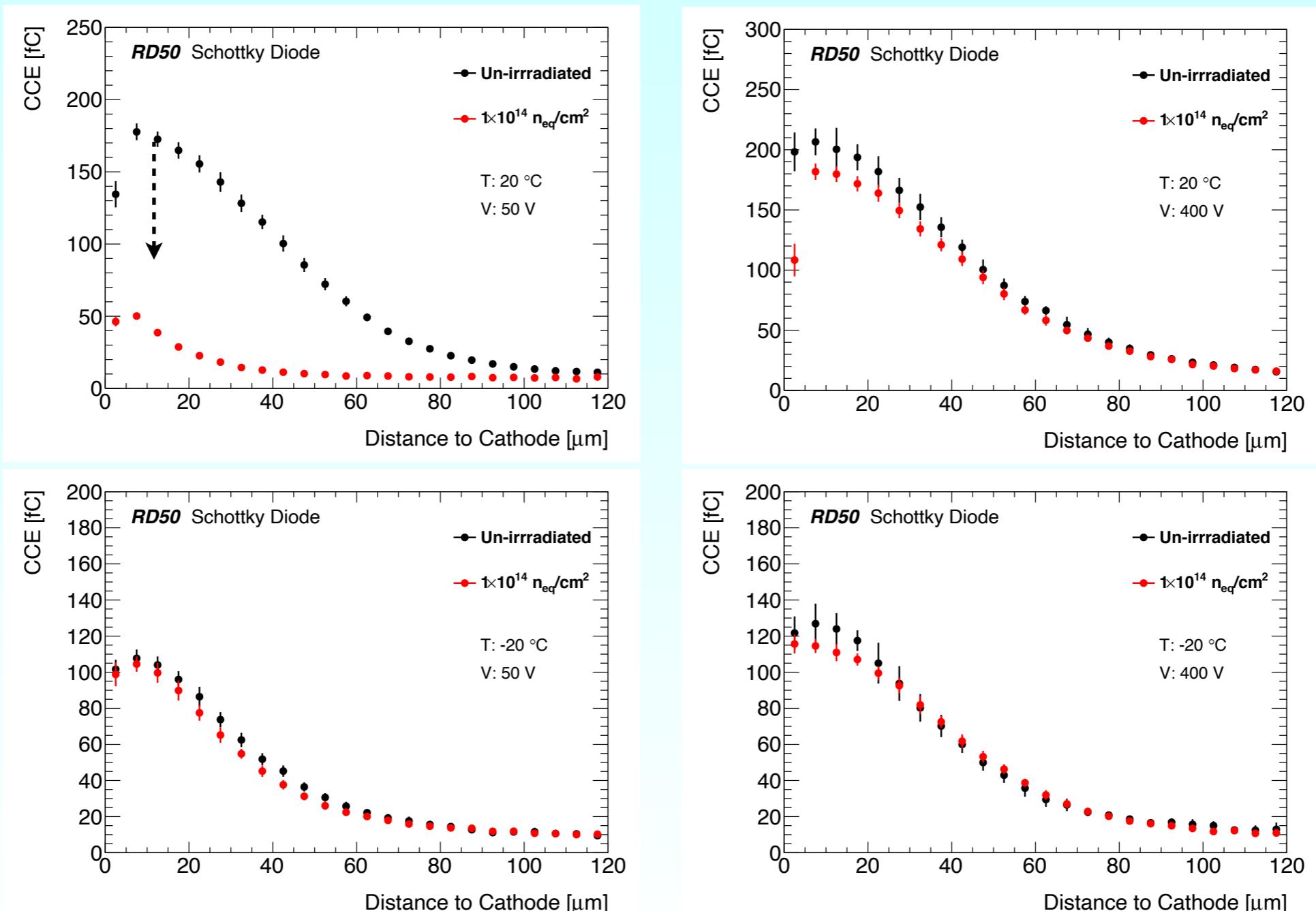
# CCE of un-irradiated Schottky diode

- Depleted thickness decreases with increased distance from the cathode edge,
- At fixed bias voltage, the higher the temperature, the larger the CCE, still under investigation,
- At low temperature, not significant improvement on CCE for various bias voltages.



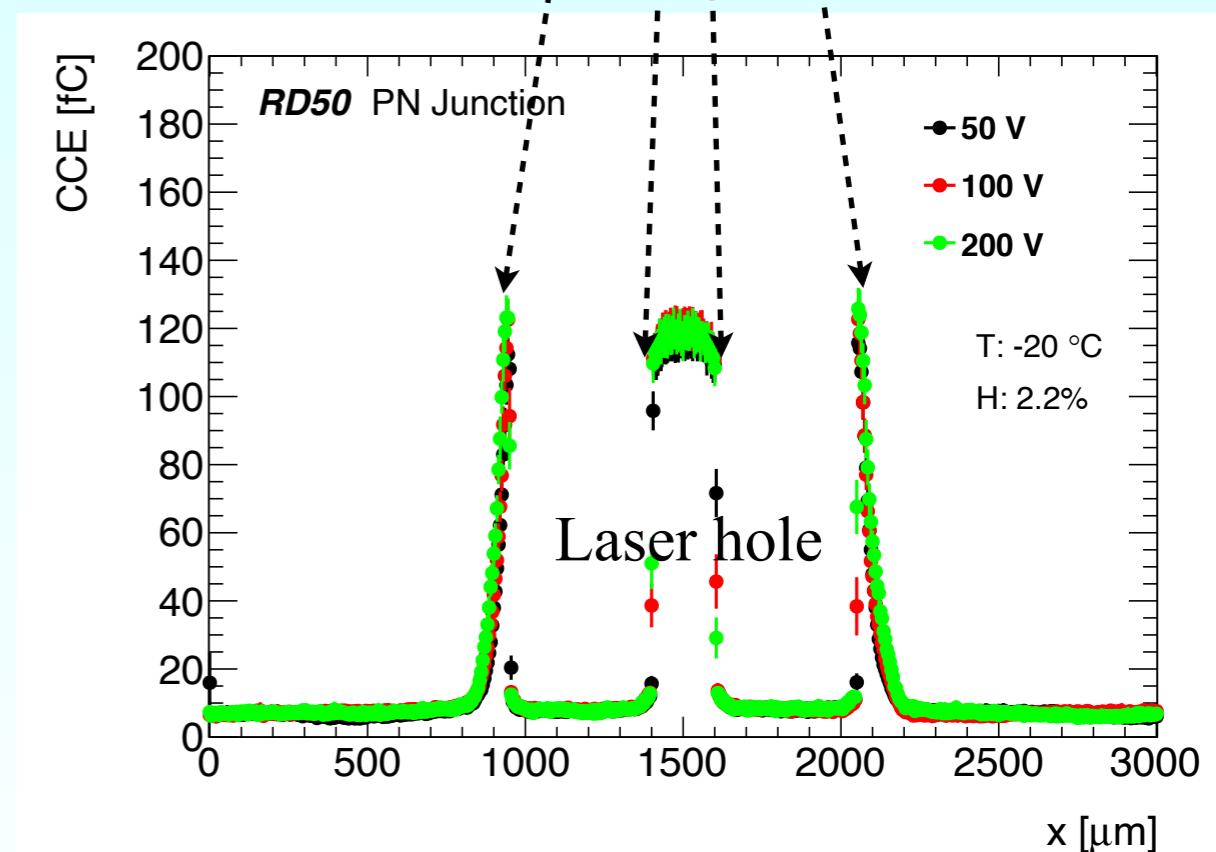
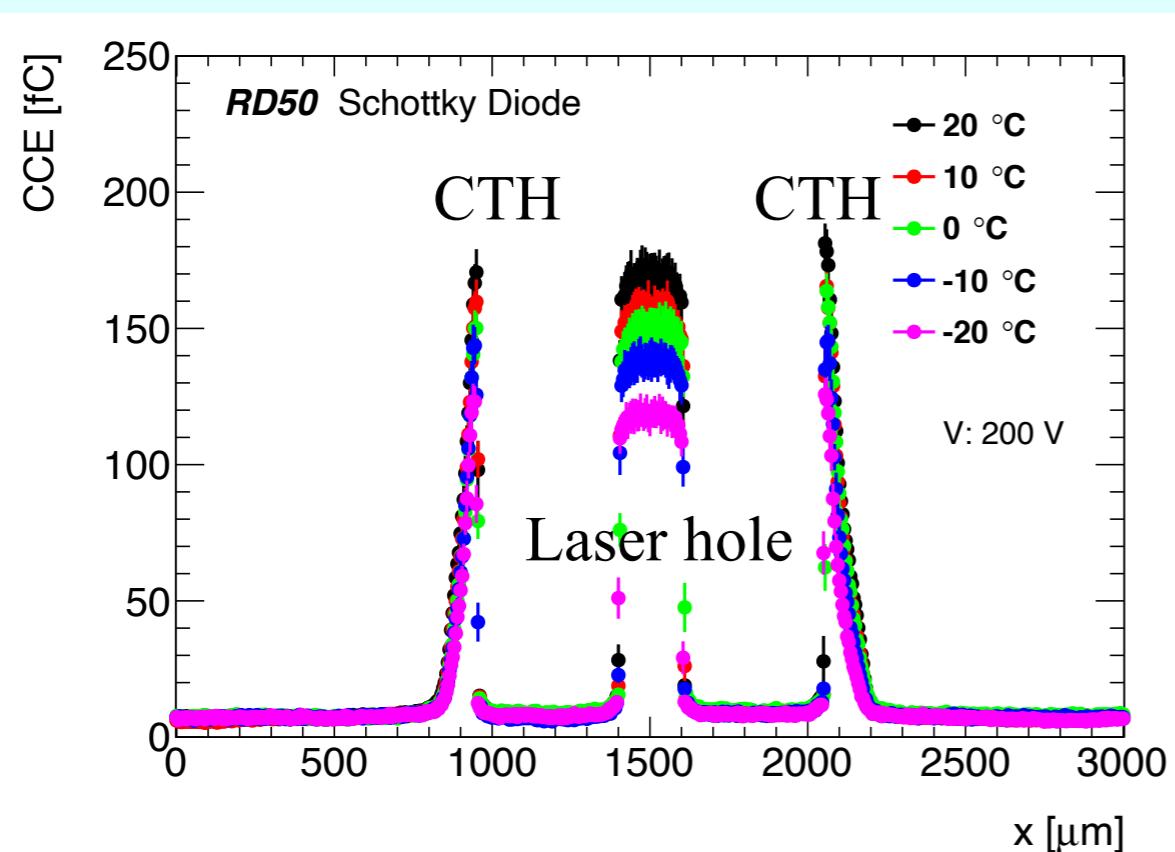
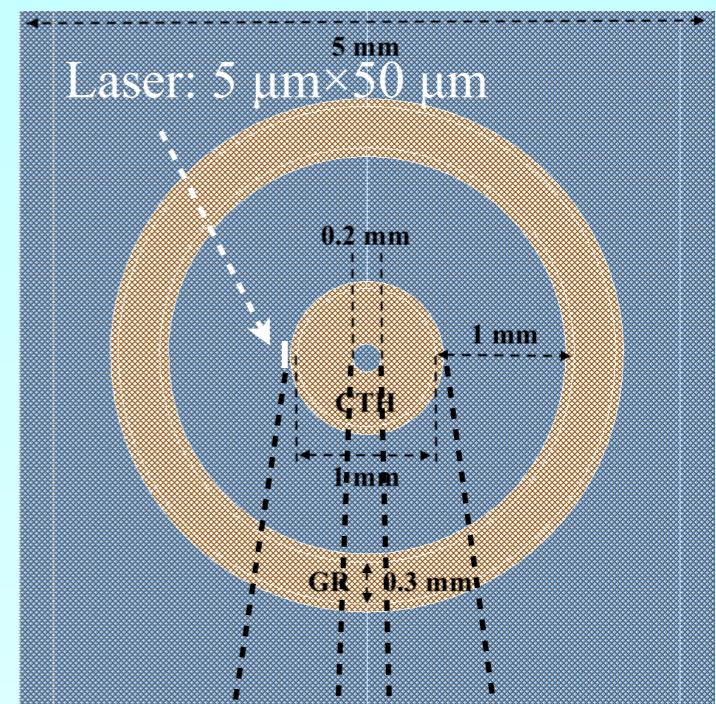
# CCE of Schottky diode

- CCEs of un-irradiated and irradiated( $1 \times 10^{14} n_{eq}/cm^2$ ) Schottky diodes(T3),
- Low temperature or hight voltage mitigated the charge trapping.



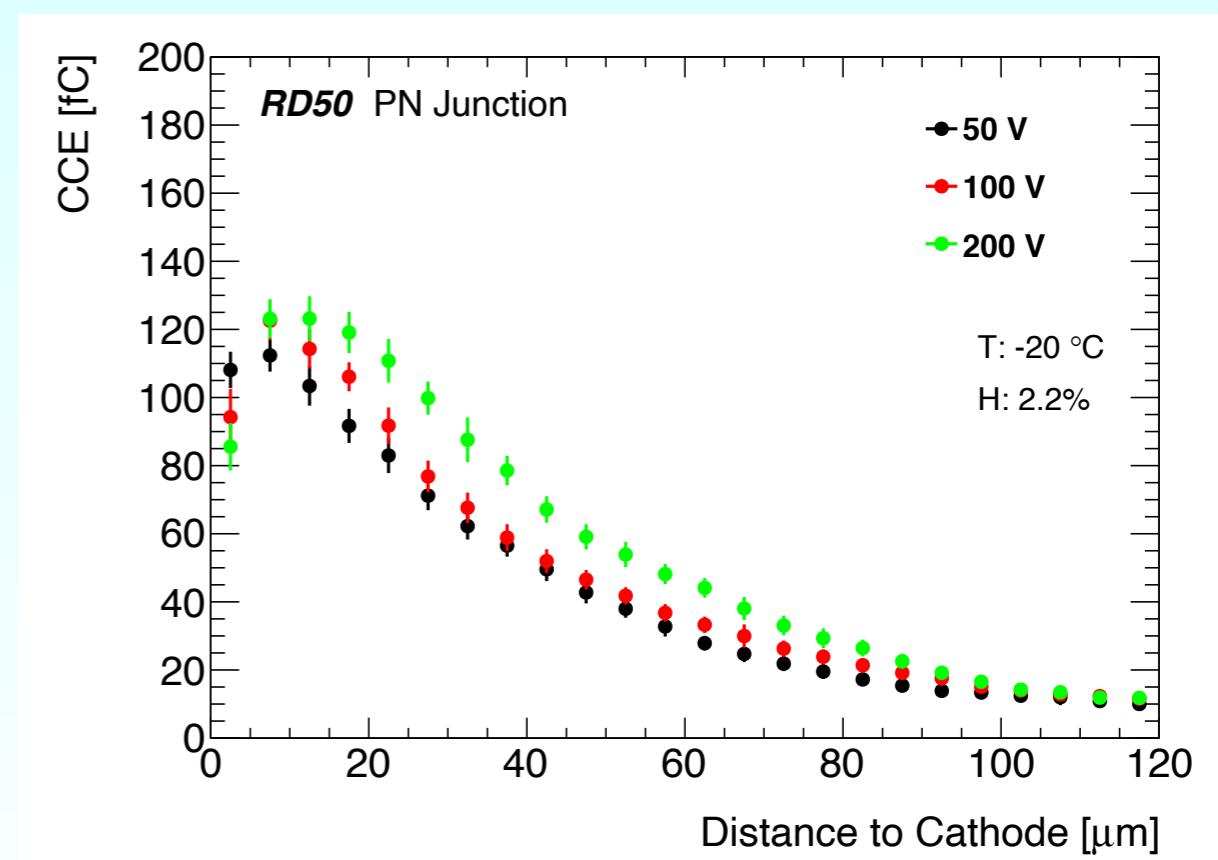
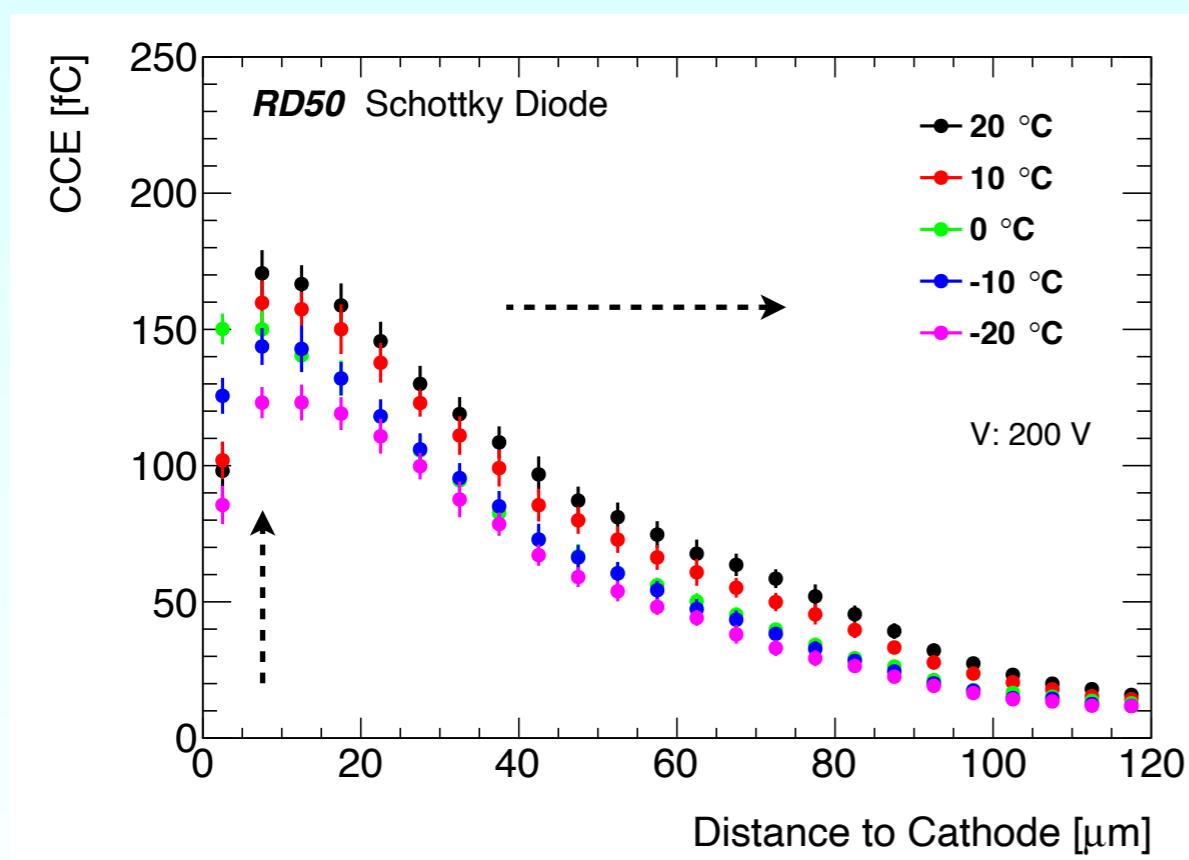
# CCE of un-irradiated PN junction

- T2 PN junction with 0.2 mm central hole,
- Bias Voltages: 50, 100, 200 V
- Temperatures: 20, 10, 0, -10, -20 °C



# CCE of un-irradiated PN junction

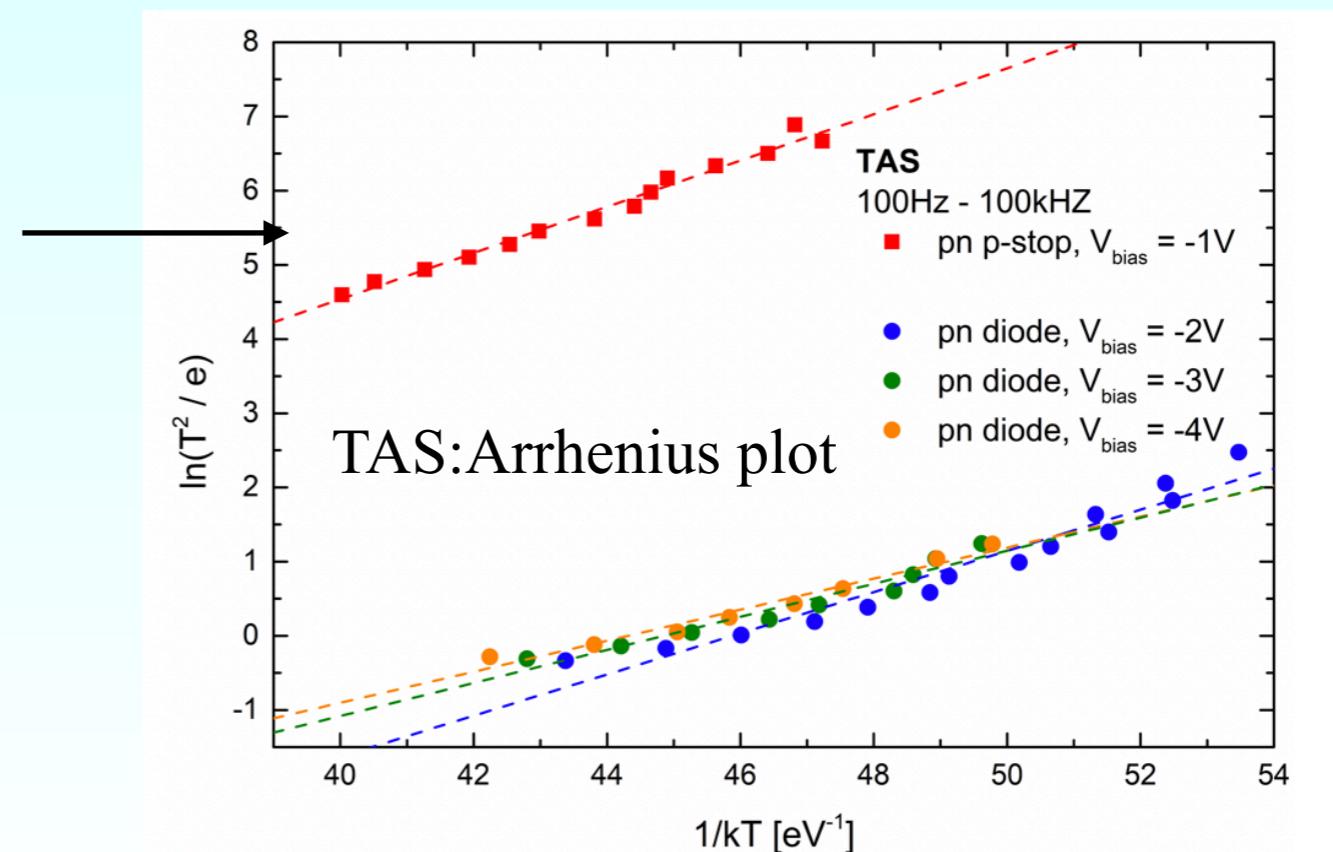
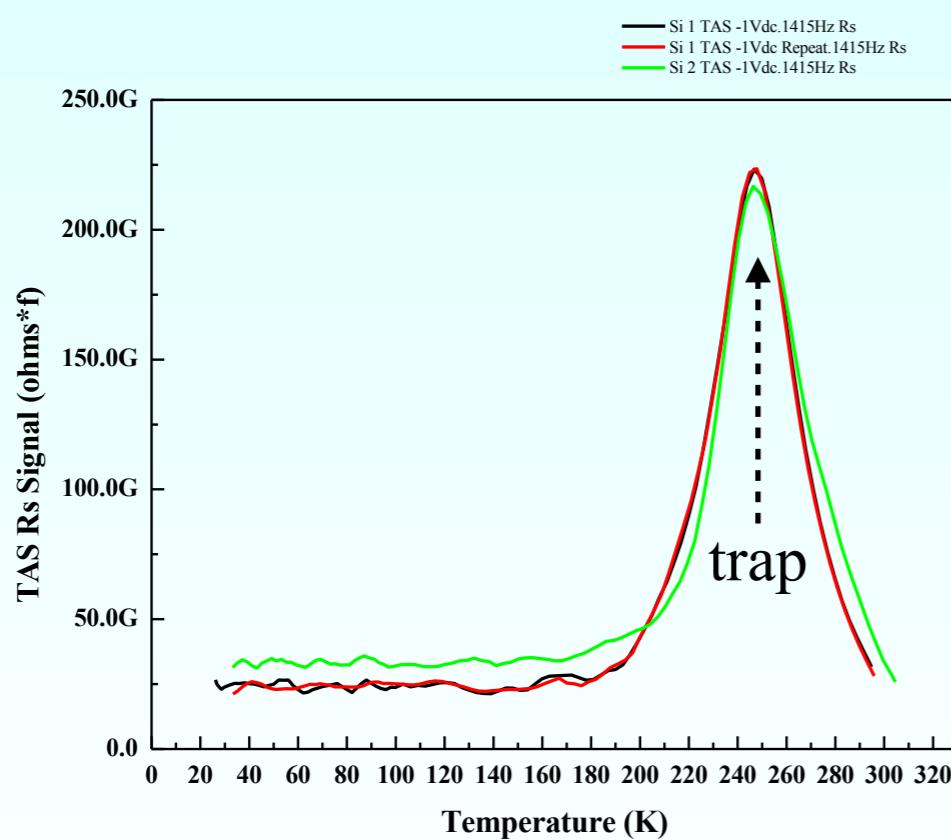
- Depleted thickness decreases with increased distance from the cathode edge,
- At fixed bias voltage, the higher the temperature, the larger the CCE, still under investigation,
- At low temperature, not fully depleted up to 100 V.



# Defect characteristics in TAS and DLTS

# Thermal Admittance Spectroscopy(TAS)

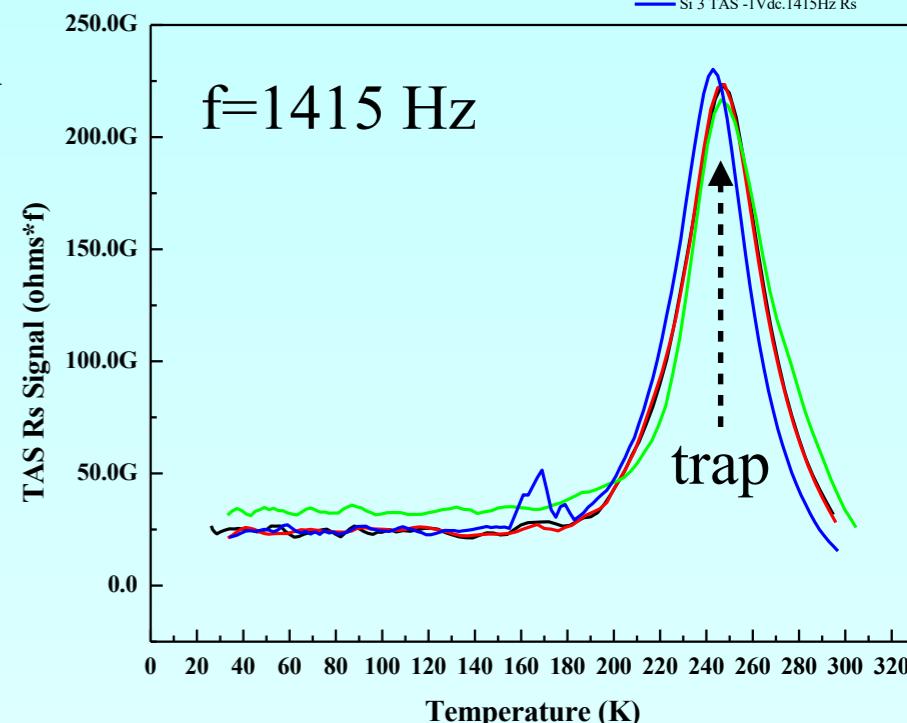
- TAS is steady-state measurement method to detect traps in the semiconductor:
  - Measure capacitance-C and conductance-G as function of frequency and temperature,
  - Defect contribution to C/G depending on test signal frequency and temperature,
  - Steps in C or peak in G temperature dependence indicate thresholds for new traps contributing.



# Defect characteristics of Schottky diode in TAS



- Un-irradiated Schottky diode has been shown in [Christoph's report](#) at 40th RD50 Workshop,
- 3 Irradiated( $1 \times 10^{15} n_{eq}/cm^2$ ) T3 Schottky diodes:
  - ♦ Frequency: 20 Hz -100 kHz,
  - ♦ 100 mV test signal amplitude, -1 V DC voltage applied on back.



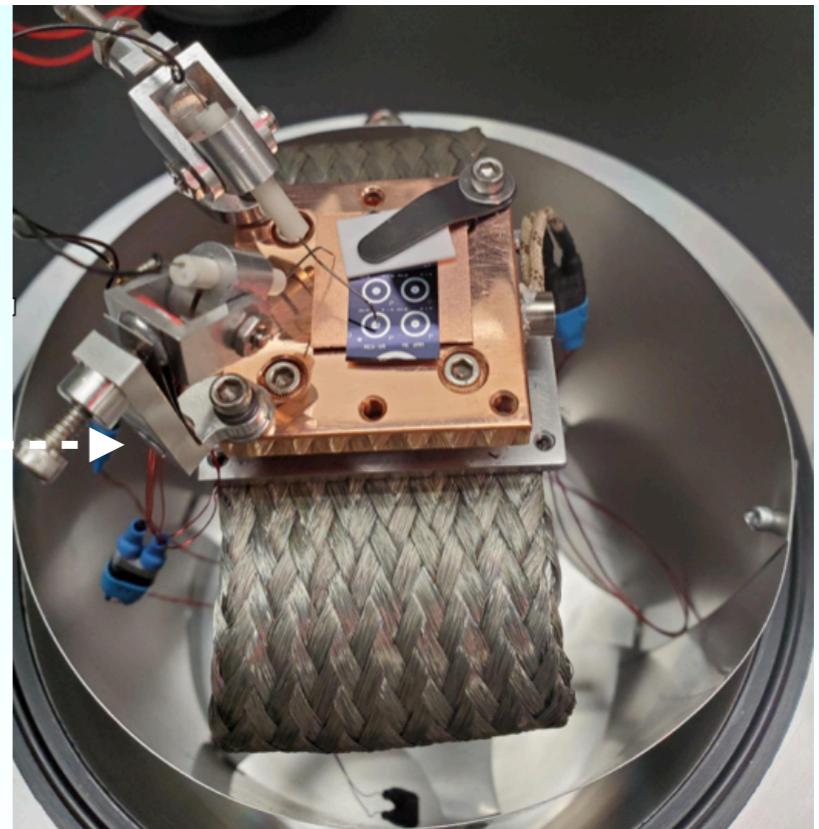
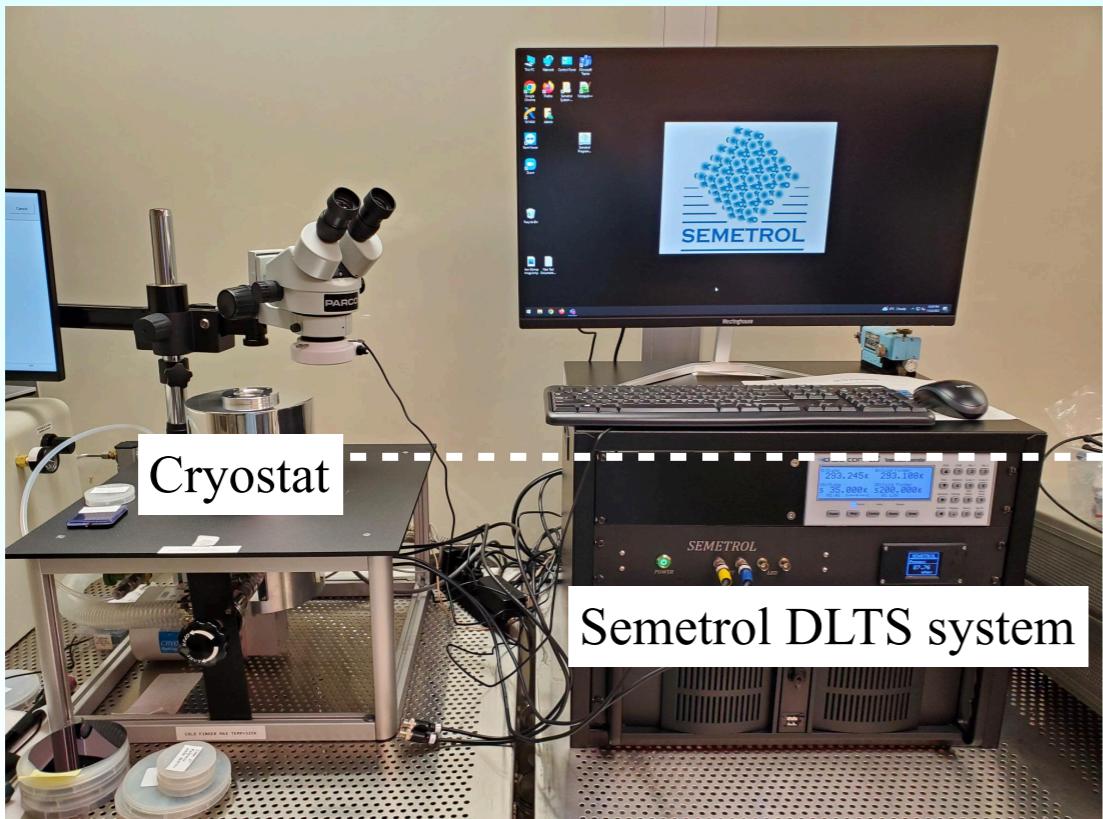
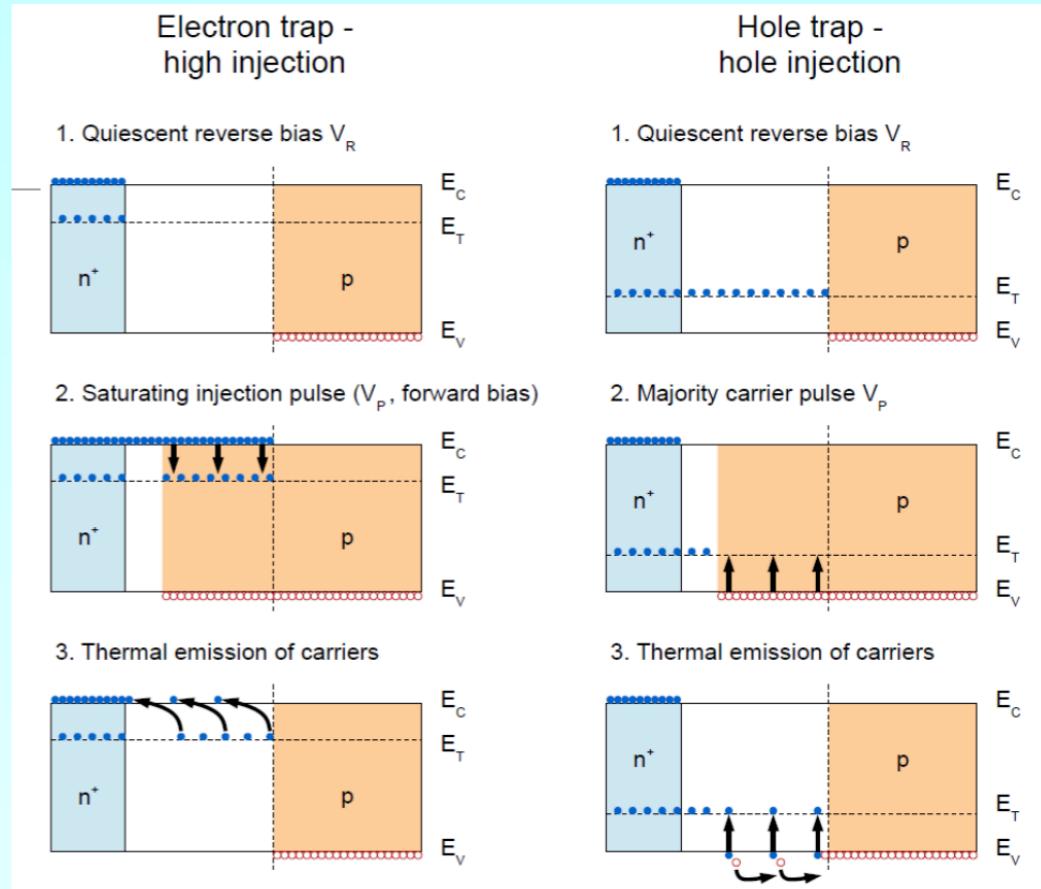
Arrhenius Summary					
File Name:	Midpoint Temperature (K)	Et (eV)	Delta Et (eV)	Capture Cross Section (cm <sup>-2</sup> )	Delta Sigma Mult.-Div. Factor
Si 1 TAS -1Vdc.Rs Arr	243.7	0.433	0.006	3.6E-14	1.3E+0
Si 1 TAS -1Vdc Repeat.Rs Arr	236.8	0.422	0.008	2.2E-14	1.5E+0
Si 1 TAS -5Vdc.Rs ARR	243.0	0.409	0.010	7.5E-15	1.7E+0
Si 2 TAS -1Vdc.Rs Arr	242.2	0.486	0.008	4.0E-13	1.5E+0
Si 3 TAS -1Vdc.Rs ARR	239.3	0.445	0.009	9.3E-14	1.5E+0

- Trap energy is 0.4-0.5 eV above the valence band with the scattering of  $\sim 60$  meV,
- Error bar on each individual measurement is  $< 10$  meV.

# Current Deep Level Transient Spectroscopy(I-DLTS)

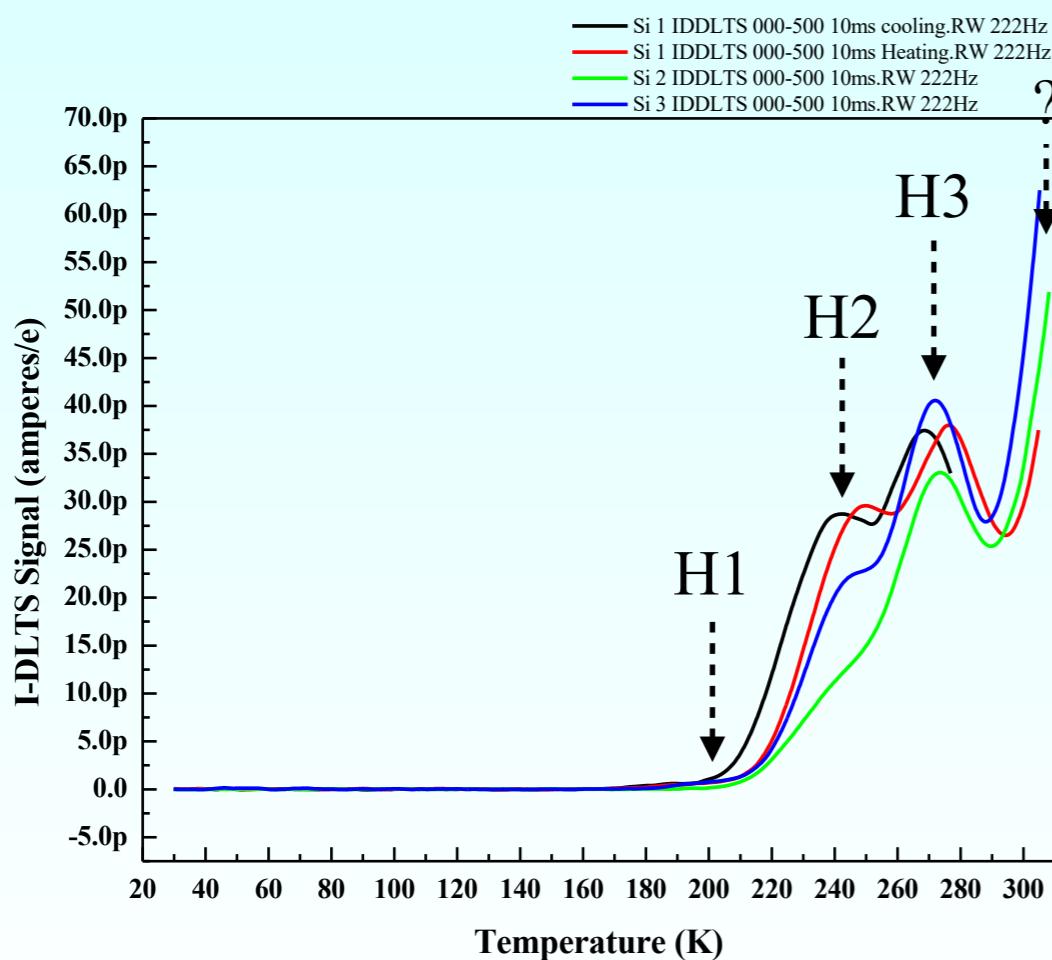


- Detects and amplifies current transients:
  - ♦ DUT is under constant reverse bias,
  - ♦ Fill pulse with specific voltage and duration,
  - ♦ Similar to DLTS, but no AC test signal, measures current transients.
- Useful for characterizing samples with small variations in capacitance, complement with TAS for each other.
- More details in [Christoph's report](#) at 40th RD50 Workshop.



# Defect characteristics of Schottky diode in I-DLTS

- 3 Irradiated( $1 \times 10^{15} n_{eq}/cm^2$ ) T3 Schottky diode,
- Filling pulse 0 V in 10 ms, then measure at -5 V(back),
- Trap signals at 200, 240, 270 K, possible trap at >300 K,
- Arrhenius plots to extract trap energy and cross-section.



Trap Concentration

Nt (1/cm <sup>3</sup> )	Si-1	Si-2	Si-3
H1	3.3E+08	1.0E+08	4.3E+08
H2	7.3E+09	4.3E+09	1.0E+10
H3	1.9E+10	1.8E+10	2.4E+10

Trap Energy

	Midpoint T (K)	E <sub>t</sub> (eV)	ΔE <sub>t</sub> (eV)	σ(cm <sup>2</sup> )	Δσ
H1	200				
H2	250	0.46	0.009	2.4E-15	1.5
H3	275	0.58	0.014	4.5E-14	1.8

## Summary and Outlook

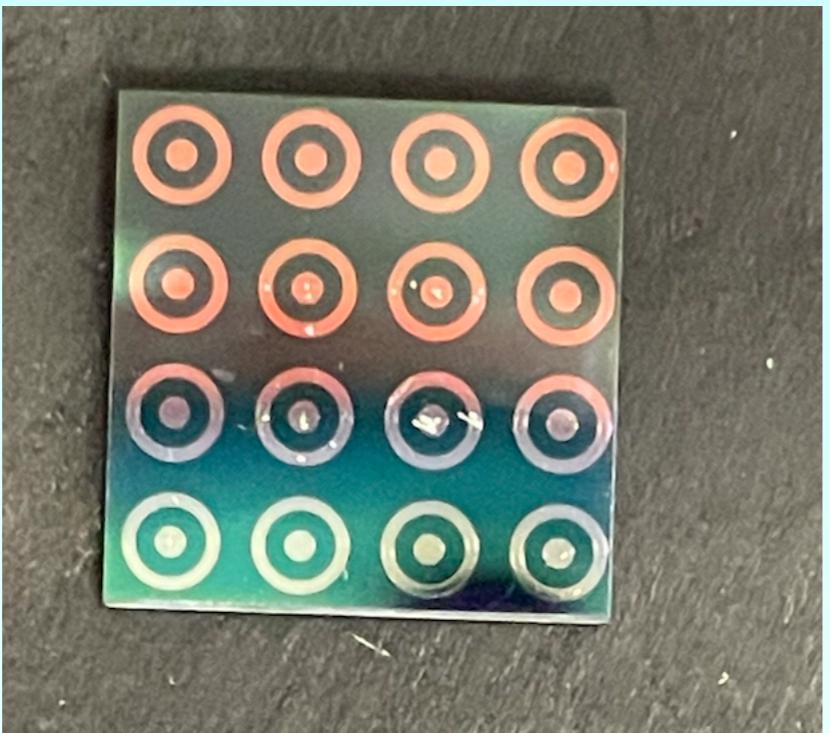
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- Several types of Schottky diode and PN junction were fabricated at RAL and Carleton,
- CCEs were measured on un-irradiated Schottky diode and PN junctions,
- Defect characteristics of irradiated Schottky diode were measured in TAS and I-DLTS,
- Need further understanding of the current measurement results, and compare with simulation,
- Irradiated PN junctions will come soon for CCE and defect measurement,
- Import the detected defects into TCAD for simulation.

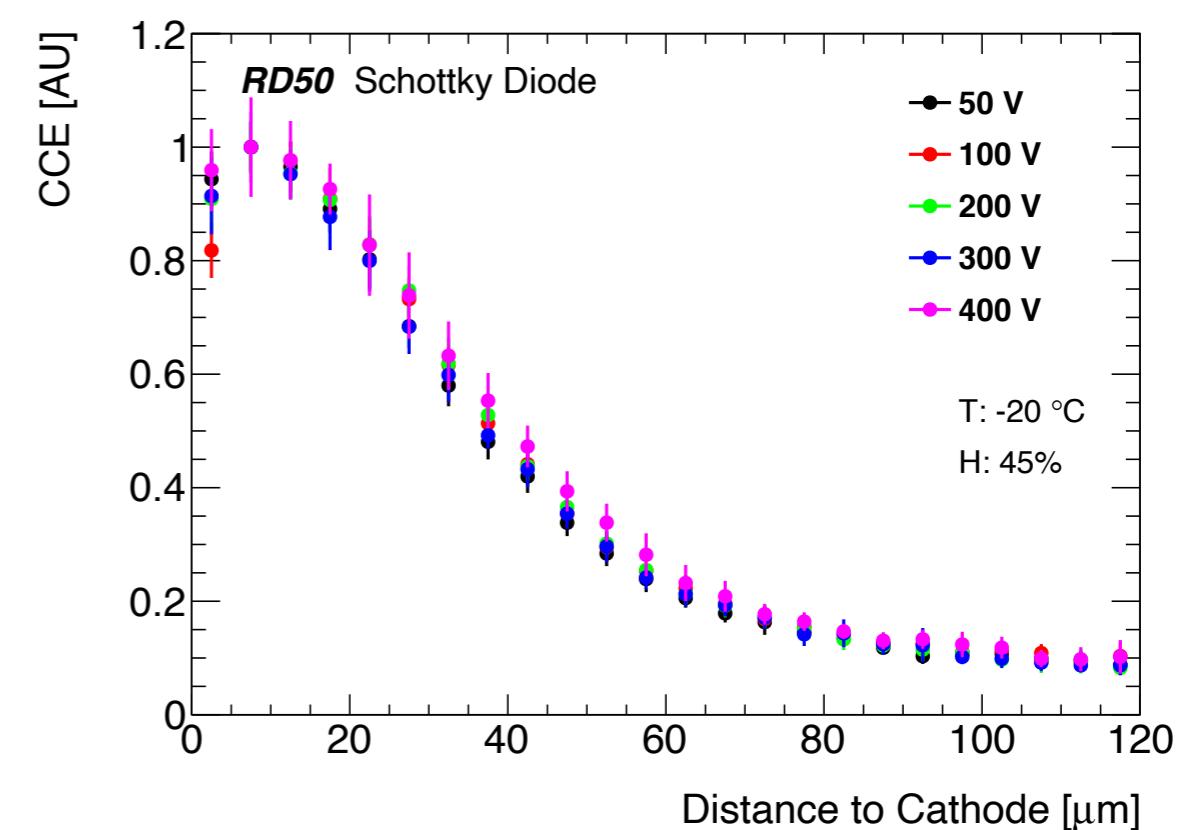
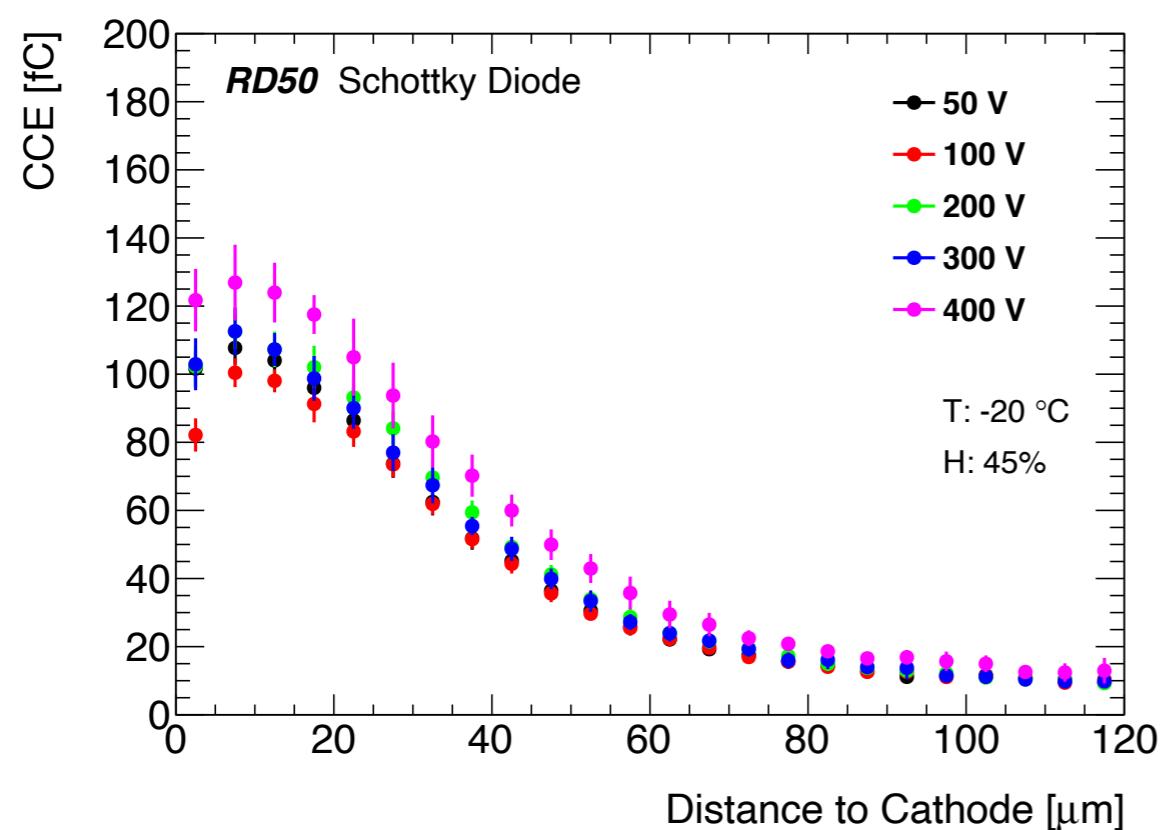
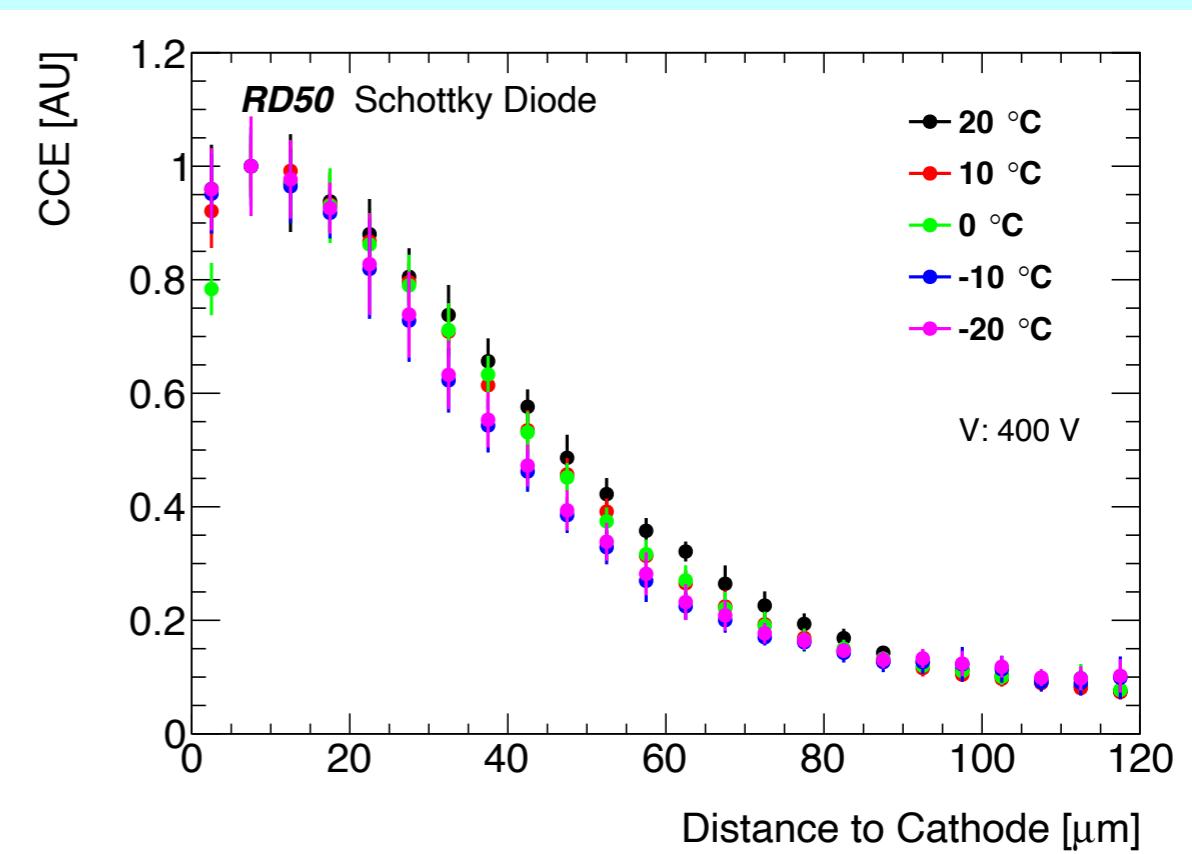
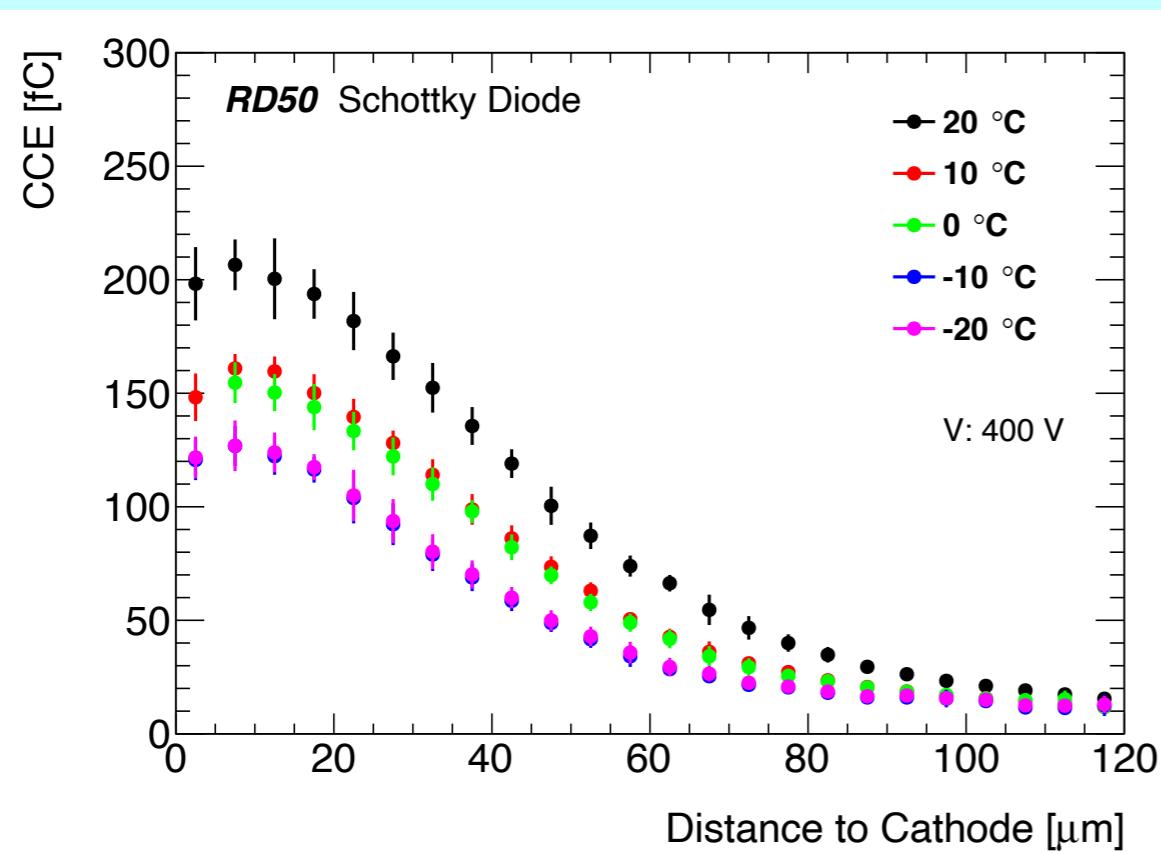
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Backup

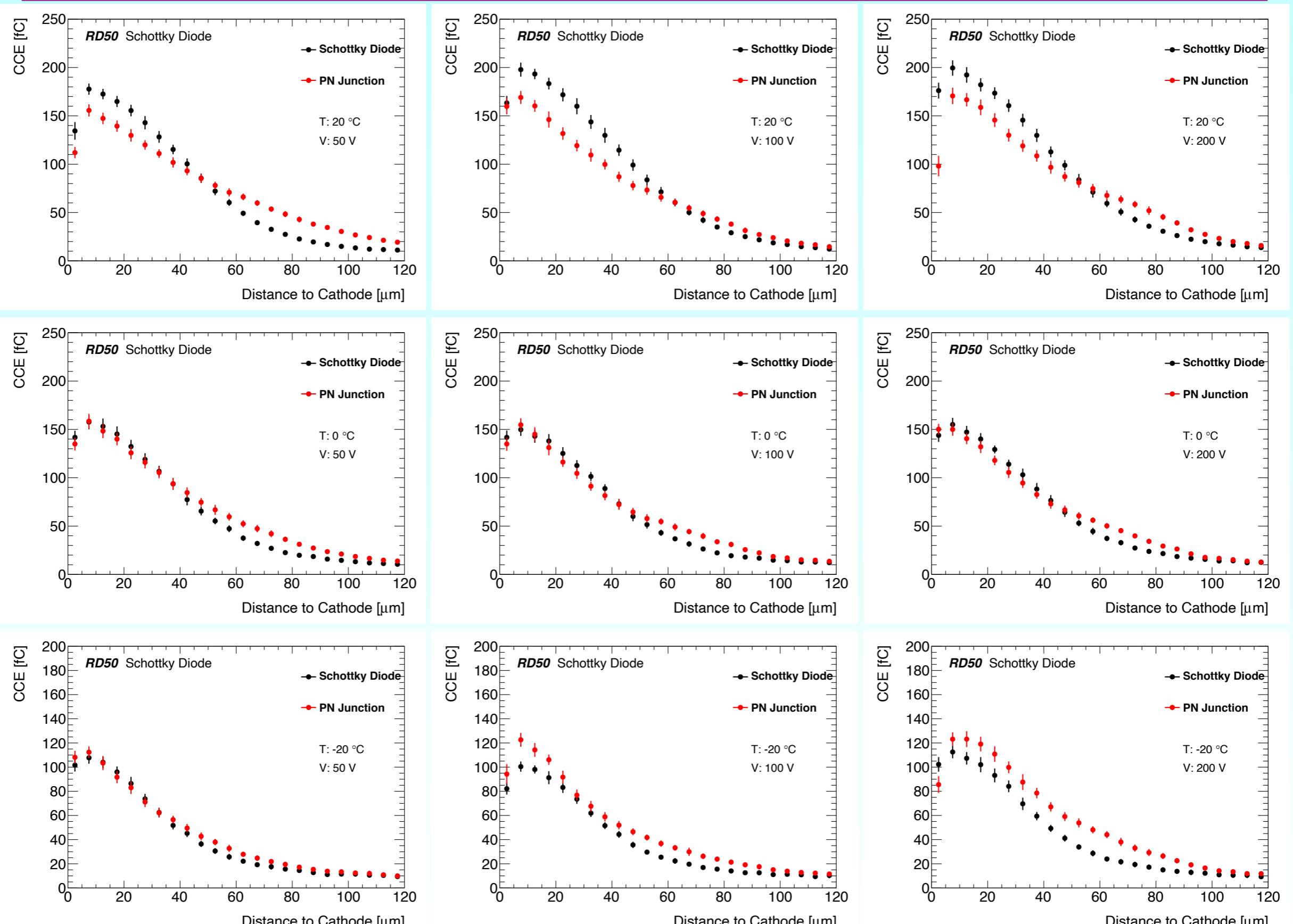
# Diced Die



# CCE of un-irradiated Schottky diode

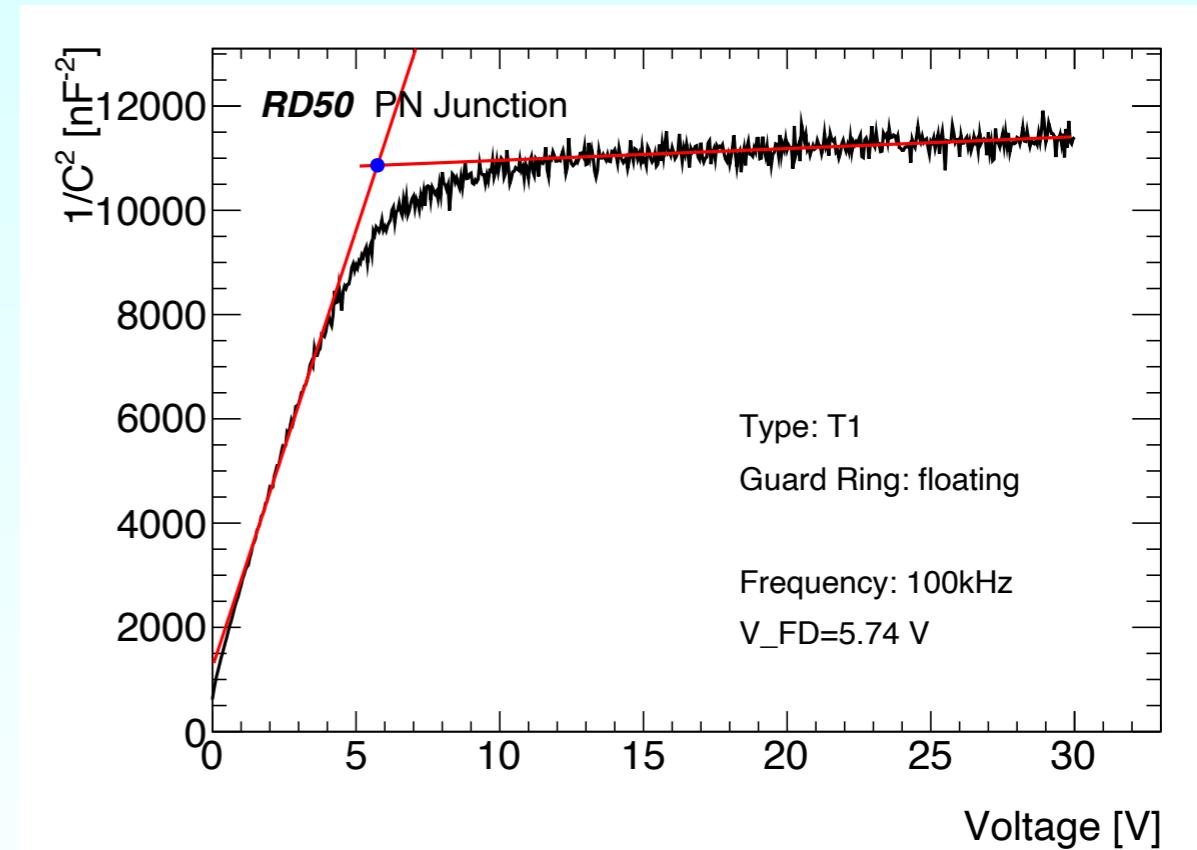
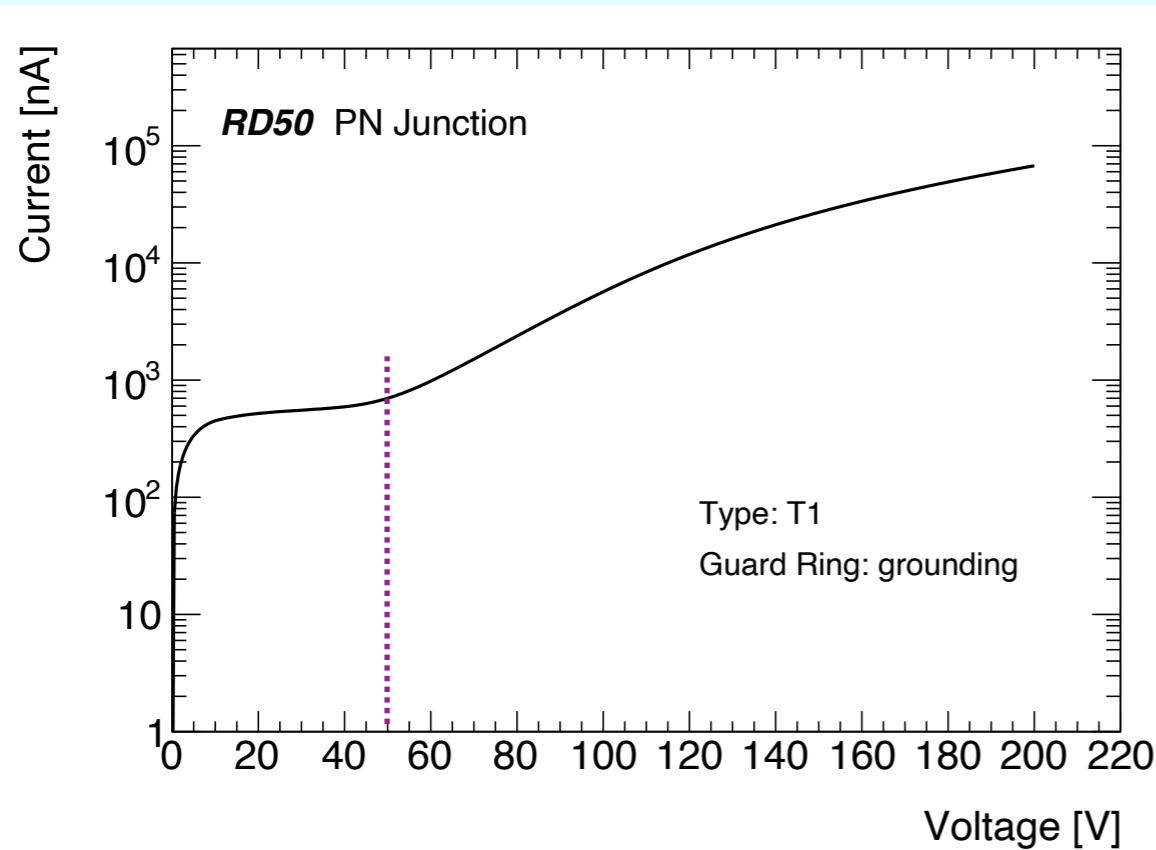


# CCE of un-irradiated Schottky diode and PN junction

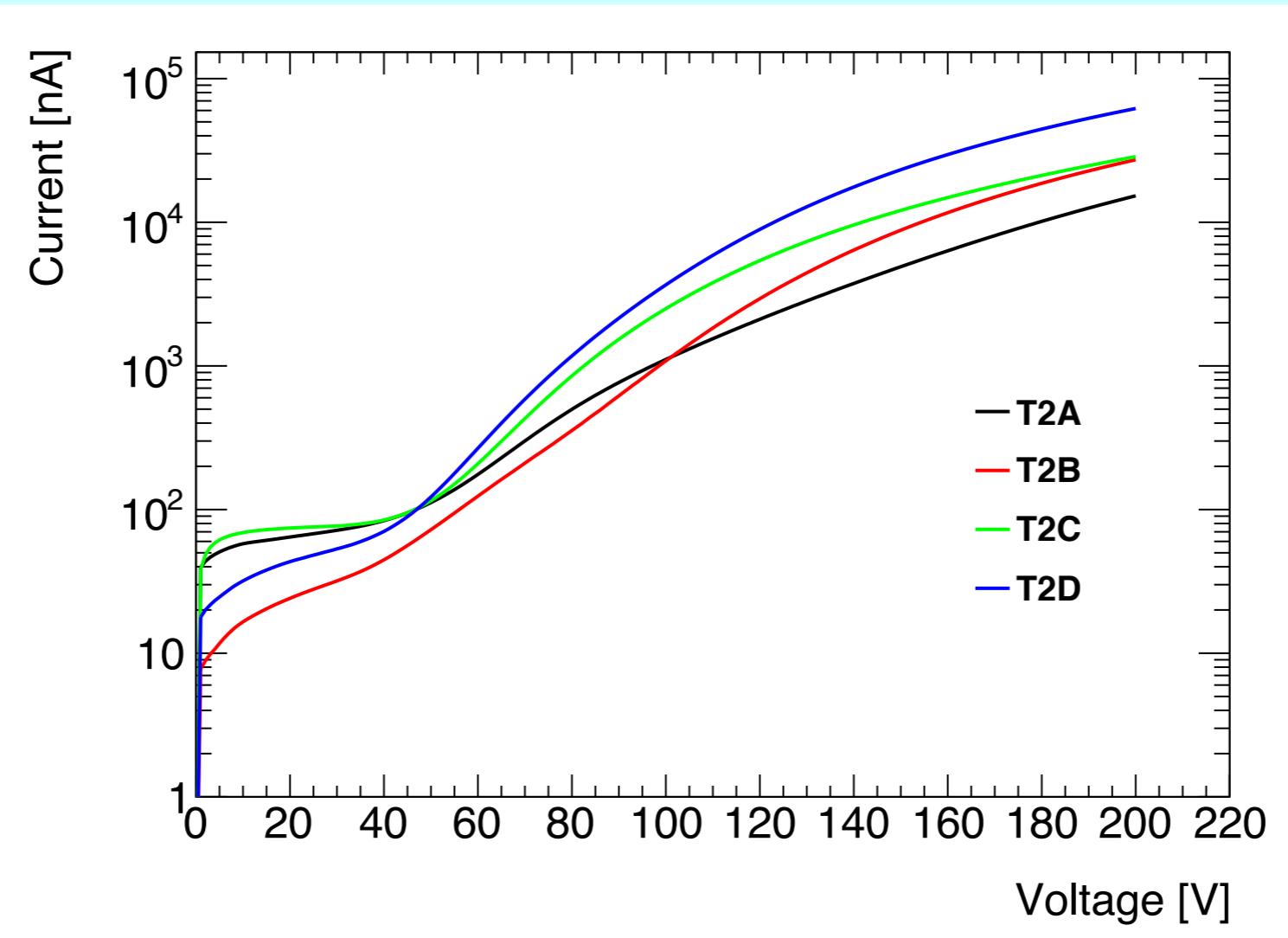


# IV/CV of un-irradiated PN junction

- Some leakage current for voltage above 50 V, but no breakdown up to 200 V
- Fully depleted voltage is  $\sim 5.74$  V



# CV of un-irradiated PN junction



# IV/CV of un-irradiated PN junction

- Fully depleted voltage is  $\sim 6$  V

