

AC-LGADs for 4D reconstruction

from ATLAS to EIC

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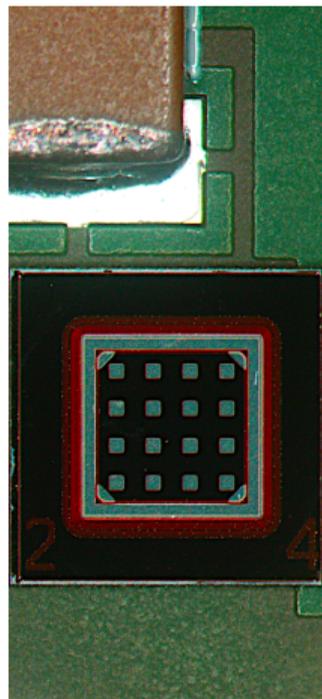
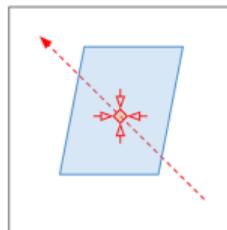


AC-LGADs — 4D DETECTION GOALS

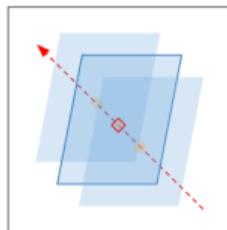
- Space resolution**

Driven by: **EIC, FCCee/hh**

Hit position res $< 5 \mu\text{m}$ for pile-up reduction and $\pi/K/p$ separation



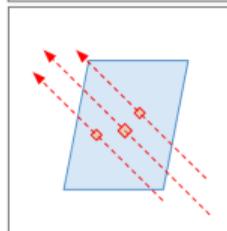
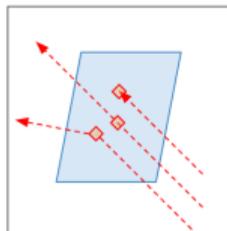
(info here)



- Time resolution**

Driven by: **FCChh**

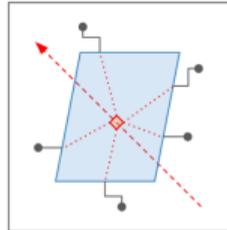
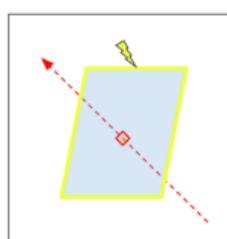
Time res/track $< 5 \text{ ps}$ for pile-up reduction/vertex disentanglement



- Radiation tolerance**

Driven by: **FCChh**

Fluence increasing by $\times 20$ compared to HL-LHC



- DAQ bandwidth**

Driven by: **EIC, FCCee/hh**

Number of channels to be readout increasing by a factor $\sim 5-10$ compared to HL-LHC

- Material budget**

Driven by: **EIC, FCCee**

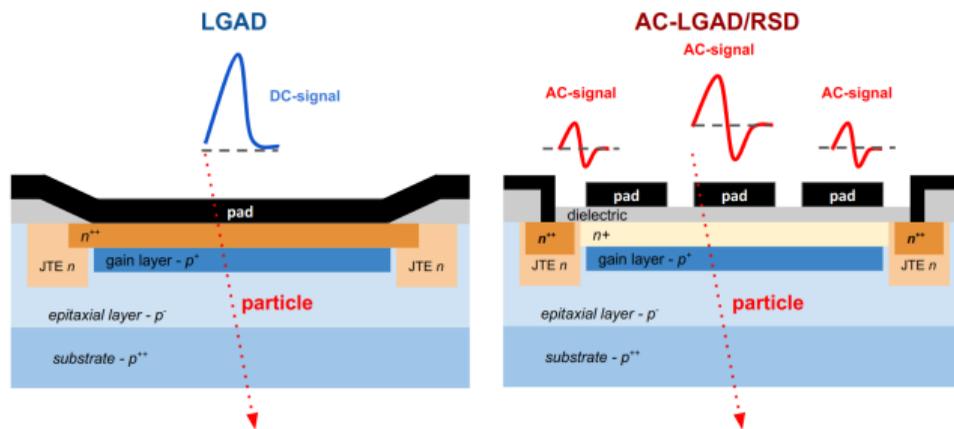
Equivalent thickness (per layer) $< 100 \mu\text{m}$ to minimize multiple scattering

- Power consumption**

Driven by: **EIC, (FCCee/hh)**

$< 1 \text{ mW/channel}$ in EIC RP due to location, beam proximity, ...

AC-LGADs — 4D DETECTION



AC-LGAD/RSD

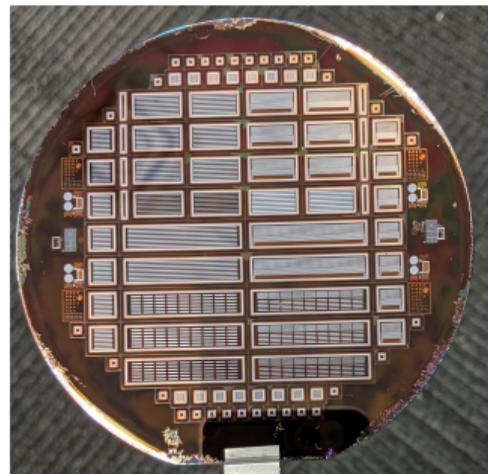
- Combines **internal gain** with internal **signal sharing**
- Keep 100% fill factor on thin substrate (30-50 μm)
- LGAD-level time resolution (< 30 ps) already proven
- Particle position reconstructed from signal shared on multiple pads
- Can achieve $\sigma_x < \frac{\text{pitch}}{\sqrt{12}}$ with ToT/analog info!
- Allows for high spatial resolution with smaller number of channels

AC-LGADs — BNL PRODUCTION

Silicon Fabrication Facility and wire-bonding @ *BNL Instrumentation Div.*
Class-100 Clean Room, full characterization, design and simulation of
silicon sensors @ *Si-Lab*

New 2022 Production includes:

- ● **Long Strip AC-LGAD** (ETA next week, great spatial resolution vs number of channels; available before January 2023 testbeam season) (A.Apresyan@CPAD2022)
- ● **EICROC AC-LGAD** (ETA December 2022, focused on studies for EIC)



Furnaces for dry oxidations and annealings



Double-sided mask aligner



Wet bench (HF, RCA I & II, piranha, polvetch. ...)



Sputtering (Al, Al1%Si, Ti)



RTA for sintering

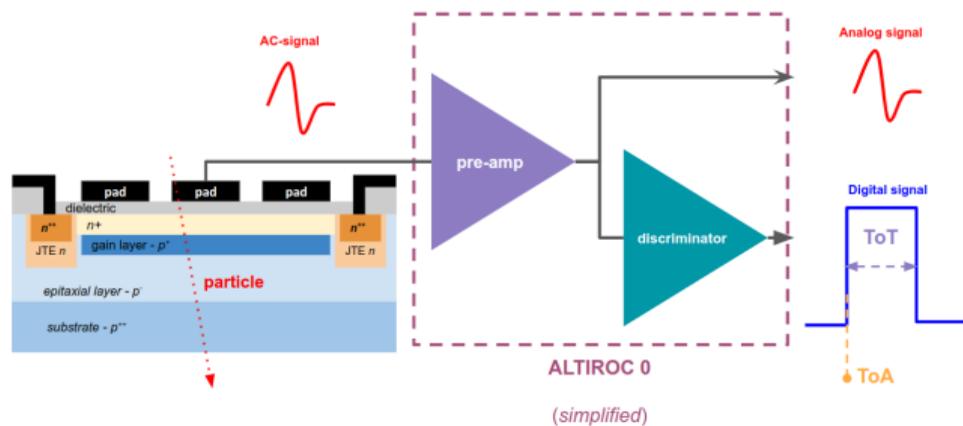


Laser dicing

ALTIROC 0 — OVERVIEW

G.D'Amen et al., Signal formation and sharing in AC-LGADs using the ALTIROC 0 front-end chip, JINST 17 2022

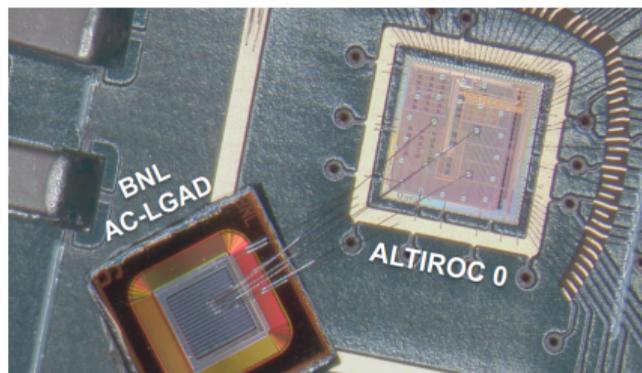
In large-scale, multi-channel systems targeting 4D tracking, we need to evaluate AC-LGAD performances when coupled to higher-complexity readout systems.



ATLAS LGAD TIMING ROC

- ● ALTIROC designed for LGAD (unipolar/DC-) signals for ATLAS High-Granularity Timing Detector (HGTD).
- ● Compatibility to AC-LGAD bipolar signals not ensured!
- ● **ALTIROC 0 ASIC** first prototype of ALTIROC chip (CMOS 130 nm); includes Pre-amplifier (Analog VPA signals) + Discriminator (Digital signals) for ToT measurement

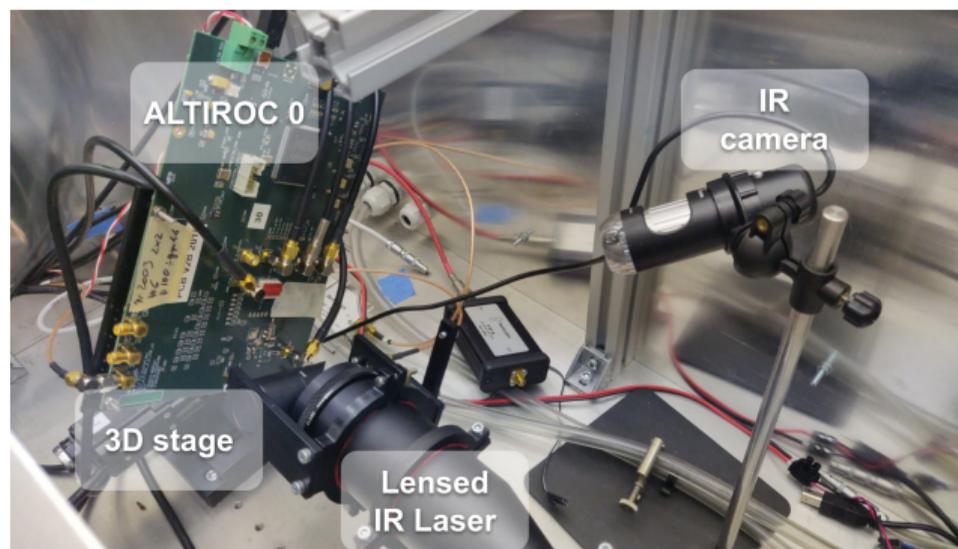
ALTIROC 0 — COUPLING TO AC-LGAD



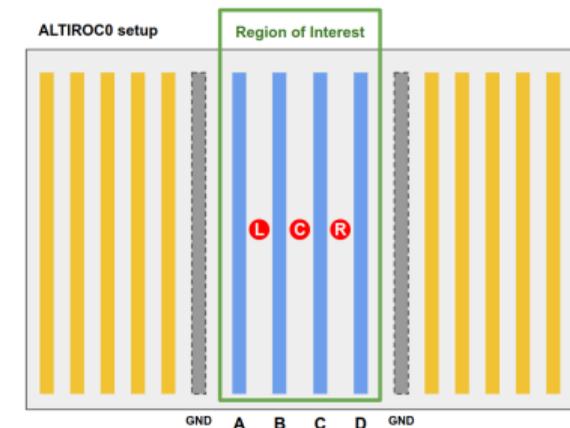
BNL AC-LGAD characteristics

- ● Area: $2 \times 2 \text{ mm}^2$
- ● 16 strips
- ● strip pitch $100 \mu\text{m}$, gap $44 \mu\text{m}$
- ● $V_{\text{bias}} = -170 \text{ V}$

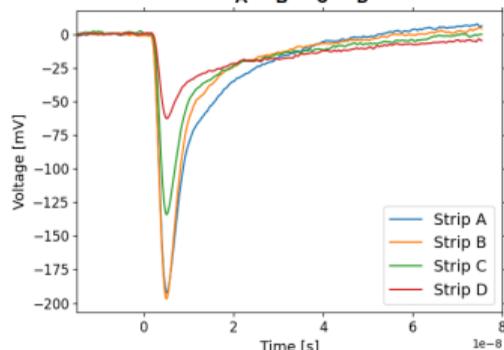
Betas from ^{90}Sr and IR Laser from TCT used to characterize ALTIROC response to AC-coupled signals



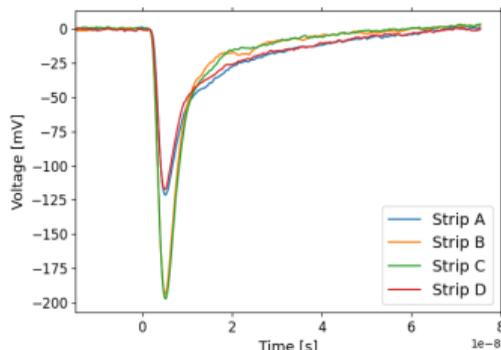
ALTIROC 0 — VPA CHARACTERIZATION



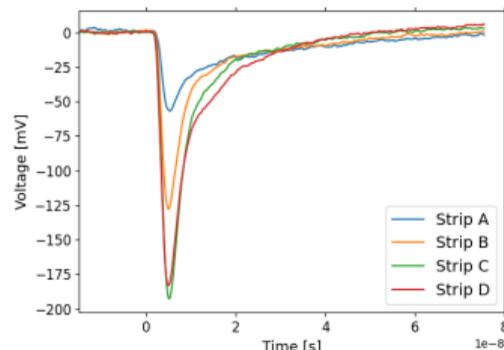
- Signals acquired at the ALTIROC 0 VPA stage on four strips when the laser is focused at the left, center, or right of the sensor
- The laser injects 32 mip on the sensor
- Signal amplitude decreases linearly with distance due to the resistivity of the n^{++} layer



Point L



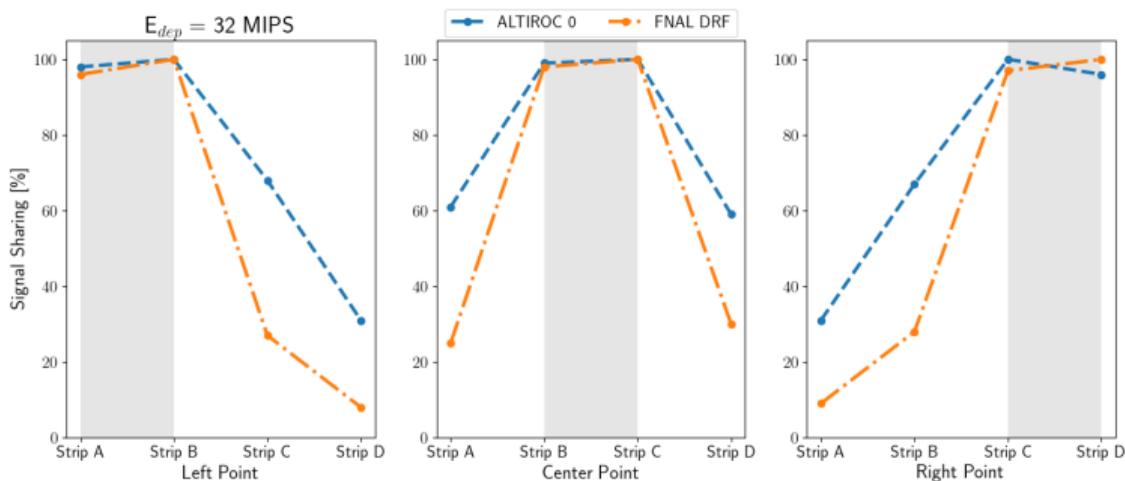
Point C



Point R

ALTIROC 0 — SIGNAL SHARING PROFILE

Signal sharing profile on AC-LGAD strips read out by ALTIROC 0 or a discrete RF amplifier (FNAL DRF)

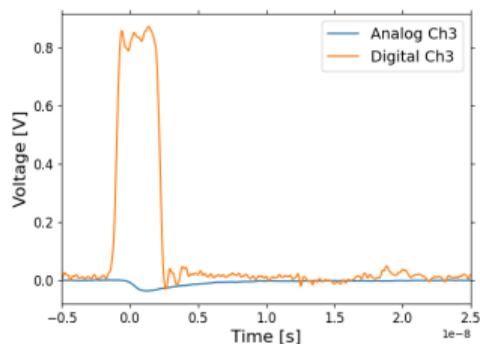


$$\text{Signal Sharing}_i [\%] = \frac{A_i}{A_{highest}}$$

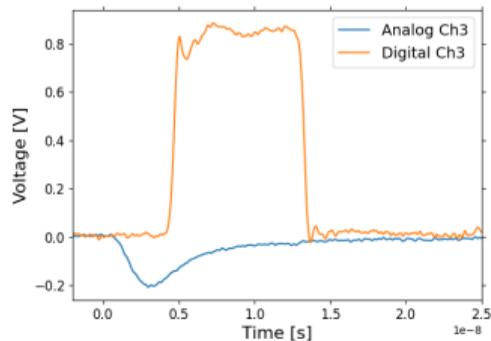
- ● A_i : Signal amplitude measured by i -th strip
- ● $A_{highest}$: Signal amplitude measured by the strip closest to the focus-point (gray area)

Measured difference in signal sharing profile can be explained, on first order, due to different input impedance of ALTIROC 0 and the RF amplifier

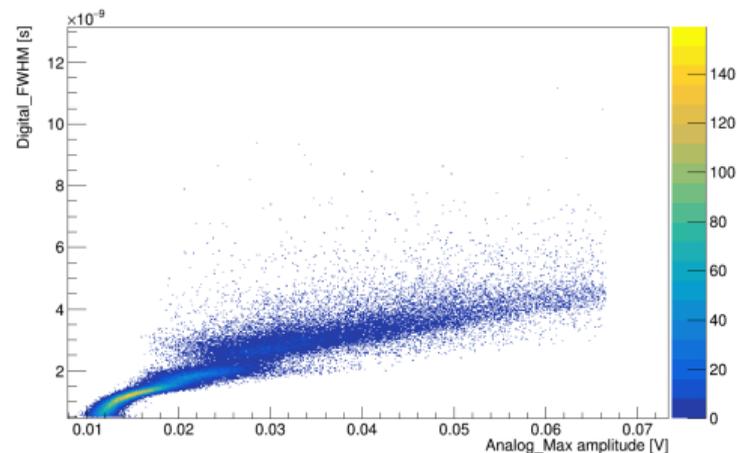
ALTIROC 0 — DIGITAL RESPONSE



Analog and digital output of ALTIROC extracted from Strip C generated by the interactions of **betas** (top) and **IR laser** (bottom)



Width of the digital signal (ToT) proportional to the amplitude of the analog signal



- FWHM of discriminator output as function of the amplitude of the analog signal
- Interaction with beta particles leaves a long tail of deposited energies
- Univocal dependence on the analog signal amplitude/deposited energy

ALTIROC 0 ENERGY SENSITIVITY

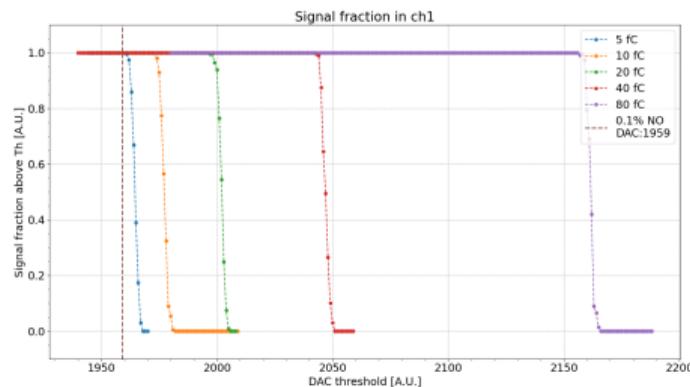
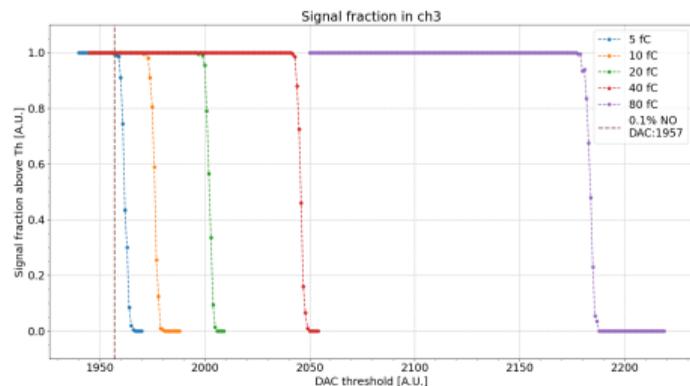
- Fast signal injected from pulse generator
- S-curve of digital signal fraction** computed for multiple (200) DAC points in wide range

$$\text{SIGNAL}\% = \frac{\text{SIGNALS ABOVE } > 500 \text{ mV}}{\text{TOTAL SIGNALS}}$$

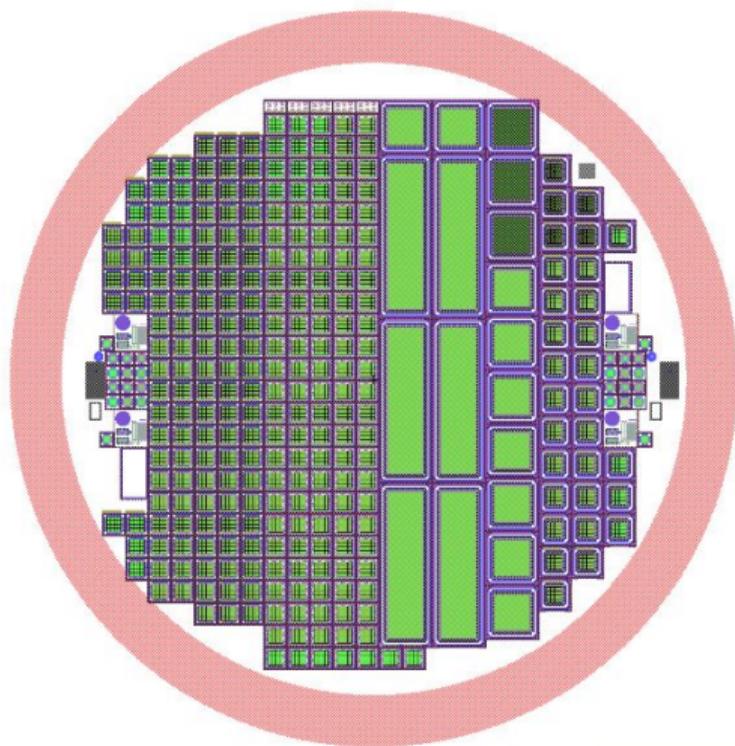
S-curves scan repeated with **multiple input charges (5 fC, 10 fC, 20 fC, 40 fC and 80 fC)** obtained by modulating input signal amplitude (50 - 800 mV)¹

Can discriminate signals with charge as low as 5 fC

¹ALTIROC0 input capacitance: 100 fF and $Q = C \cdot V$



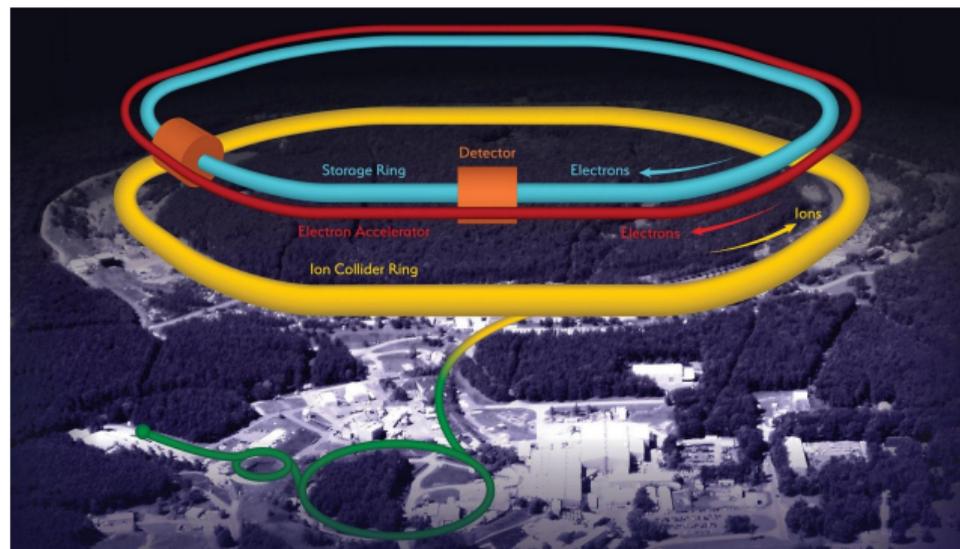
AC-LGADs FOR EIC



EIC — THE ELECTRON ION COLLIDER @ BNL

EIC PARAMETERS

- High Luminosity: $\mathcal{L} = 10^{33} - 10^{34} \text{ cm}^{-2} \text{ s}^{-1}$, 10–100 $\text{fb}^{-1}/\text{year}$
- Highly Polarized Beams: 70%
- Large Center of Mass Energy Range: $E_{\text{cm}} = 20 - 140 \text{ GeV}$
- Electron Beam: 5-18 GeV Ion (protons - Uranium): 40, 100-275 GeV
- Large Detector Acceptance and Good Background Conditions
- Accommodate two Interaction Regions (IR)



EICROC — FUNDAMENTALS

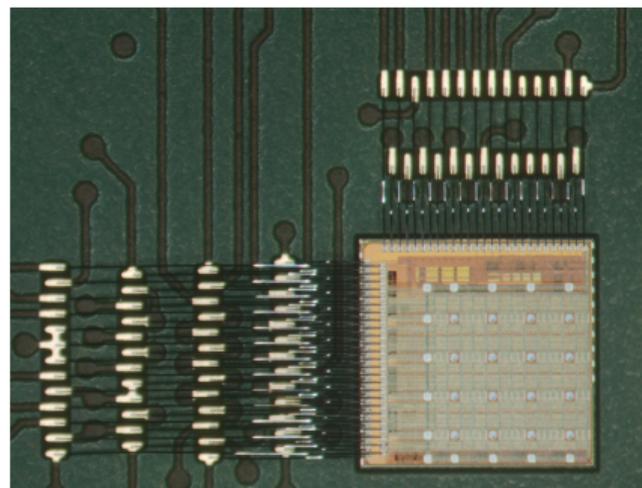
EIC Roman Pots (RP): aim for $500 \times 500 \mu\text{m}^2$ pixels with ~ 30 ps time resolution (O.Hartbrich@CPAD 2022)

- ● 1,310 cm^2 silicon, 128 modules, 512 ASICs (32×32 channels), $\sim 500\text{k}$ channels
- ● Signal sharing between pixels to improve time and space resolution
- ● Low occupancy
- ● Low radiation environment
- ● Triggerless system

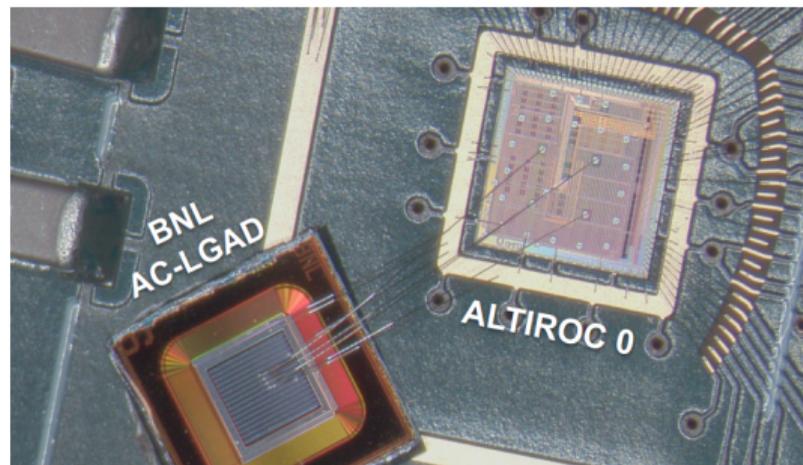
1st ASIC prototype (EICROC 0) for EIC Roman Pots, based on ALTIROC experience

- ● TDC for ToA and ADC for amplitude measurements exploit Signal Sharing

Similar design may be used in EIC ToF detector

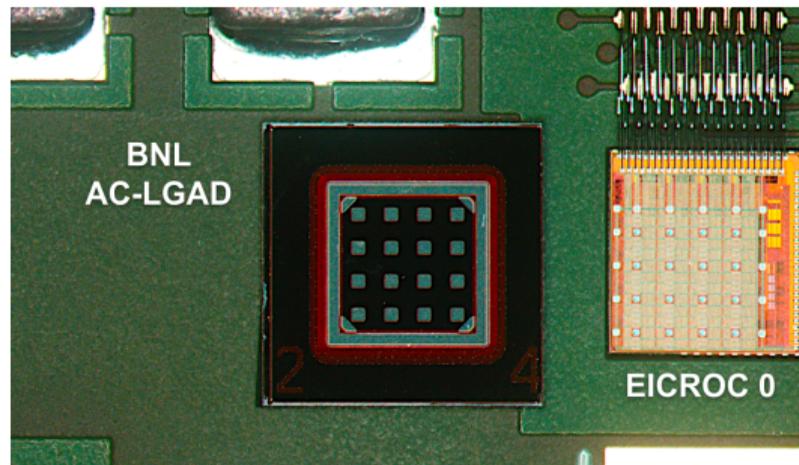


EICROC — MAIN DIFFERENCES WITH ALTIROC



ALTIROC 0

TARGET SENSOR	DC-LGAD
PIXEL SIZE	$1.3 \times 1.3 \text{ mm}^2$
CHANNELS	4
PIXEL CAPACITANCE	4 pF
TDC (TOT)	8bit/10bit



EICROC 0

TARGET SENSOR	AC-LGAD
PIXEL SIZE	$0.5 \times 0.5 \text{ mm}^2$
CHANNELS	16
PIXEL CAPACITANCE	0.5 pF
ADC (AMPLITUDE)	8bit@40MHz

EICROC — TESTING STRATEGY

ALREADY AVAILABLE

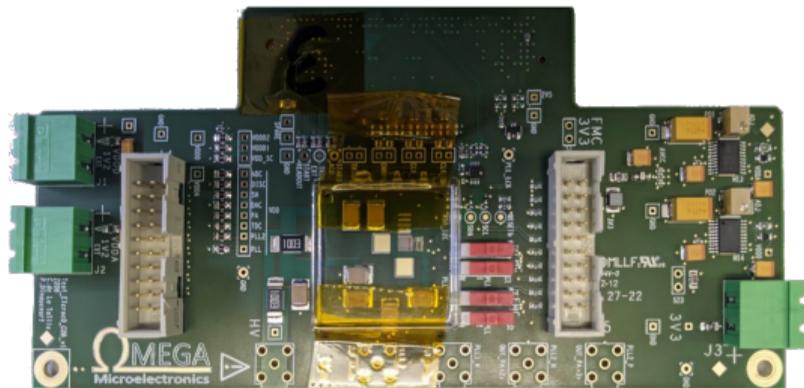
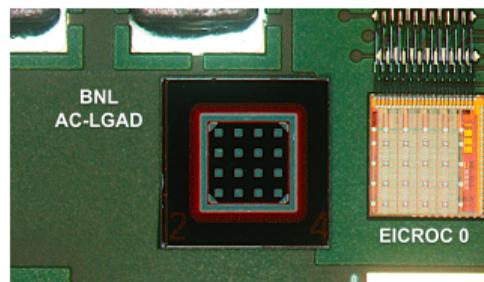
- ● EICROC 0 bonded to custom designed mezzanine board and readout via XILINX ZYNQ-7000 ZC706 evaluation board
- ● BNL AC-LGAD wire-bonded to EICROC 0

UNDER CONSTRUCTION

- ● Firmware & C/C++ Embedded Software under development by IJCLAB team
- ● Dedicated AC-LGAD design coming soon

NEXT STEPS...

- ● Characterization of ADC linearity for signal sharing
- ● Study of detector response to TCT (IR laser) and particle sources/test beams



FMC MEZZANINE BOARD, design by OMEGA Team

RECAP & CONCLUSIONS ●

- ● The next generation of accelerators will pose several experimental challenges; this requires a **new generation 4D detector**
- ● The AC-LGAD paradigm proved to be a prime candidate for 4D reconstruction thanks to its fast timing and signal sharing capabilities, among others
- ● A new detector requires a **dedicated readout system**: we have successfully read out a BNL-made AC-LGAD using the ALTIROC 0 chip, designed for DC-LGADs
- ● AC-LGAD dedicated readout system for EIC application, **EICROC** (based on the ALTIROC design) is being developed by OMEGA and IJCLAB
- ● A first chip prototype, EICROC 0, is now available and has been coupled to a BNL AC-LGAD
- ● The readout system is currently under development and will be tested following the procedures developed during the AC-LGAD + ALTIROC 0 testing campaign

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- ● S. Robinson
- ● D. Pinelli
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- ● T. Kersten

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from the **Universite Paris-Saclay, CNRS/IN2P3, IJCLab** for the design of the readout board and software.

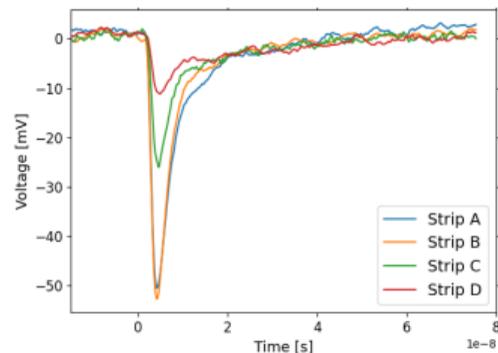
- ● A. Apresyan
- ● R. Heller
- ● C. Madrid

from Fermilab for their work and expertise on the Discrete-RF board

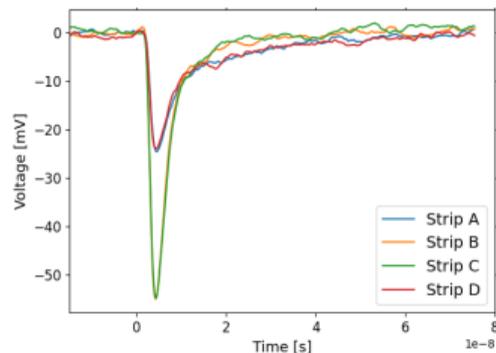
This material is based upon work supported by the U.S. Department of Energy under grant DE-SC0012704. This research used resources of the Center for Functional Nanomaterials, which is a U.S. DOE Office of Science Facility, at Brookhaven National Laboratory under Contract No. DE-SC0012704.

BACKUP

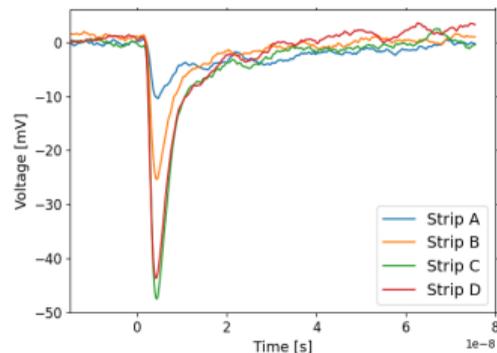
ALTIROC 0 ● — 11 MIPS vs 32 MIPS



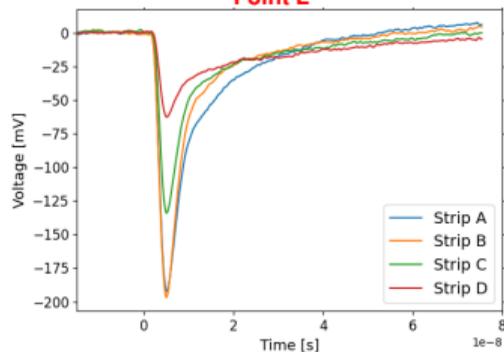
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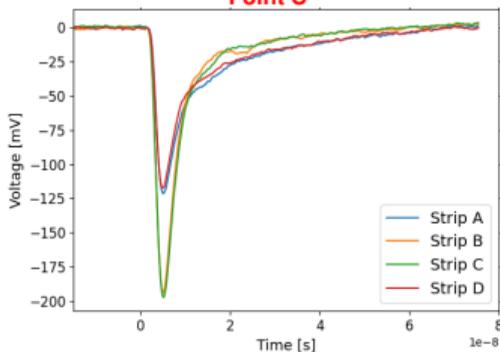
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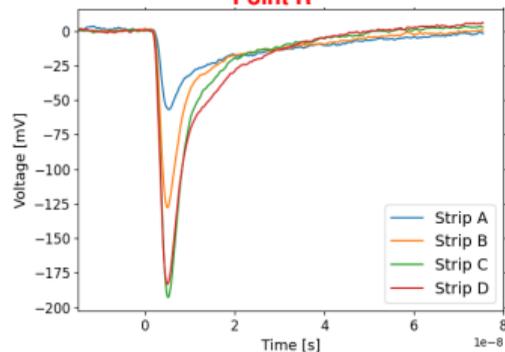
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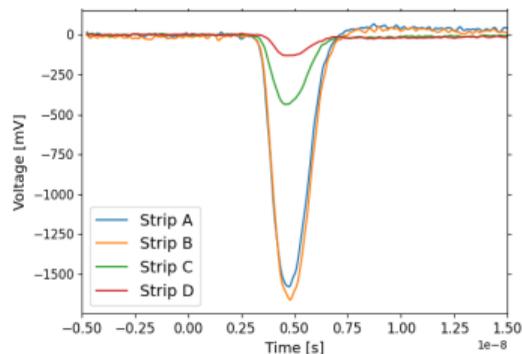


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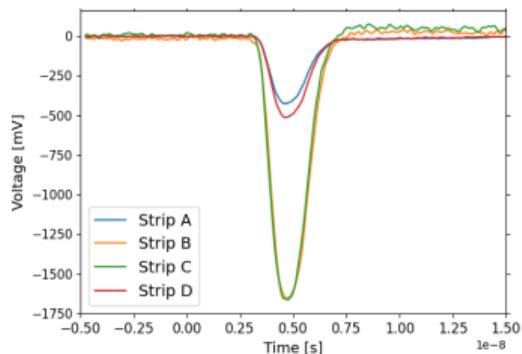


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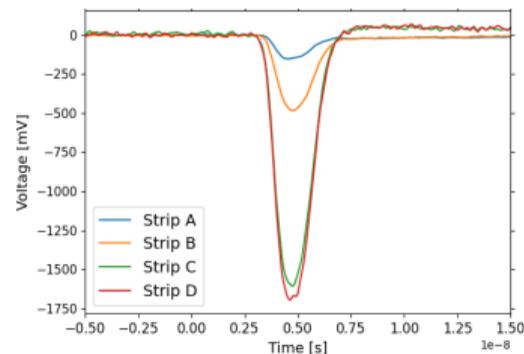
IR LASER ● — ALTIROC vs FNAL



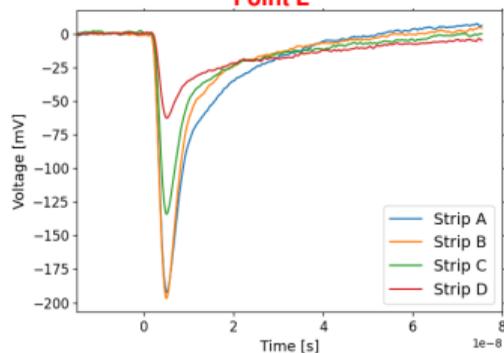
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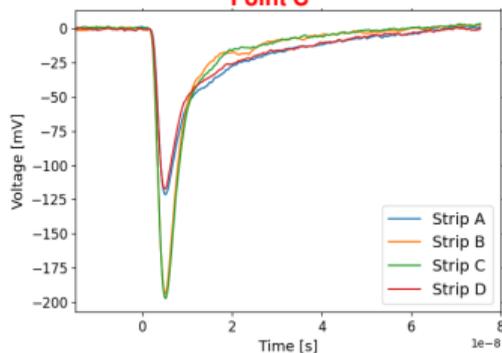
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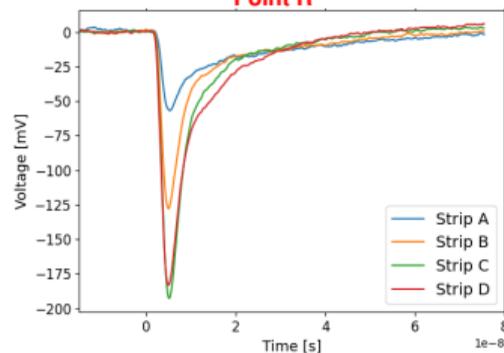
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DIGITAL CHARACTERIZATION - TRIMMING

