UKRI-MPW0: A proof-of-concept, backside biased only High Voltage CMOS pixel chip

E. Vilella, M. Franks[1], J. Hammerich, N. Karim[2], S. Powell, B. Wade, C. Zhang

University of Liverpool

[1]Now with ETH Zürich

[2]Now with Leonardo UK Ltd

vilella@hep.ph.liv.ac.uk

Motivation

- **To improve radiation tolerance of HV-CMOS sensors**
  - Increasing V_BD
  - With HV backside biasing

UK Research and Innovation UNIVERSITY OF LIVERPOOL

State-of-the-art

- **150 nm HV-CMOS LFoundry – Traditional cross-section**
  - P-substrate/DNWELL sensing junction
  - Topside p-type contacts to bias the p-substrate to HV
  - Pixel readout electronics embedded inside DNWELL

e.g. RD50-MPWx pixel chips, hyperlinks:

Vilella PoS(Vertex2019)019
Marco JPS Conf. Proc. 010008 (2021)
Vilella NIMA 2022 166826

Breakdown start

V_{HV} V_{DN} V_{HV}
PW NW PWELL NWELL PWELL NWELL PW
NISO PSUB NISO
DNWELL
p-
LFoundry 150 nm
280 µm
3 µm 3 µm
50 µm

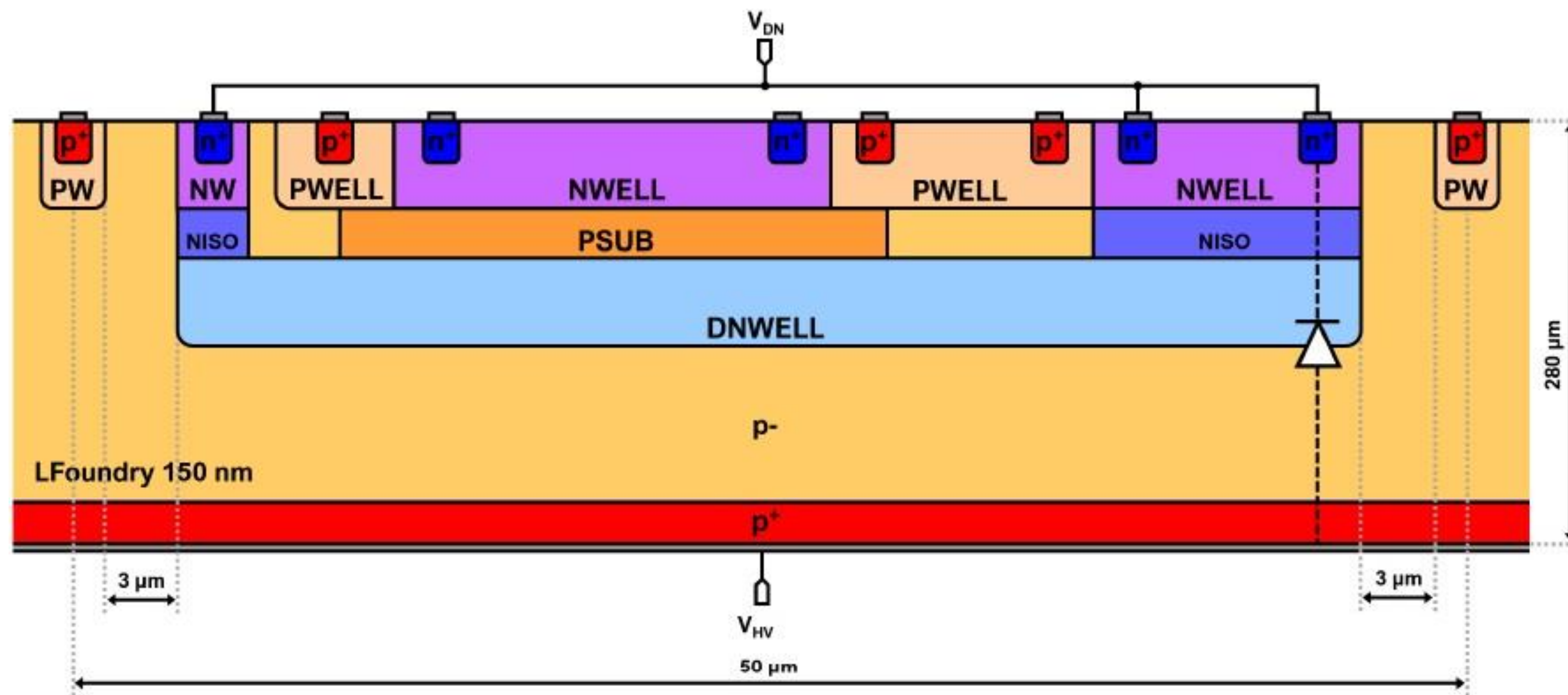
UK Research and Innovation
UNIVERSITY OF LIVERPOOL

State-of-the-art

- **150 nm HV-CMOS LFoundry – Optimised cross-section**
  - P-substrate/DNWELL sensing junction
  - Backside p-type contacts to bias the p-substrate to HV, keeping topside p-type contacts
  - Pixel readout electronics embedded inside DNWELL

e.g. H35DEMO, LF-CPIX, hyperlinks:

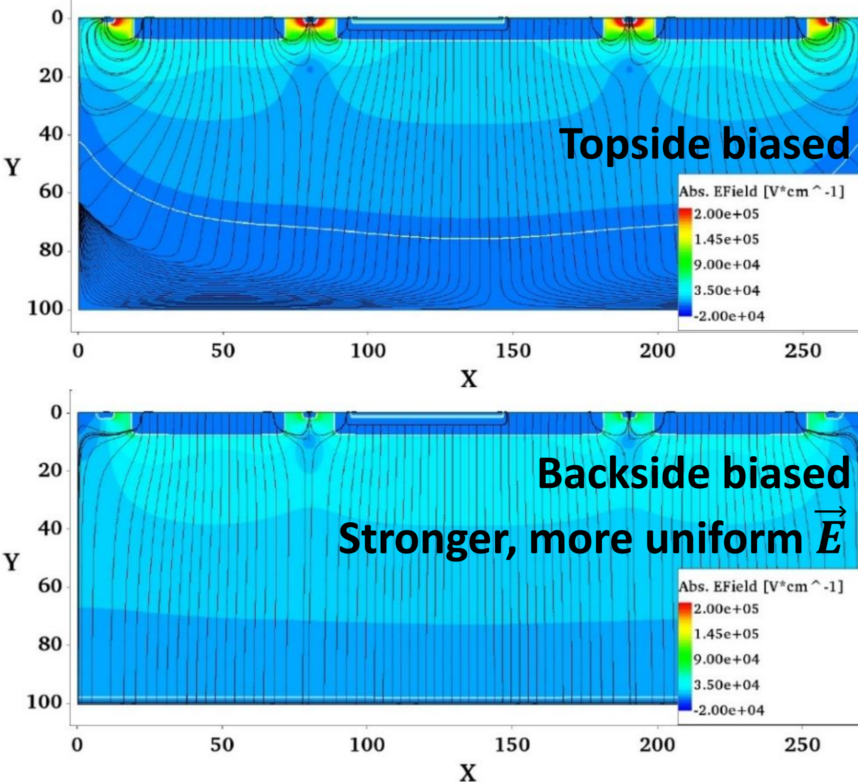
Franks NIMA 2021 164949
Mandic arXiv:1801.03671v2 2018
Meng CERN-THESIS-2018-153



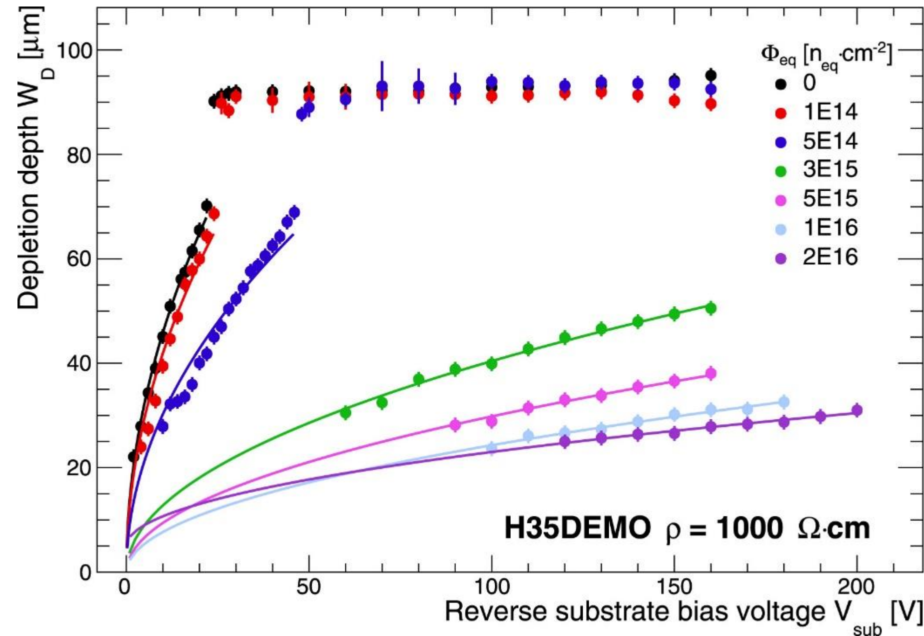
UK Research and Innovation
UNIVERSITY OF LIVERPOOL

State-of-the-art

Electric field – TCAD simulated
H35DEMO (0.35 µm HV-CMOS ams)
1 kΩ·cm
100 µm
120 V Meng CERN-THESIS-2018-153



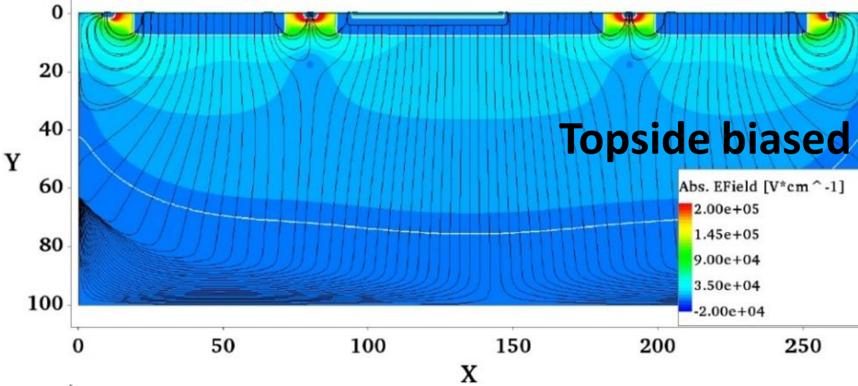
Depleted depth – Measured
Depletion voltage 30 V @ 5e14 n_{eq}/cm^2
Franks NIMA 2021 164949

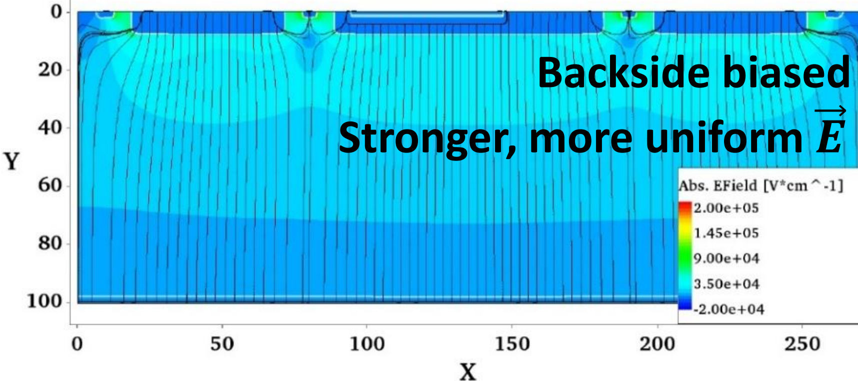


UK Research and Innovation
UNIVERSITY OF LIVERPOOL

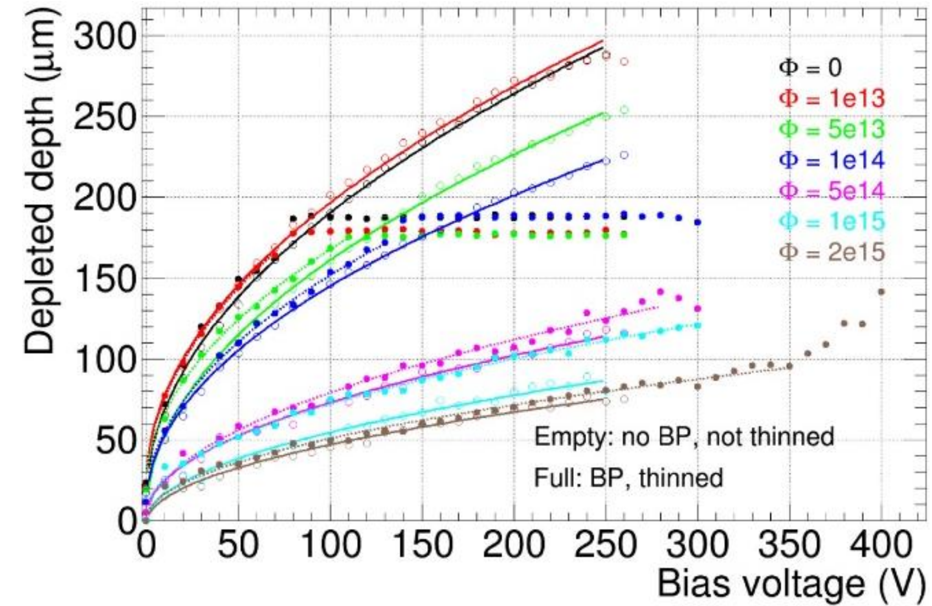
State-of-the-art

Electric field – <u>TCAD simulated</u>
H35DEMO (0.35 µm HV-CMOS ams)
1 kΩ·cm
100 µm
120 V [Meng CERN-THESIS-2018-153]

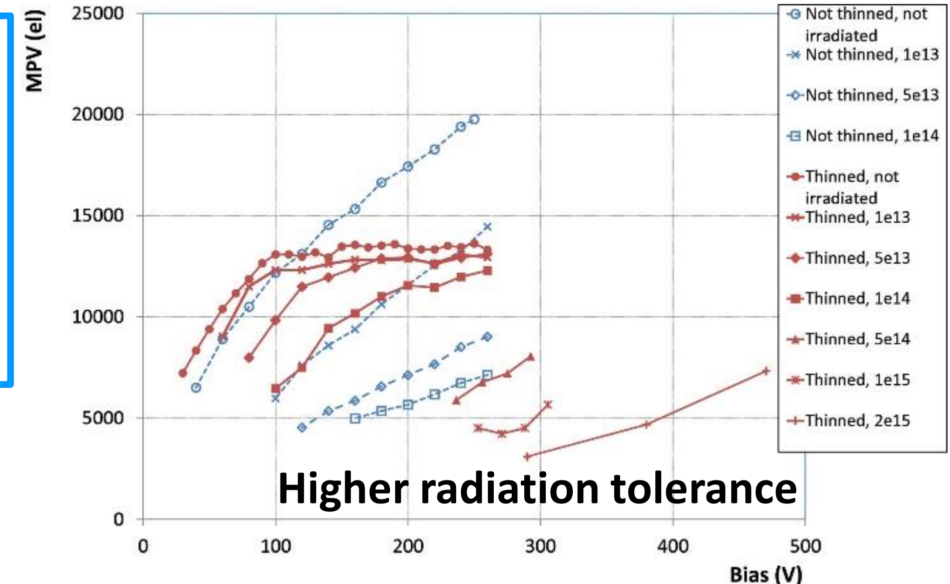




Depleted depth – <u>Measured</u>
150 nm HV-CMOS LFoundry
HR (3 kΩ·cm)
Backside vs topside biased
200 µm vs full thickness
[Mandic arXiv:1801.03671v2 2018]

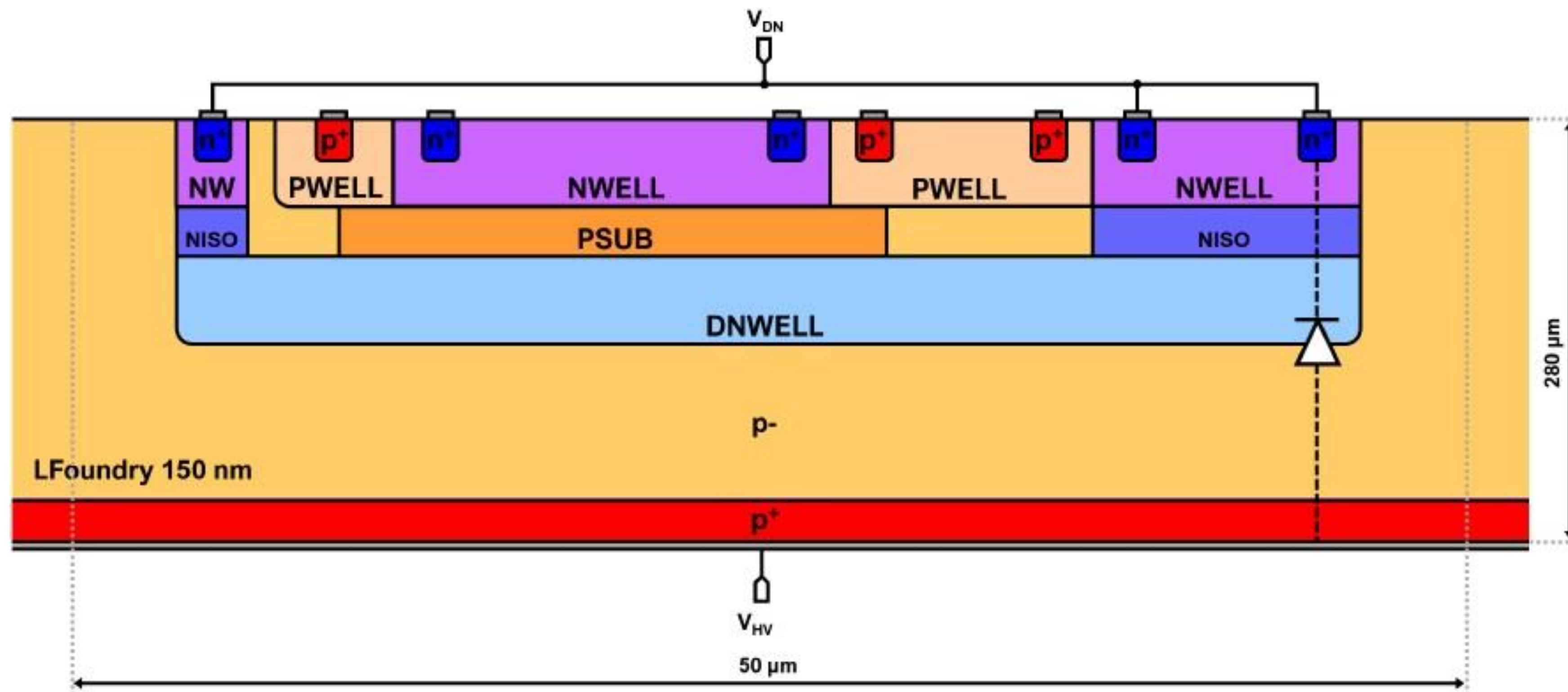


Collected charge – <u>Measured</u>
150 nm HV-CMOS LFoundry
HR (3 kΩ·cm)
Backside vs topside biased
200 µm vs full thickness
[Mandic arXiv:1801.03671v2 2018]



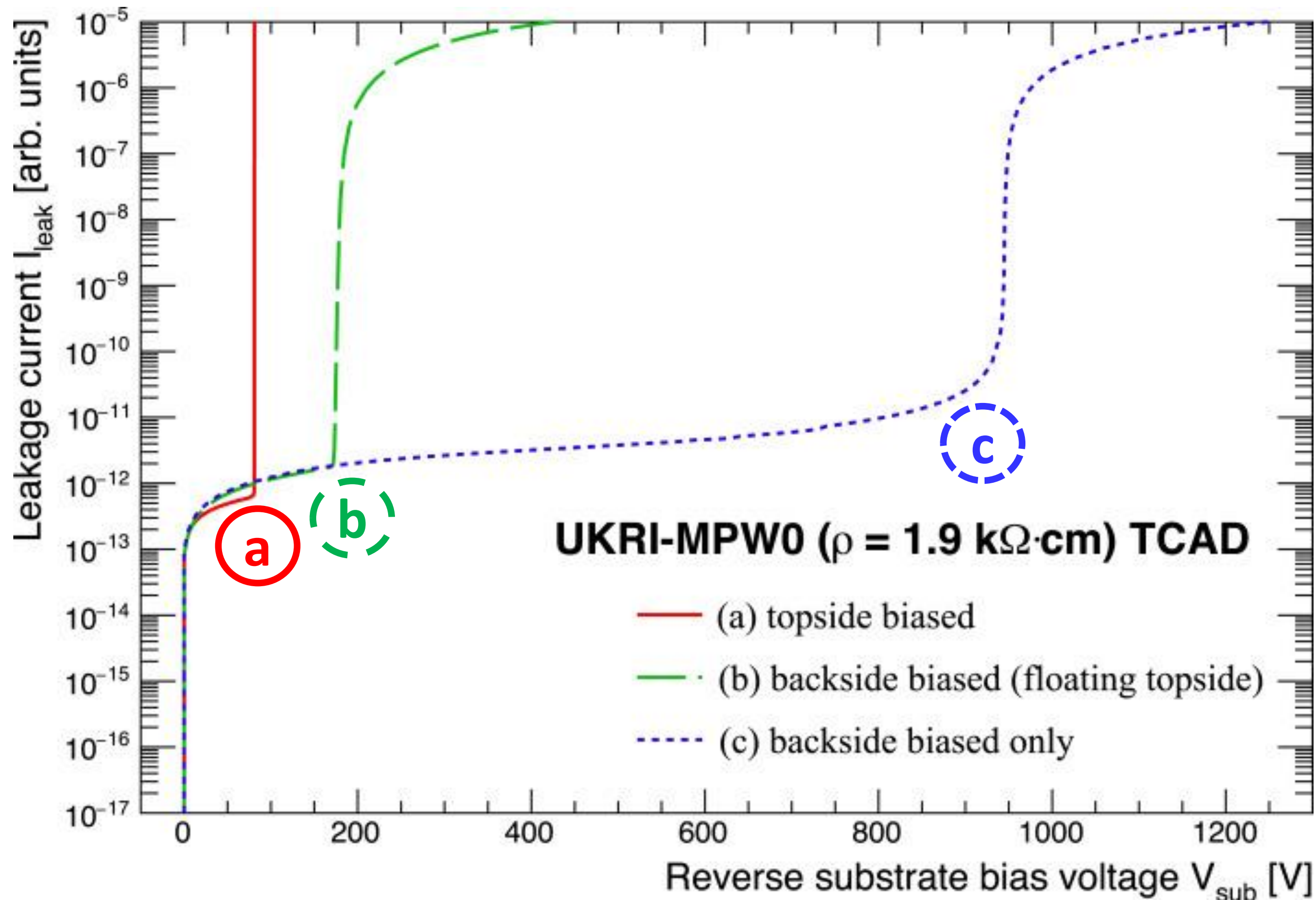
Idea

- **150 nm HV-CMOS LFoundry – New cross-section**
  – P-substrate/DNWELL sensing junction
  – Backside p-type contacts only to bias the p-substrate to HV
  – Pixel readout electronics embedded inside DNWELL



UK Research and Innovation
UNIVERSITY OF LIVERPOOL

Simulated pixel I-V



TCAD simulations	
Scenario	V_BD [V]
a ———	80
b – – –	180
c ------	900

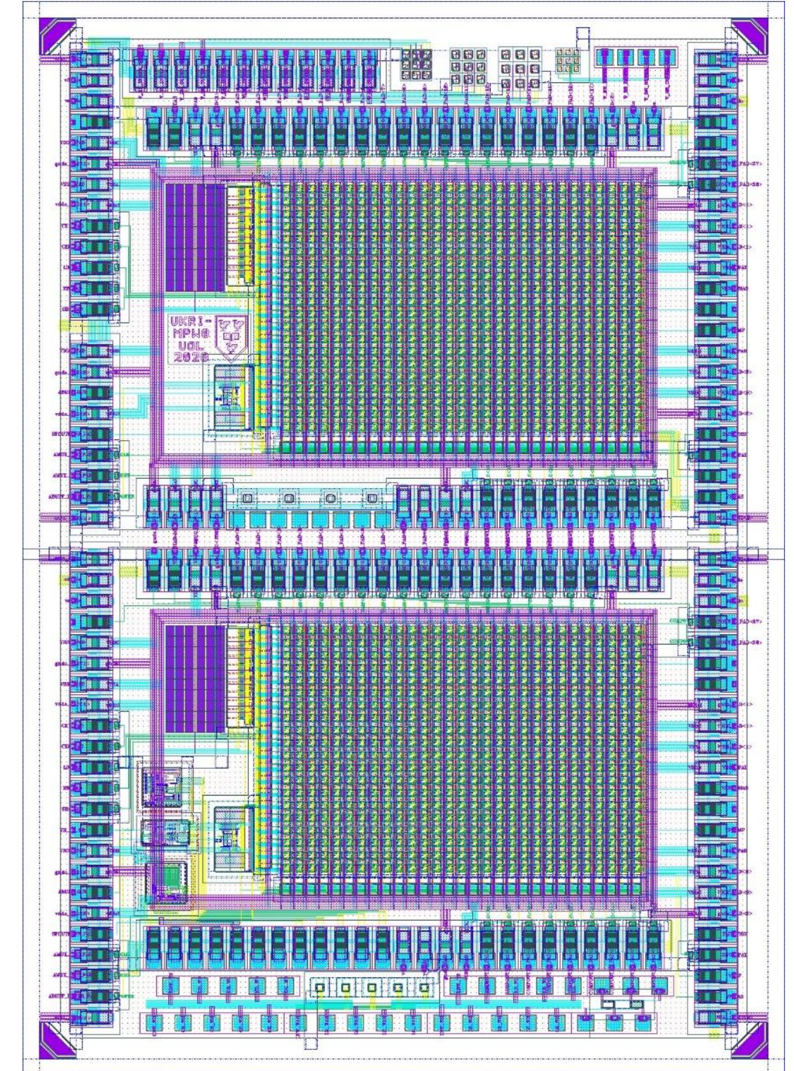
State-of-the-art	
HV-CMOS pixel chip	V_BD [V]
RD50-MPW3 – Matrix ref RD50-MPW3 – Test ref	120 > 400 V
AstroPix ref	250
LF-MonoPix2 ref	460
RD50-MPW4	?

- By removing the topside p-type contacts entirely → V_BD can be increased significantly
- These simulations form the basis for the UKRI-MPW0 design (see CERN-THESIS-2022-144)

UK Research and Innovation
UNIVERSITY OF LIVERPOOL

UKRI-MPW0 – Chip overview

Technology process	150 nm HV-CMOS LFoundry
Substrate resistivity	1.9 kΩ·cm
Chip size	3.5 mm x 5 mm
Fabrication type	MultiProject Wafer (MPW)
Submission date	November 2020
Chip thickness	280 µm (TAIKO grinding*)
HV biasing	From the chip backside only



***TAIKO grinding (more info here)**

- Leaves ring of silicon around the outer edge of the wafer
- Inner area can be made very thin (100 µm)
- Ring is removed prior to dicing and assembly
- 4000 mesh
- Compatibility with backside processing
- Backside plasma etching for a less rough surface less and to etch the potential defects

UK Research and Innovation
UNIVERSITY OF LIVERPOOL

UKRI-MPW0 – Backside processing

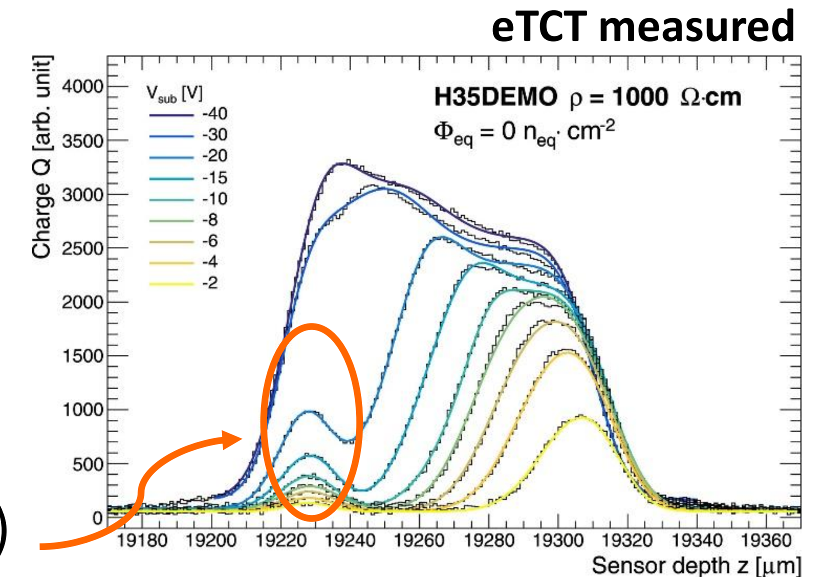
- **Two alternative methods investigated**

1) **Beamline Implantation + Rapid Thermal Annealing (BI + RTA)**
   - Annealed at 450°C
     - Too low to properly activate all the implanted boron
     - High enough to potentially damage the MOS transistors
   - Backside peak observed in eTCT measurements (H35DEMO)

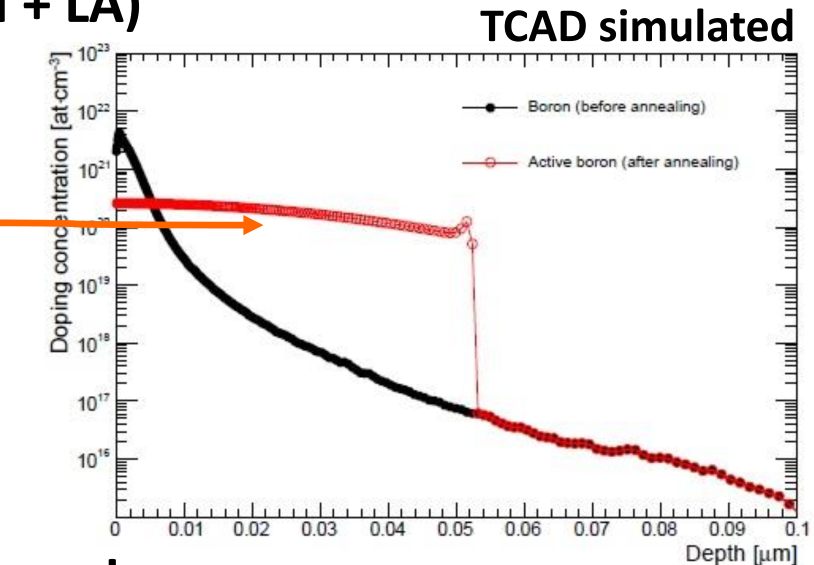
2) **Plasma Ion Immersion Implantation + UV Laser Annealing (PIII + LA)**
   - Localised annealing
     - Annealing T can be higher
     - All the implanted boron can be properly activated
     - No damage to the MOS transistors
   - Shallow implant profile
     - Keeps all dopants and defects into annealed region
   - Advantageous over BI + RTA

- **Done by Ion Beam Services (IBS) on full wafers loaned by the foundry**

eTCT measured



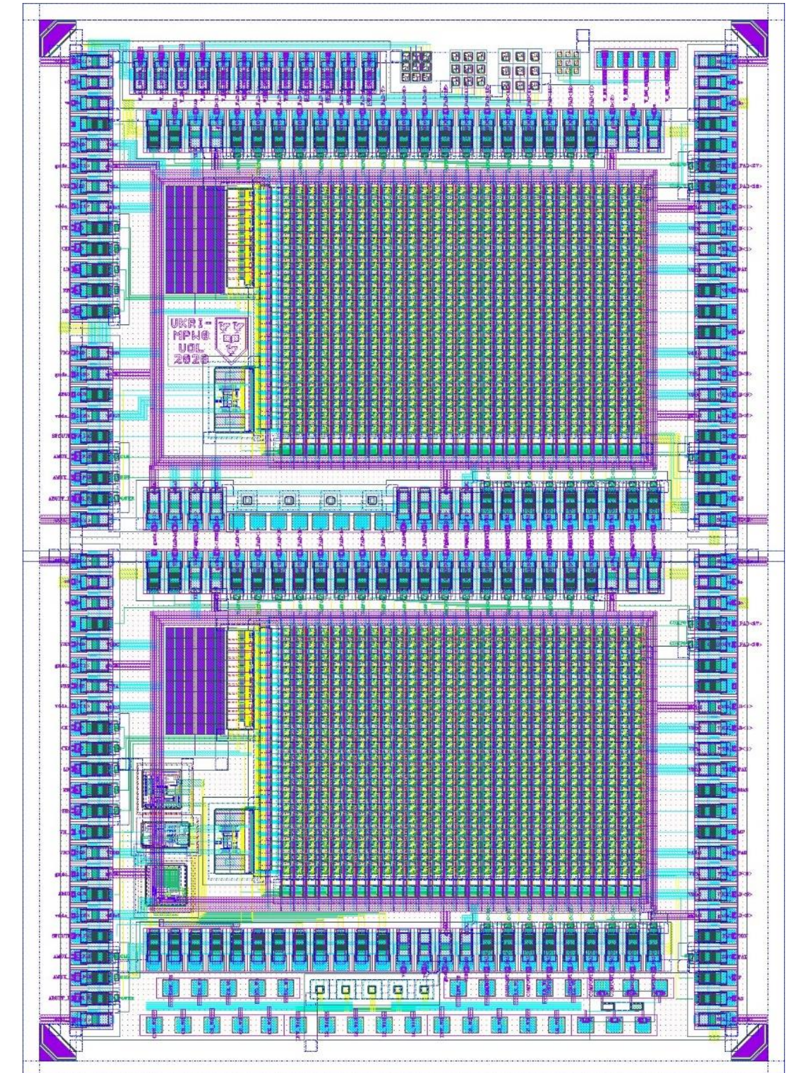
TCAD simulated



UK Research and Innovation
UNIVERSITY OF LIVERPOOL

UKRI-MPW0 – Chip overview

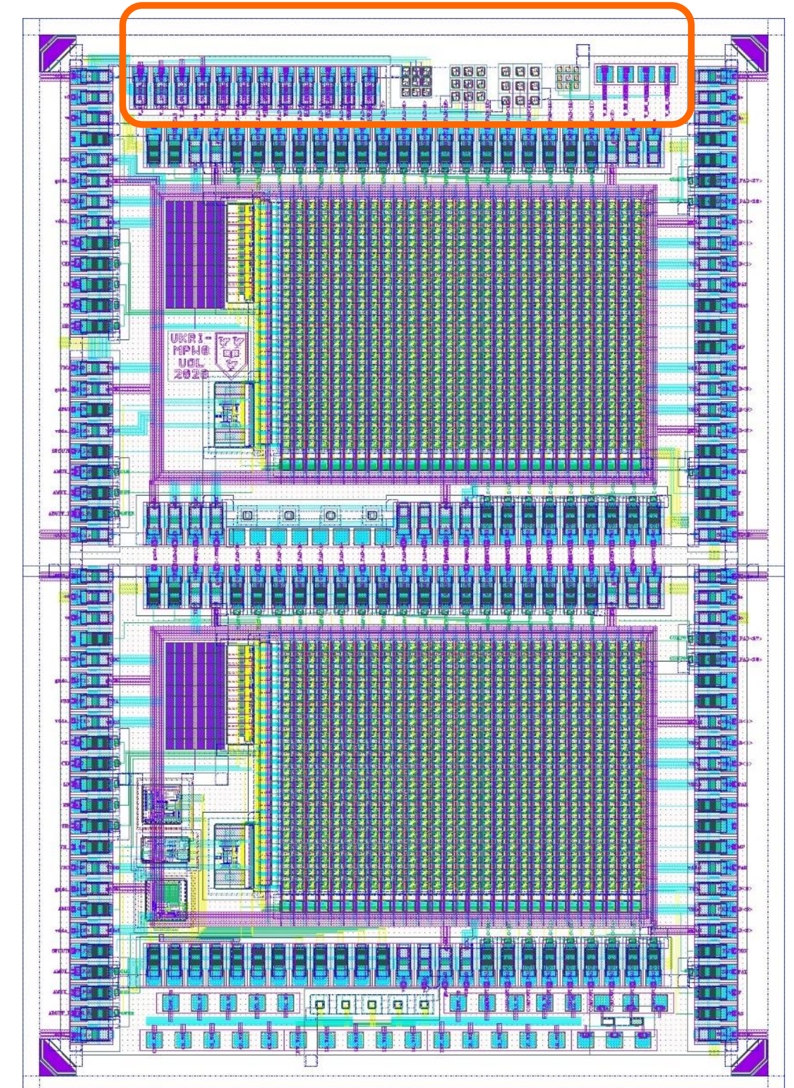
2 active pixel matrices	• With linear transistors only • With linear and ELT transistors • With 20 x 29 pixels per matrix
3 pixel flavours	• Continuous reset • Switched reset • Modulated feedback
Test structures	• With passive pixels for eTCT (RD50-MPWx style) • With linear and ELT transistors
Pixel size	60 µm x 60 µm



UK Research and Innovation UNIVERSITY OF LIVERPOOL

UKRI-MPW0 – Chip overview

2 active pixel matrices	• With linear transistors only • With linear and ELT transistors • With 20 x 29 pixels per matrix
3 pixel flavours	• Continuous reset • Switched reset • Modulated feedback
Test structures	• With passive pixels for eTCT (RD50-MPWx style) • With linear and ELT transistors
Pixel size	60 µm x 60 µm

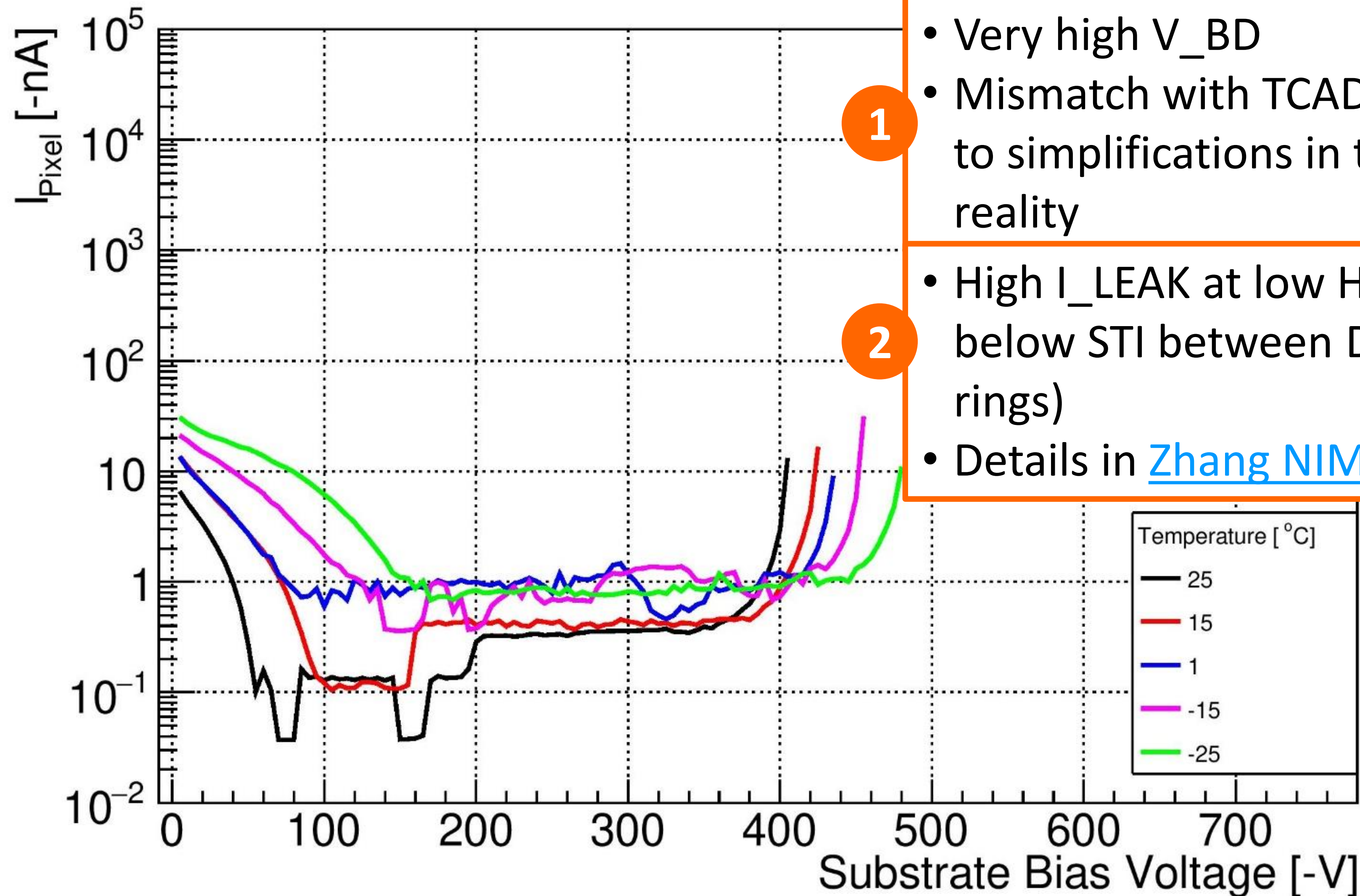


UK Research and Innovation UNIVERSITY OF LIVERPOOL

Measured pixel I-V – PIII + LA, before irradiation

1
- Very high V_BD
- Mismatch with TCAD simulations due to simplifications in the simulations vs reality

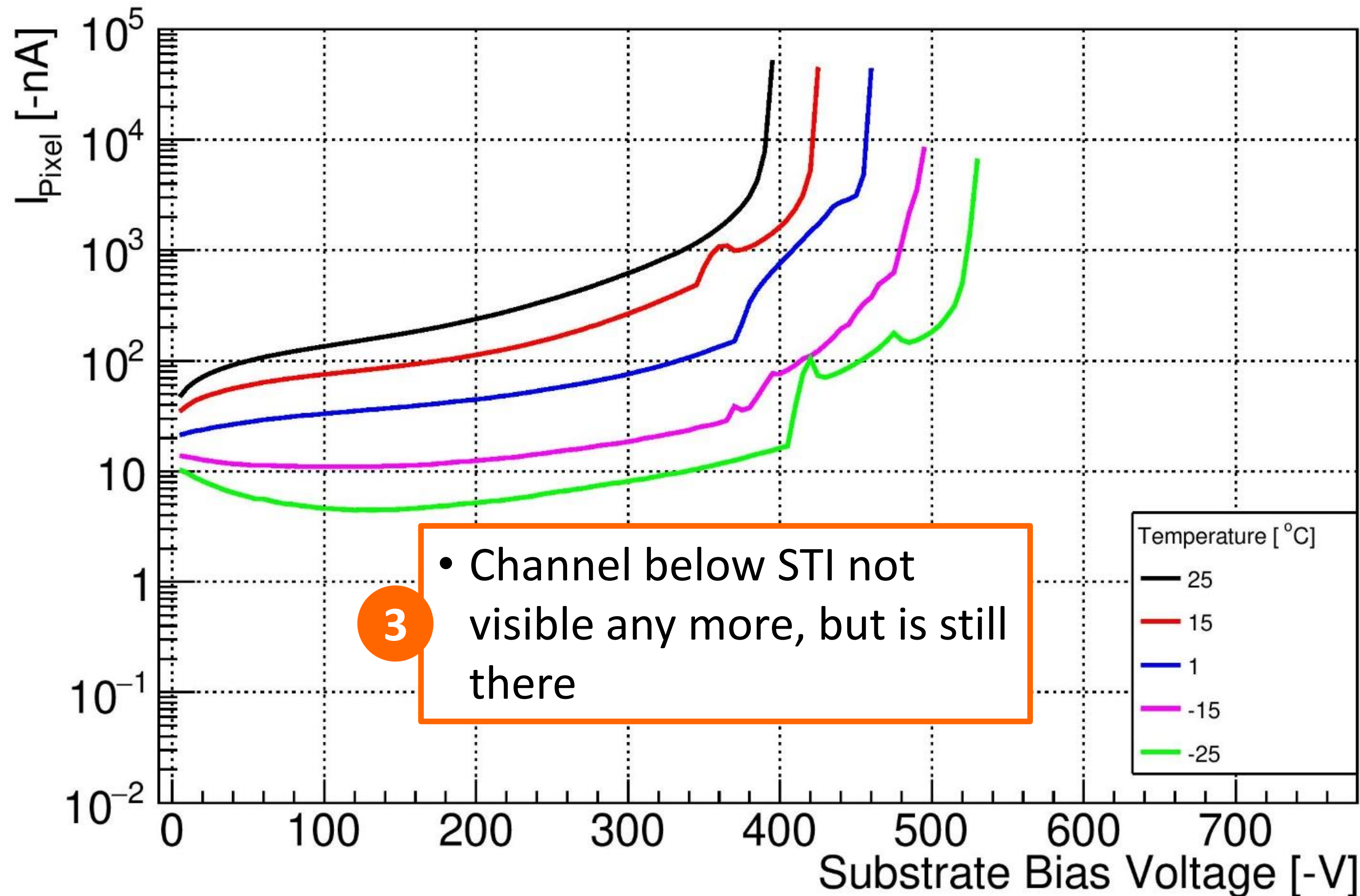
2
- High I_LEAK at low HV due to channel below STI between DNWELLs (pixels, rings)
- Details in [Zhang NIMA 2022 167214]



- Measurement at several T
- Cooling setup details [here]

UK Research and Innovation
UNIVERSITY OF LIVERPOOL

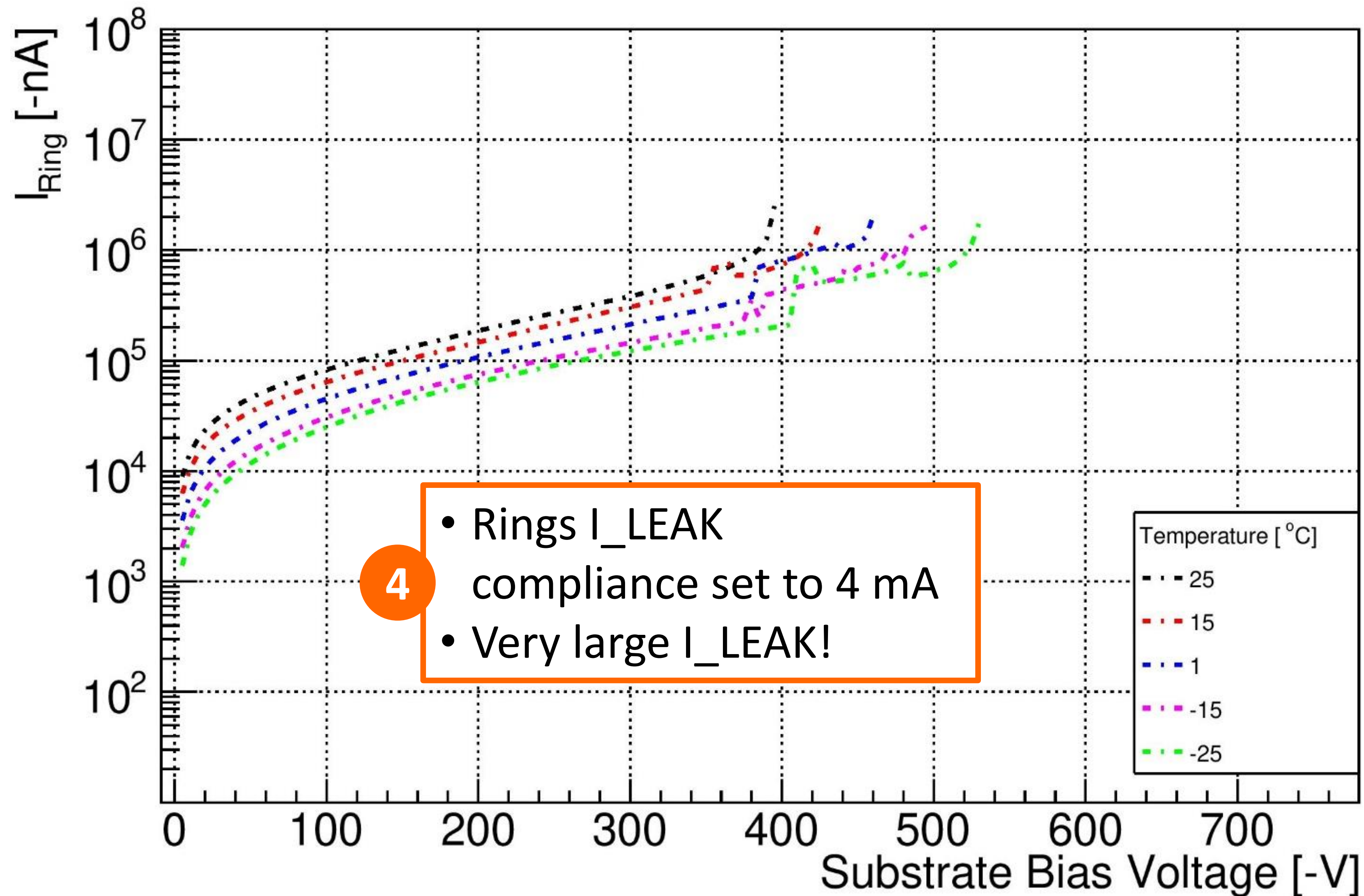
Measured pixel I-V – PIII + LA, neutron 3e13 n_{eq}/cm^2



- Measurement at several T
- Cooling setup details here

UK Research and Innovation
UNIVERSITY OF LIVERPOOL

Measured chip rings I-V – PIII + LA, neutron 3e13 n_{eq}/cm^2



- Measurement at several T
- Cooling setup details here

UK Research and Innovation
UNIVERSITY OF LIVERPOOL

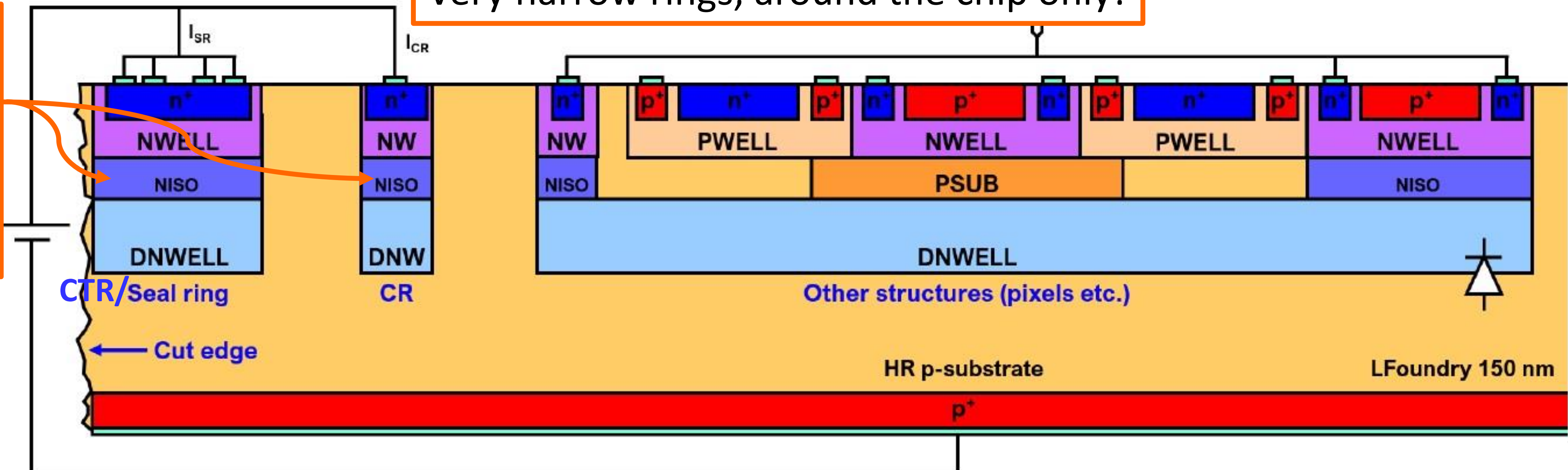
UKRI-MPW0 – Chip rings

Noschis NIMA 2006 4144

- **Current Terminating Ring (CTR) that surrounds the whole chip**
  - Collects the current generated at the cut edge surface
  - Used also as the chip seal ring to protect the design during the dicing process
- **A Clean-up Ring (CR) between the CTR and the sensor**
  - Cleans up the remaining current that cannot be collected by the CTR due to diffusion into the bulk

Very narrow rings, around the chip only!

Made of n-type layers only!

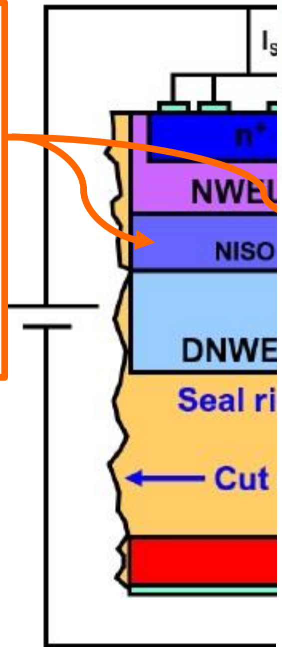


UK Research and Innovation
UNIVERSITY OF LIVERPOOL

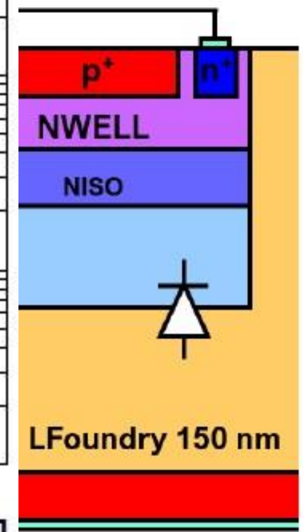
UKRI-MPW0 – Chip rings

- **Current Terr**
  - Collects
  - Used als … s
- **A Clean-up I**
  - Cleans u … diffusion into the bulk

Made of n-type layers only!

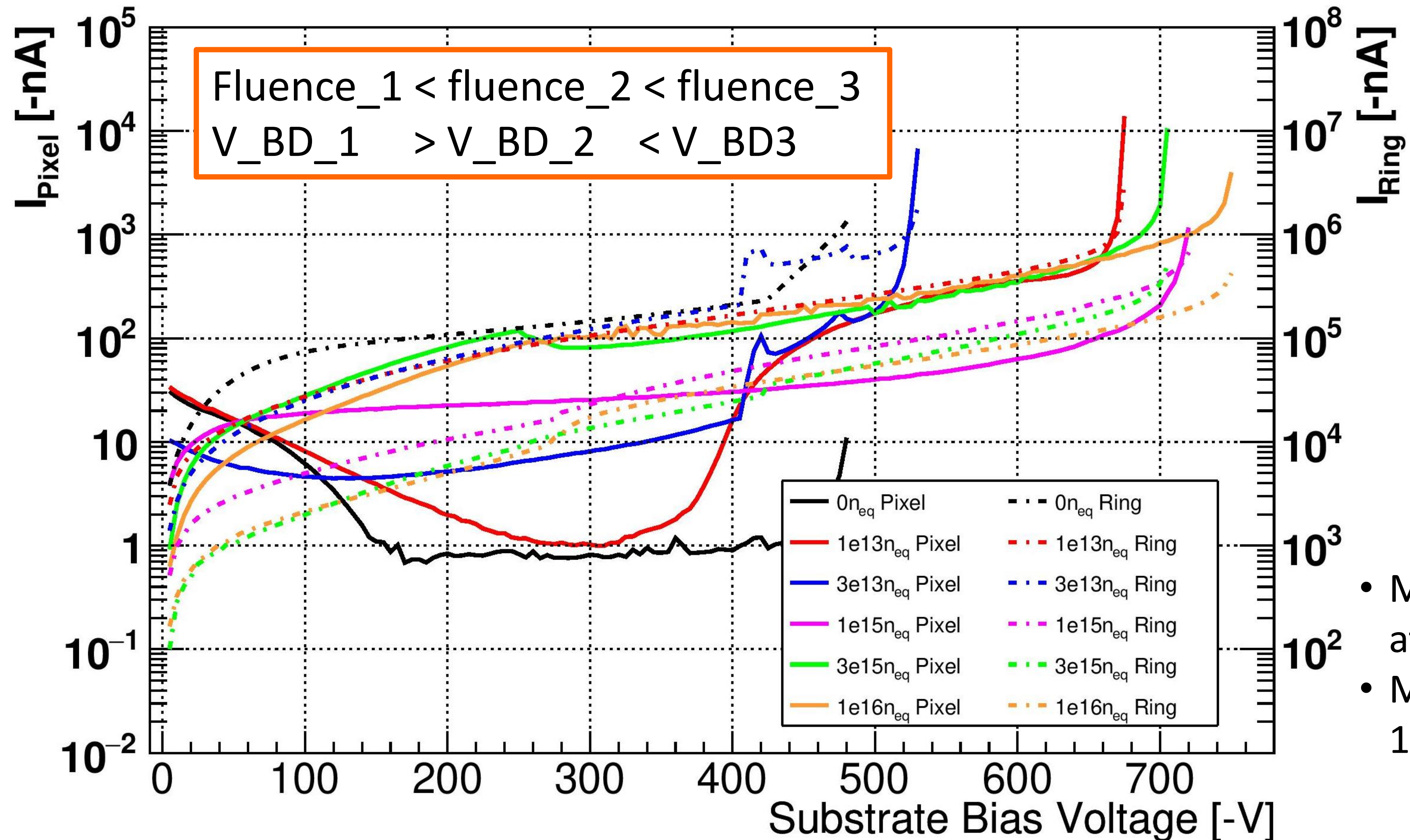


10^{-8}
10^{-9}
10^{-10}
10^{-11}
10^{-12}
10^{-13}
Leakage current I_{leak} [A·µm^{-1}]
I_{sub}
I_{CTR}
I_{CR}
I_{pixel}
UKRI-MPW0 (ρ = 1900 Ω·cm) TCAD
0
500
1000
1500
2000
Reverse substrate bias voltage V_{sub} [V]



UK Research and Innovation
UNIVERSITY OF LIVERPOOL

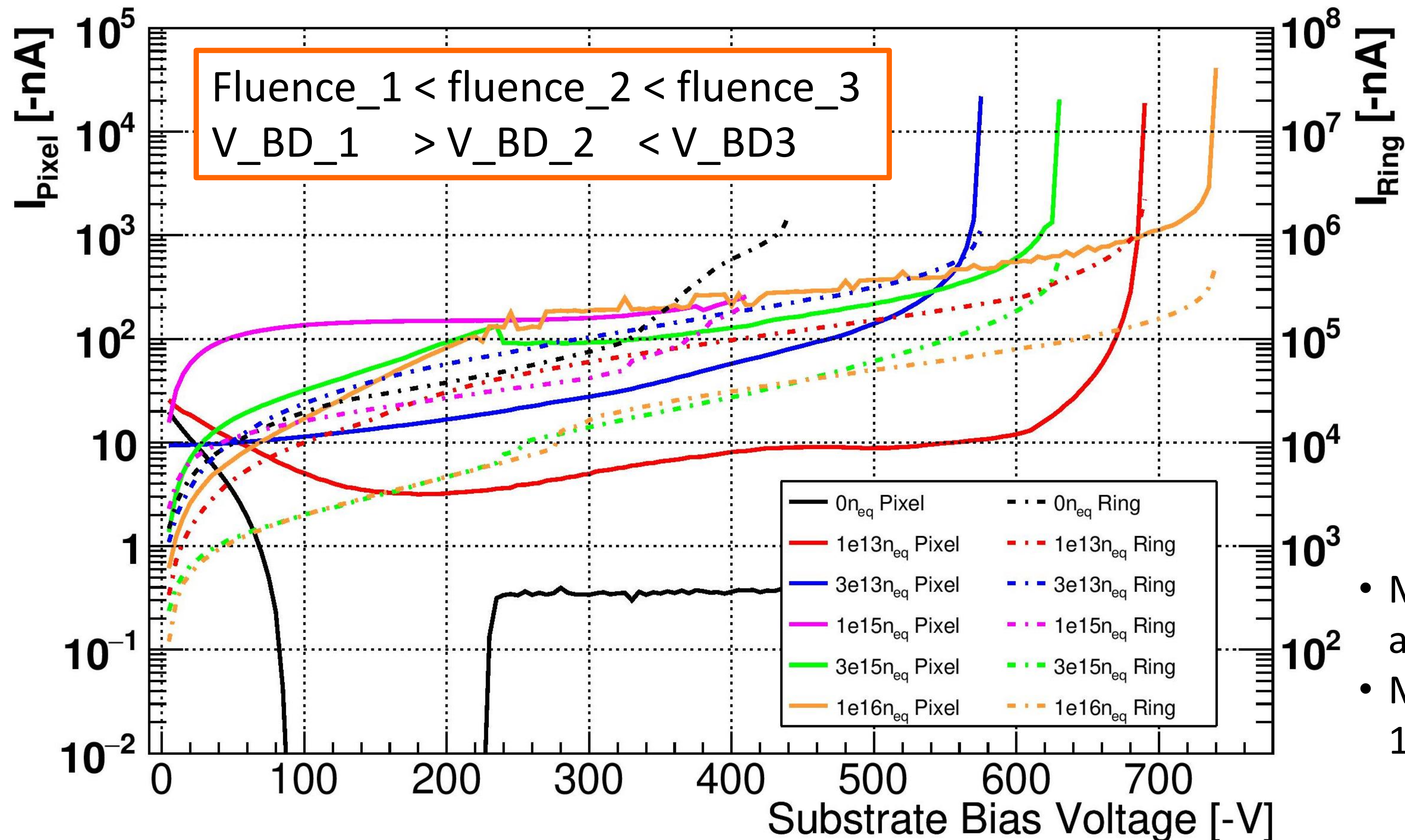
Measured pixel + chip rings I-Vs – PIII + LA, all fluence



- Measurement at -25°C
- Max. fluence is 1e16 n_{eq}/cm^2

UKRI UK Research and Innovation
UNIVERSITY OF LIVERPOOL

Measured pixel + chip rings I-Vs – BI + RTA, all fluence

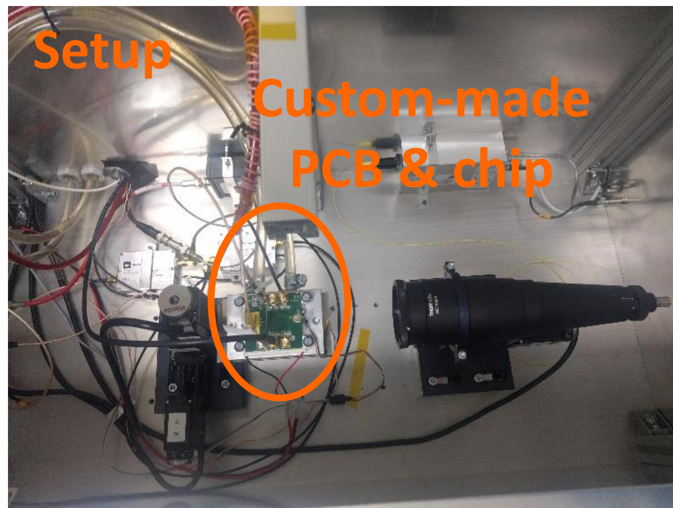


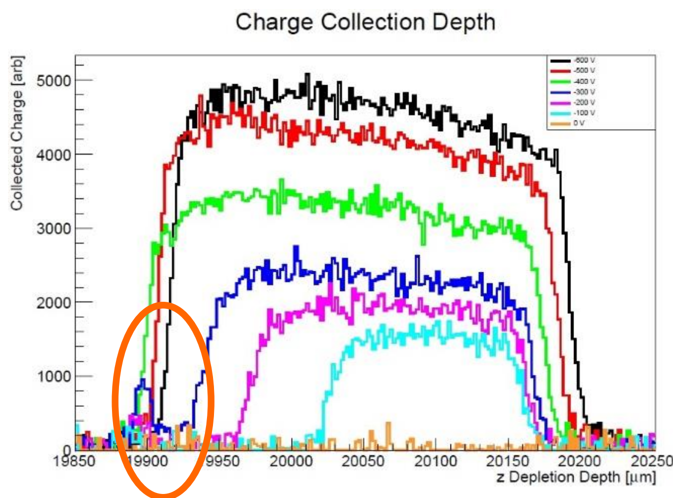
- Measurement at -25°C
- Max. fluence is 1e16 n_{eq}/cm^2

UK Research and Innovation
UNIVERSITY OF LIVERPOOL

Measured eTCT – BI + RTA

Wade IWORID 2022





Backside peak

Depletion Depth W_D [μm]

Φ_{eq} [1 MeV n_{eq} cm^{-2}]
- 0
- $1 \cdot 10^{13}$
- $1 \cdot 10^{14}$
- $1 \cdot 10^{15}$
- $3 \cdot 10^{15}$
- $1 \cdot 10^{16}$

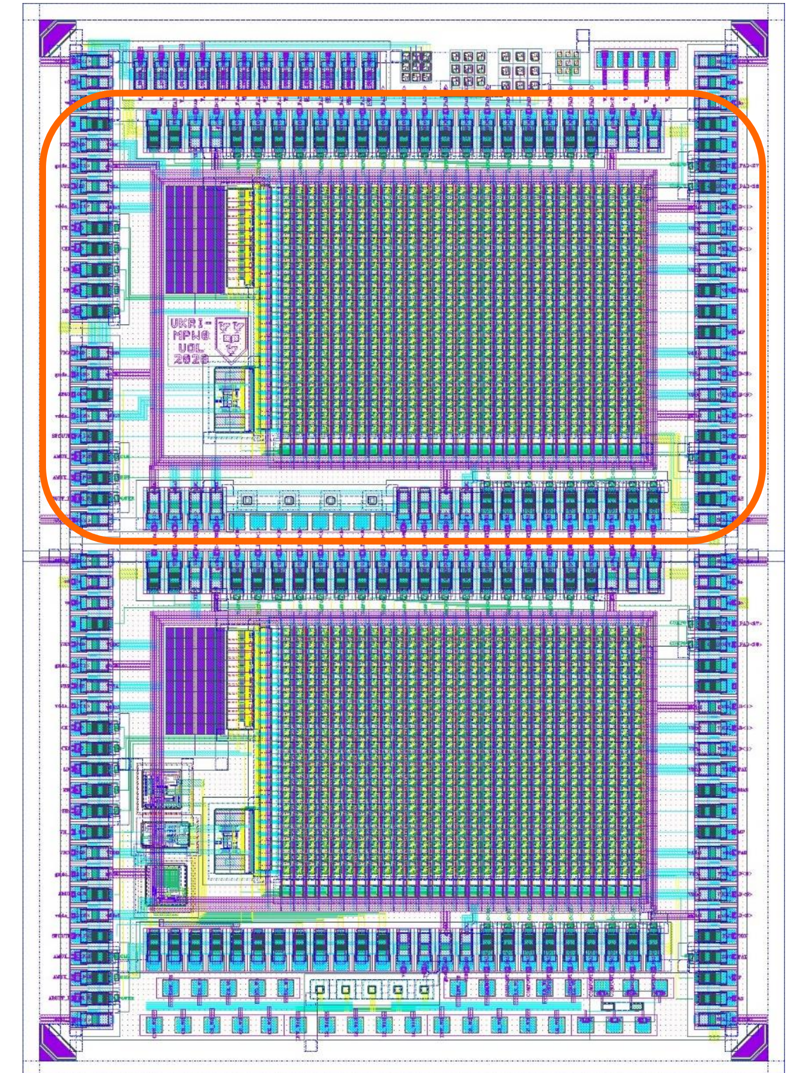
Nominal Reverse Bias Voltage V_{bias} [V]

- Depletion voltage 300 V @ 1e14 n_{eq}/cm^2 (280 μm)
- > 50μm depleted depth @ 1e16 n_{eq}/cm^2
- Irradiated PIII + LA samples currently being evaluated

UK Research and Innovation
UNIVERSITY OF LIVERPOOL

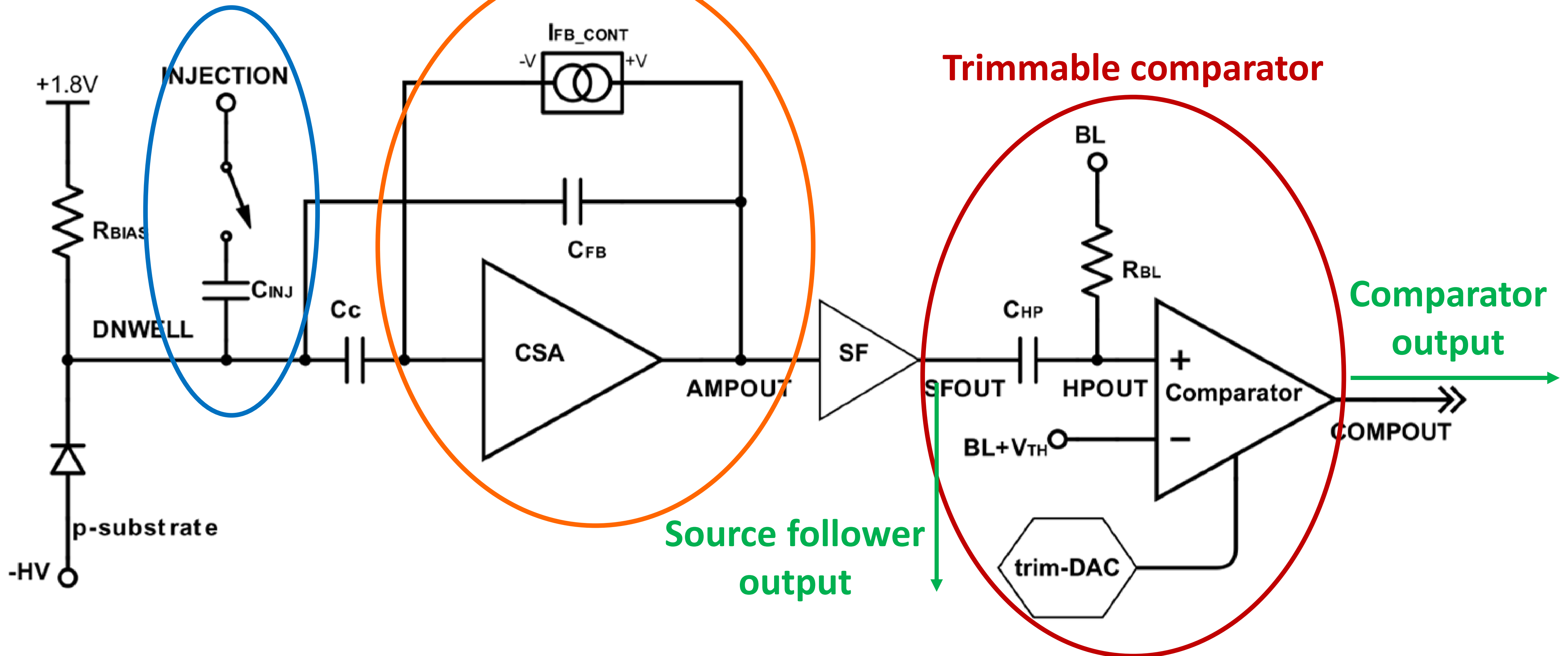
UKRI-MPW0 – Chip overview

2 active pixel matrices	• With linear transistors only • With linear and ELT transistors • With 20 x 29 pixels per matrix
3 pixel flavours	• Continuous reset • Switched reset • Modulated feedback
Test structures	• With passive pixels for eTCT (RD50-MPWx style) • With linear and ELT transistors
Pixel size	60 µm x 60 µm



UK Research and Innovation
UNIVERSITY OF LIVERPOOL

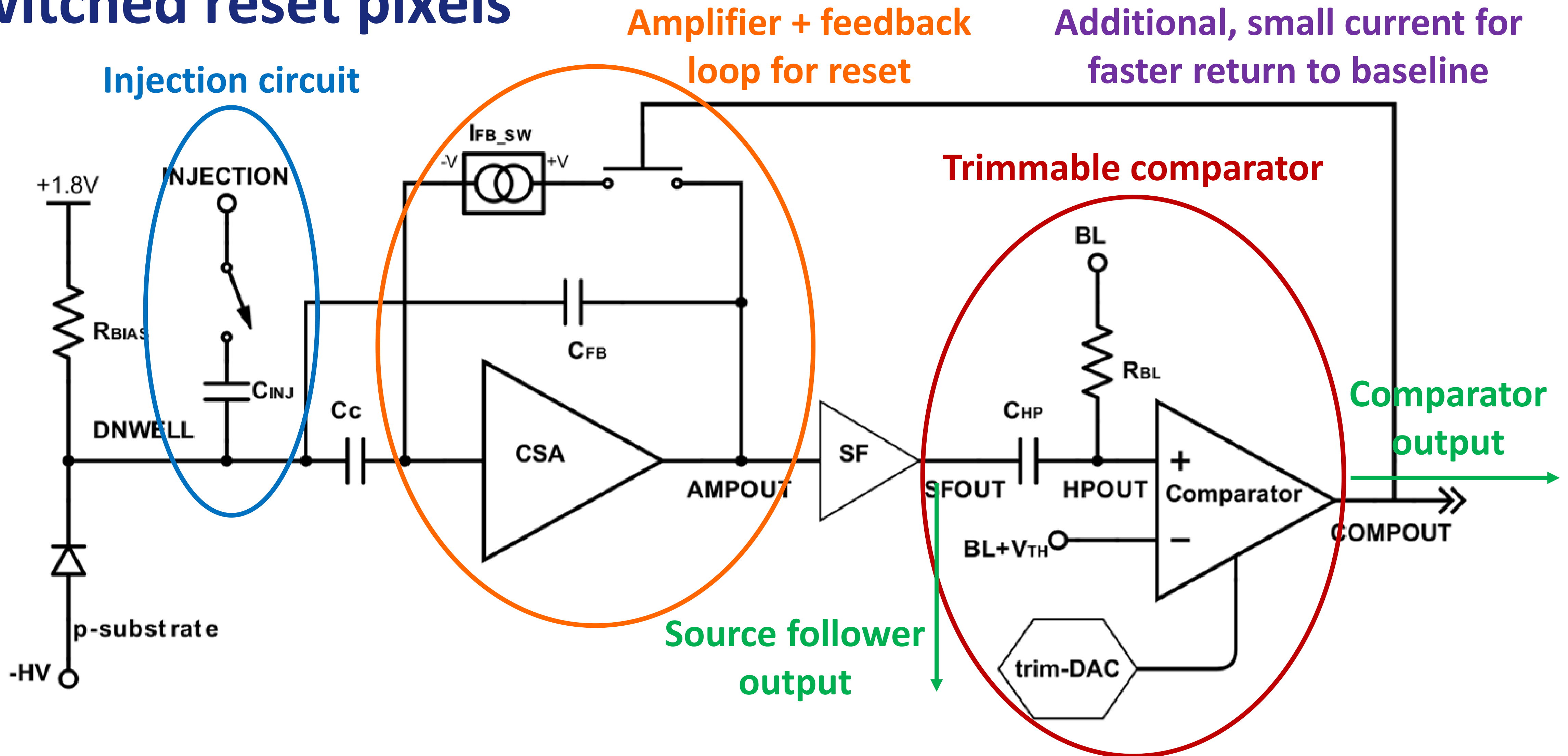
Continuous reset pixels



- Based on the well understood RD50-MPW2 design [Zhang PoS(TWEPP2019)045]

UK Research and Innovation
UNIVERSITY OF LIVERPOOL

Switched reset pixels

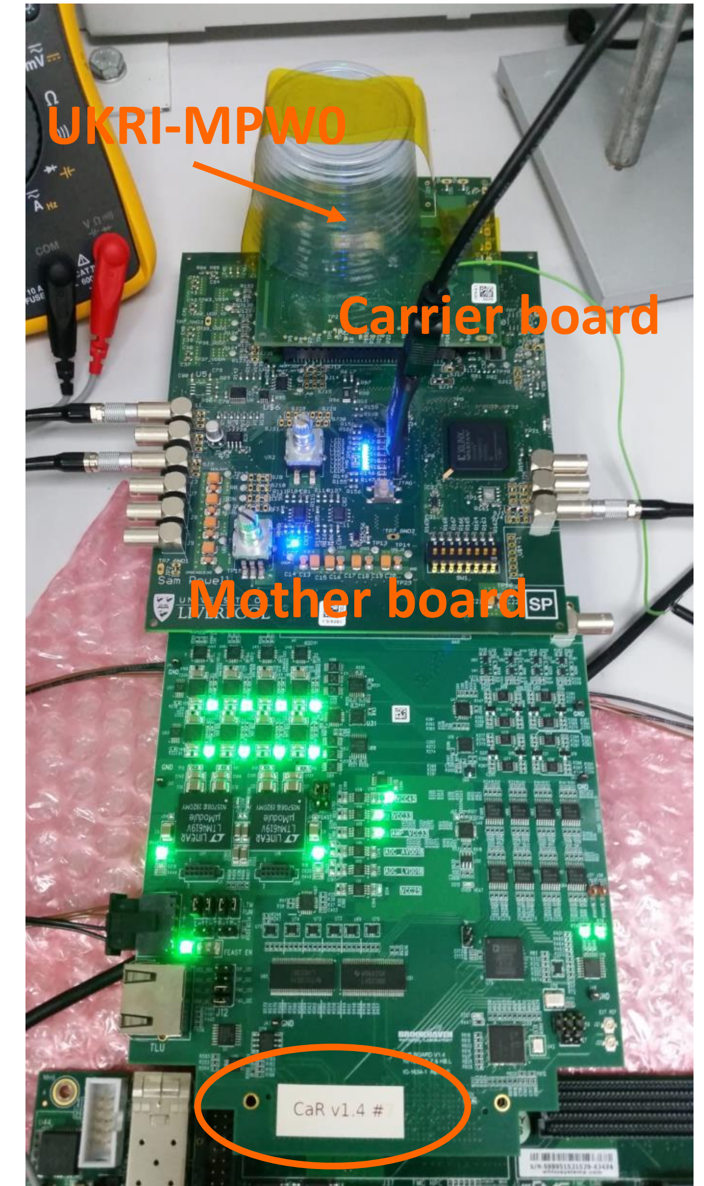


- Based on the well understood RD50-MPW2 design Zhang PoS(TWEPP2019)045

UK Research and Innovation
UNIVERSITY OF LIVERPOOL

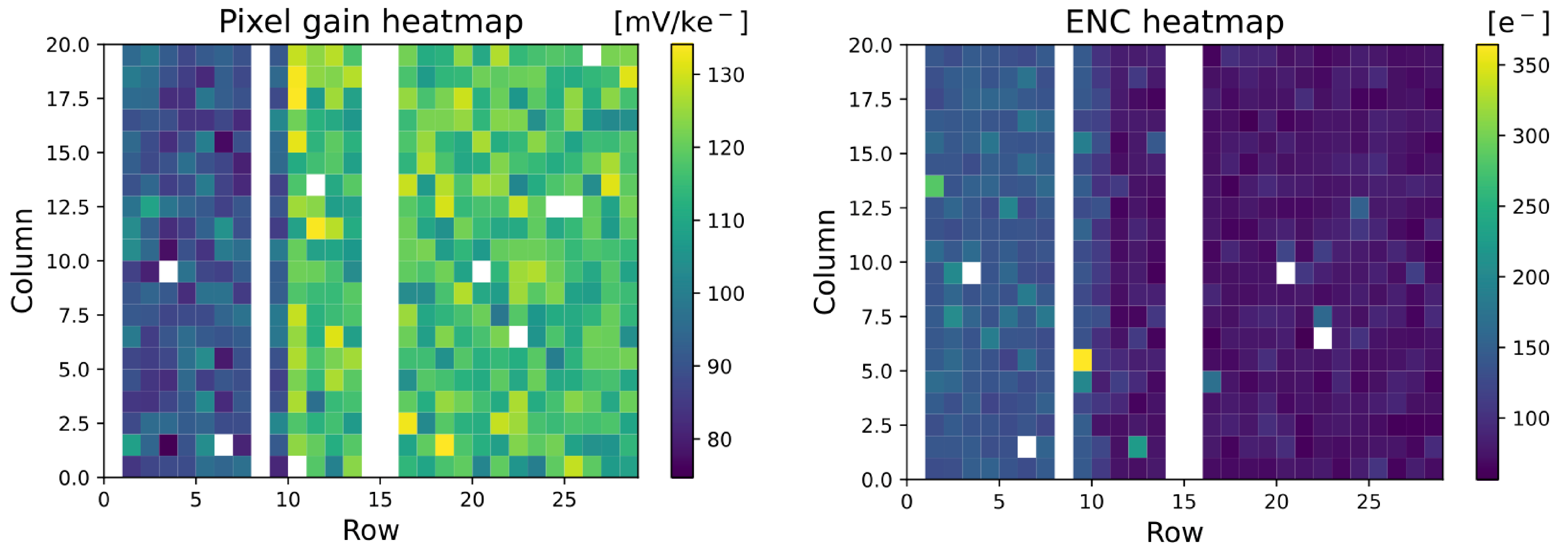
UKRI-MPW0 – DAQ

- **Based on Caribou**
  - UKRI-MPW0 chip carrier board
  - UKRI-MPW0 mother board
    - Analogue pixels have SFOUT & COMPOUT readout only
    - This boards incorporates digital readout
    - Measurements of pixel address and time-stamp are possible
  - CaR board
  - SoC (ZC706)



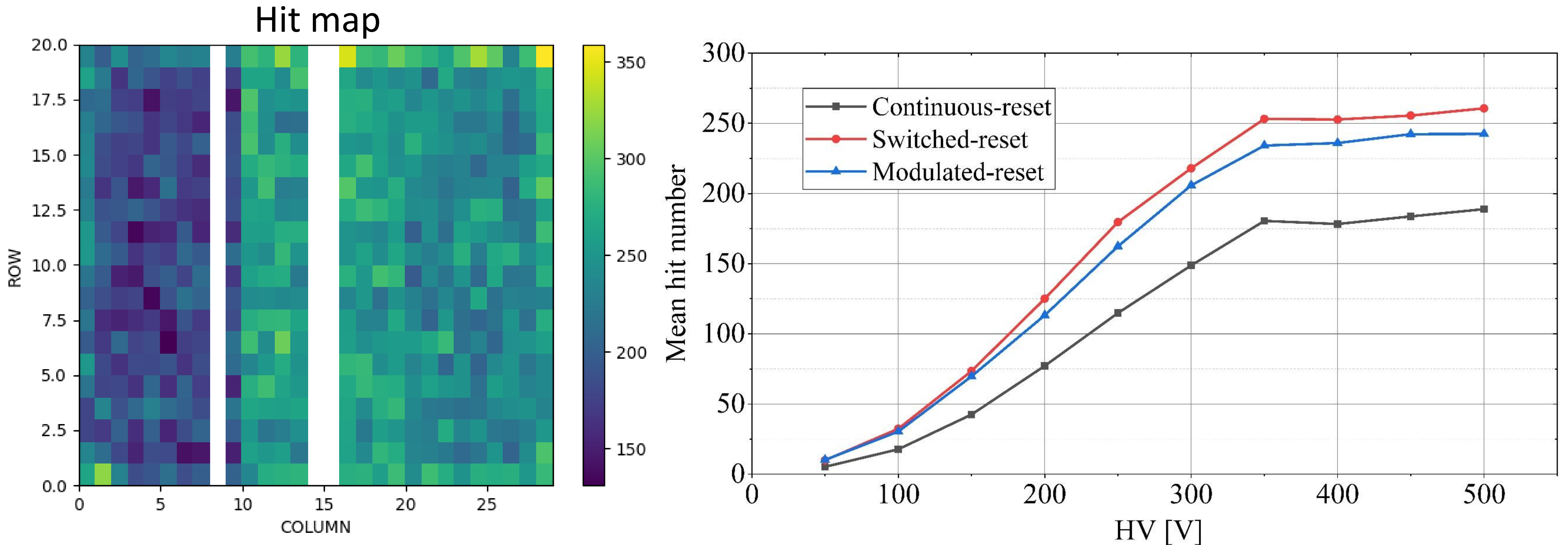
UK Research and Innovation
UNIVERSITY OF LIVERPOOL

Active matrix – BI + RTA, before irradiation



- The three different pixel flavours are visible (please ignore three dead columns in the FPGA)
- Measured (using test pulses) and simulated values agree
  - Gain expected from design → 65 µV/e⁻ (continuous), 80 µV/e⁻ (switched)
  - Noise expected from design → 150 e⁻ (continuous), 100 e⁻ (switched)

Active matrix – BI + RTA, before irradiation

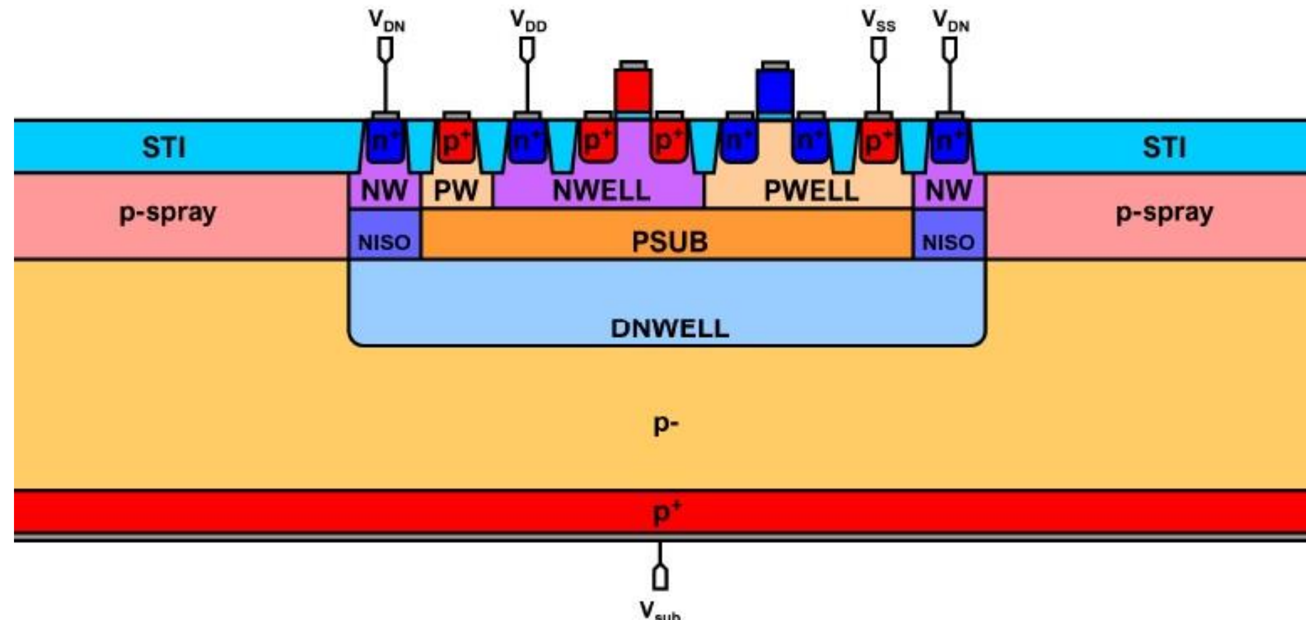


- HV = 500 V, V_TH = 1050 mV
- Sr90 source (old and weak)
- Shutter window = 20 s
- Switched reset pixels have better sensitivity (as in RD50-MPW2)

UK Research and Innovation
UNIVERSITY OF LIVERPOOL

Current plans to improve sensor design

- To improve pixel I_LEAK, while keeping a high V_BD
  - Prevent channel below STI & achieve isolation between n-type layers
  - Adding a low or moderate-doped and shallow p-type layer beneath the STI
    - Running TCAD simulations to understand dose, depth, and spacing
    - In conversations with the foundry
- To improve rings I_LEAK



UK Research and Innovation
UNIVERSITY OF LIVERPOOL

Conclusion and outlook

- UKRI-MPW0 is a proof-of-concept, backside biased only HV-CMOS pixel chip
- After 1e16 n_{eq}/cm^2 neutron irradiation
  - V_BD > 700 V
  - Depletion depth > 50 μm
- We are doing studies to improve the sensor leakage current
- Unfortunately we don’t have conclusive results yet on the what type of backside processing works better
- We have evaluated the matrix of active pixels before irradiation, and we’ll measure irradiated samples next