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Guard Ring Optimisation of Passive-CMOS pixel structures

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In high energy physics, the silicon pixel sensors manufactured in commercial CMOS chip fabrication lines have been proven to have good radiation hardness and spatial resolution. Along with the mature manufacturing techniques and the potential of large throughput provided by the foundries, the so-called “passive CMOS” sensor has become an interesting alternative to standard planer sensors.

High and predictable breakdown behaviour is a major design goal for sensors and the guard-ring structure is one factor to optimise. This is especially important for applications that require higher voltages.

We present the preliminary results of the measurements for the passive-CMOS guard ring test structures from the MPW3 submission. Results have revealed that the deep n-well adopted for the guard ring structure results in a more uniform potential distribution across the guard rings, as predicted by TCAD simulations. The sign of improved breakdown performance from the modified potential distribution of guard rings is revealed from the breakdown measurements.

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