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Science & Technology Facilities Council
Rutherford Appleton Laboratory

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Radiation damage investigation of epitaxial p-type Schottky diodes using TCAD simulation

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Outline

- Introduction
  - Motivation
  - Introduction of TCAD
  - Devices simulated with TCAD
  - Take the thin interface oxide layer into consideration

- Procedure of Simulation
  - Simulation of the device manufactory process
  - Simulation using SDEVICE

- Comparison between Measurement and Simulation

- Summary and Next

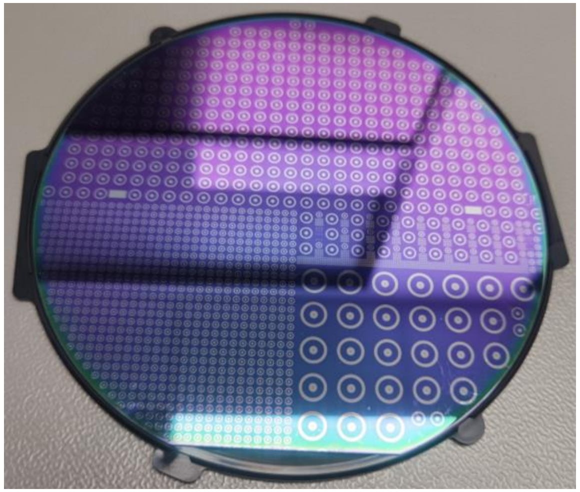
Introduction

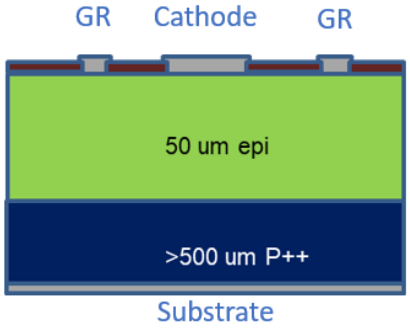
- Motivation
  - To investigate the radiation damage of epitaxial p-type silicon devices
  - Properties extracted from the IV and CV measurements to simulate
  - To summarize a radiation damage model

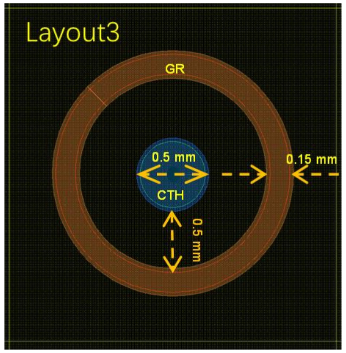
- Technology computer-aided design (TCAD)
  - Branch of electronic design automation that simulates the manufacturing and semiconductor device operation of semiconductors
  - Tools used
    - SPROCESS
      - To simulate the fabrication of devices
    - SDEVICE
      - To simulate the operation of devices under applied voltage

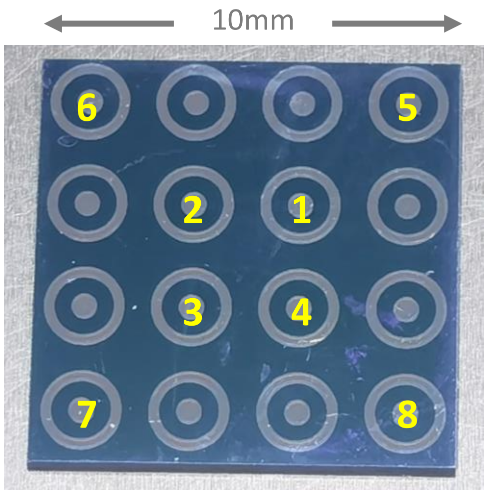
Introduction

- Devices simulated with TCAD
  - Epitaxial p-type Schottky diodes
    - Substrate
      - 5×10^{18} cm^{-3} Boron doping
      - > 500 µm thickness
    - P-type epitaxial layer
      - 10^{13} cm^{-3} Boron doping
      - 50 µm thickness
    - 10×10 mm diodes diced from the same wafer
      - 0.5mm cathode diameter
      - Non-irradiated
      - Neutron irradiated
        - 10^{12}, 10^{13}, 10^{14}, 10^{15}, 10^{16} 1MeV n_{eq}/cm^2



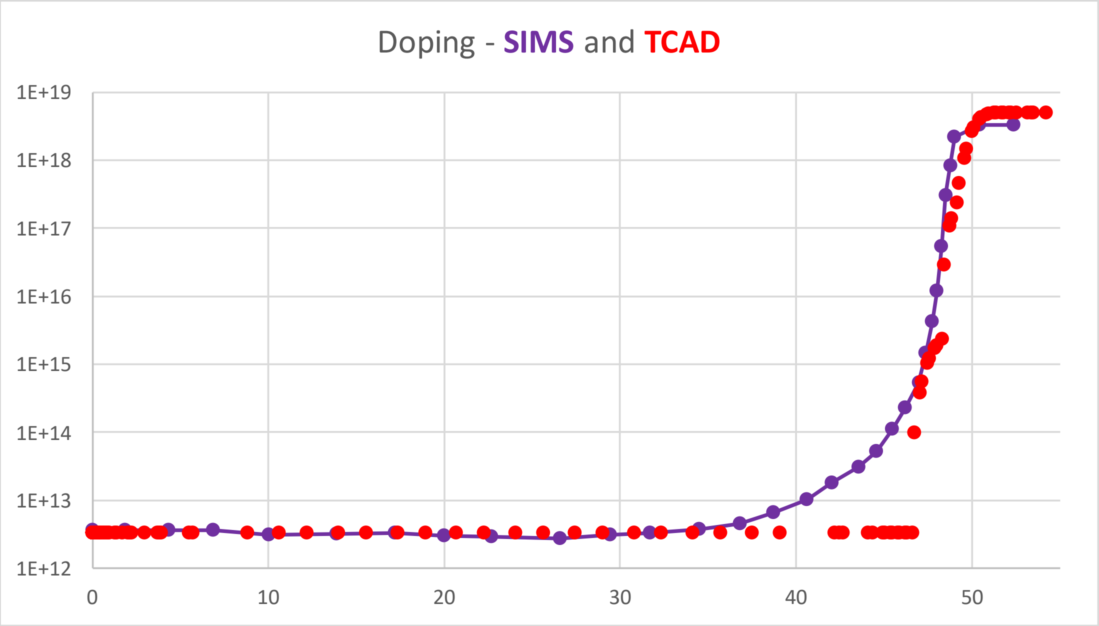






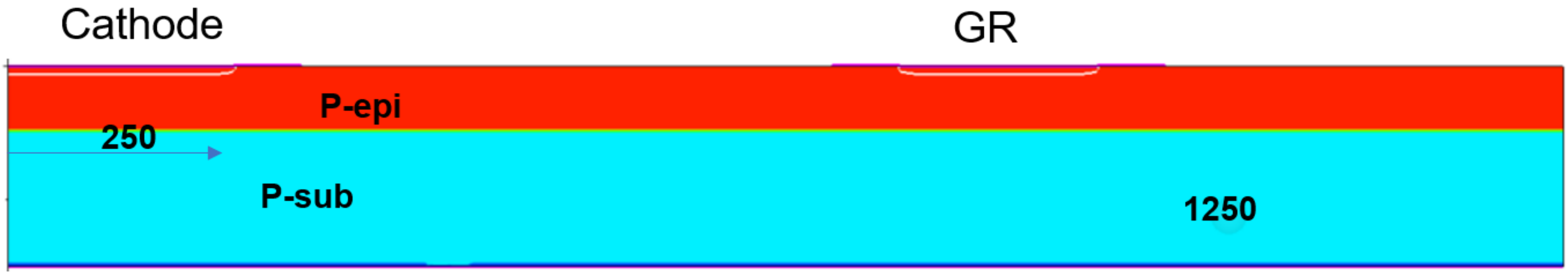
Introduction

- Devices simulated with TCAD
  - Differences of simulation
    - Doping in P-type epitaxial layer
      - Secondary Ion Mass Spectrometry (SIMS) from wafer supplier
        - 3.3×10^{12} cm^{-3}



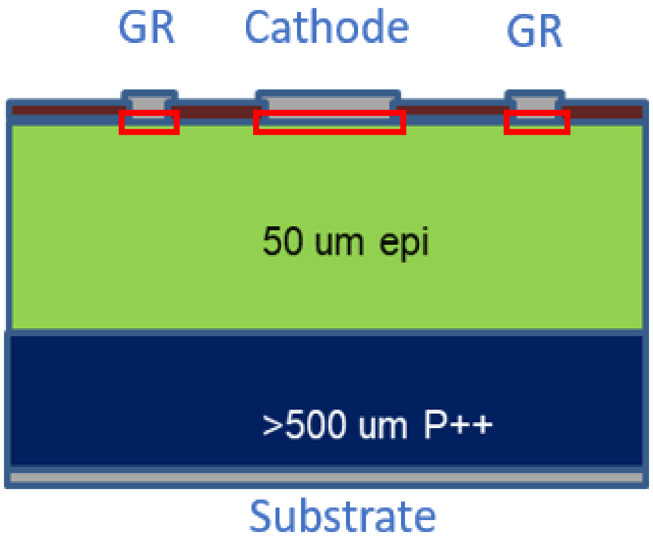
Introduction

- Devices simulated with TCAD
  - Differences of simulation
    - Structure
      - Substrate thickness
        - >500µm → 100µm
      - Only half device 0.5mm cathode is simulated, but Cylindrical symmetry is exploited to get an equivalent 3D simulation



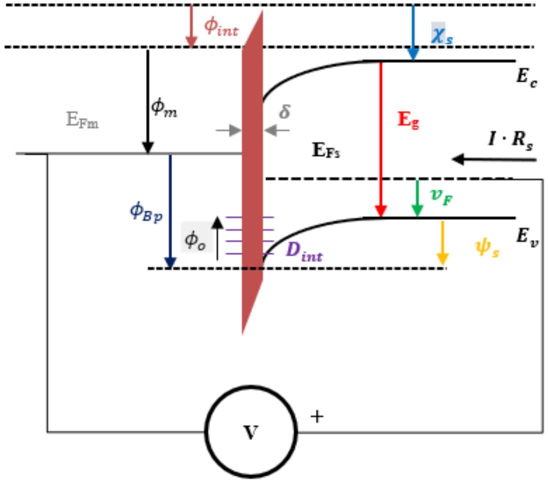
Introduction

- Take the thin interface oxide layer into consideration
  - The breakdown voltage is much higher than expected from earlier TCAD simulation
    - Wafers were left exposed in air after etching and prior to Al deposit
    - The silicon surface is oxidized to form an additional silicon dioxide layer



Introduction

- Take the thin interface oxide layer into consideration
  - Modelling of Schottky barrier in TCAD requires description of Fermi pinning
    - 2 models available in SDEVICE
      - Monch
      - Sze – used here



  - Schottky barrier height in Sze module is given by
    - $\phi_{Bp0}[eV] = \gamma \frac{1}{e}\left(E_g + \chi_s - \phi_m\right) + (1-\gamma)(\phi_0)$
      - $\gamma = \frac{\varepsilon_i}{\varepsilon_i + e^2 \delta D_{is}}$
      - ε_i: Permittivity of the interface layer [Q (Vcm)$^{-1}$]
      - δ: Interface layer thickness [cm]
      - D_{is}: Density of states per unity energy [cm^{-2} eV^{-1}]
      - χ_s: Electron affinity of semiconductor
      - ϕ_m: Metal work function

Introduction

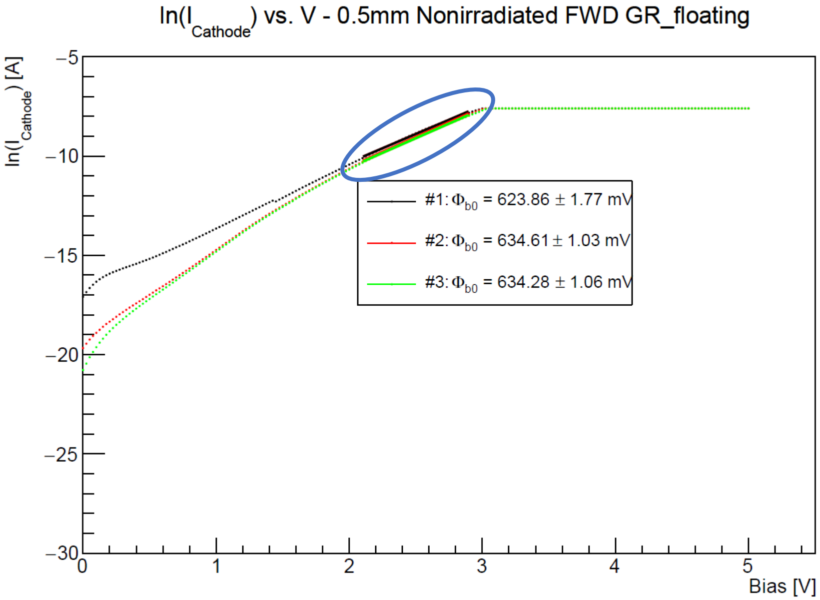
- Take the thin interface oxide layer into consideration
  - Forward current
    - Thermionic emission theory
      - Barrier height ϕ_{Bp0}
        - $I = SA^*T^2 \exp\left(-\frac{e}{k_BT}\phi_{Bp0}\right)\exp\left(\frac{e}{nk_BT}V\right) = I_0 \exp\left(\frac{e}{nk_BT}V\right)$
          - S: Area of the device $[cm^2]$
          - A^*: Richardson's constant 32 $[Acm^{-2}K^{-2}]$
          - n: Ideality factor
        - $\Rightarrow \ln(I) = \ln(I_0) + \frac{e}{nk_BT}V$
        - $\Rightarrow \phi_{Bp0} = \frac{k_BT}{e}\ln\left(\frac{SA^*T^2}{I_{V=0}}\right)$

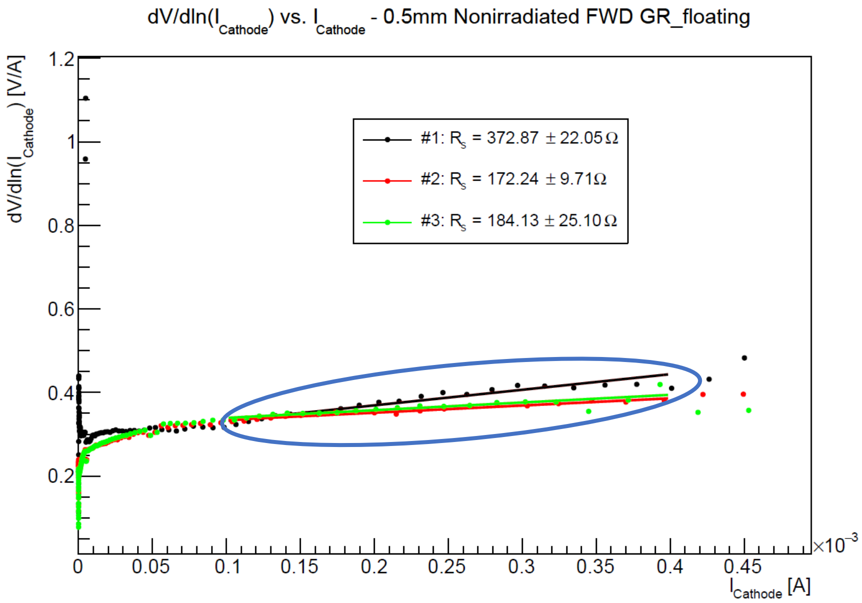
Introduction

- Take the thin interface oxide layer into consideration
  - Forward current
    - Taking into account the resistance R_s of the substrate
      - $I = SA^*T^2 \exp\left(-\frac{e}{kT}\phi_{Bp0}\right) \exp\left(\frac{e}{nkT}(V - R_sI)\right) = I_0 \exp\left(\frac{e}{nkT}(V - R_sI)\right)$
      - $\Rightarrow \frac{dV}{dln(I)} = \frac{nkT}{e} + R_sI$
        - $R_s \sim \rho\frac{L}{S} = \frac{1}{eN_A\mu_p}\frac{L}{S}$
      - $\Rightarrow n(V)$

Introduction

- Take the thin interface oxide layer into consideration
  - Forward current (Forward bias: 0 – 5V with GR floating)
    - Φ_{b0} and $n(V)$ extracted
    - The calculation of resistivity still needs further investigation



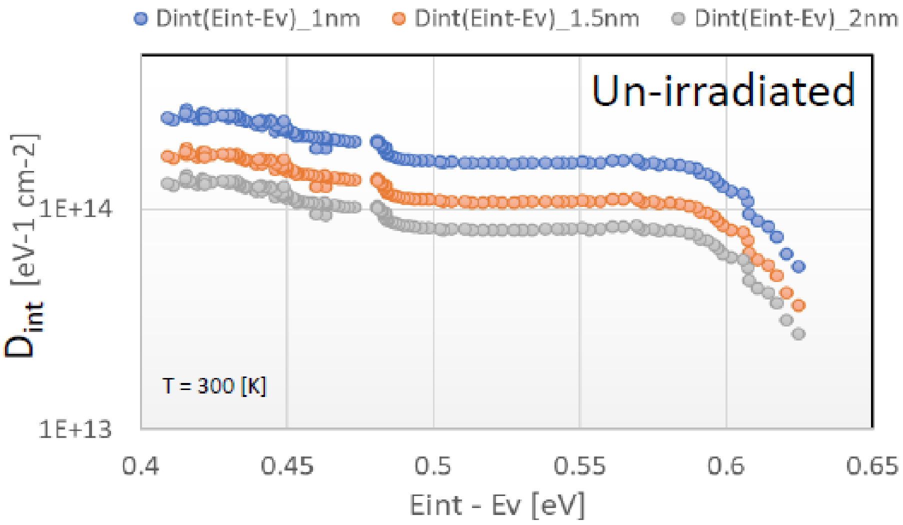


Introduction

- Take the thin interface oxide layer into consideration
  - Density of interface states extracted from ideality factor
    - Card H C, Rhoderick E H. Studies of tunnel MOS diodes I. Interface effects in silicon Schottky diodes[J]. Journal of Physics D: Applied Physics, 1971, 4(10): 1589.
    - $D_{is}(V) = \frac{1}{e}\left(\frac{\varepsilon_i}{\delta}(n(V)-1) - \frac{\varepsilon_{Si}}{W(V)}\right)$
  - Charge Neutrality Level (CNL)
    - $\phi_{Bp0}[eV] = \gamma\frac{1}{e}(E_g + \chi_s - \phi_m) + (1-\gamma)(\phi_0)$
      - At V=0 one recovers the neutrality level ϕ_0 w.r.t. top of valence band
      - In Sentaurus TCAD the CNL parameter is with respect to vacuum level
        - $CNL = \phi_m + \ 2 * \phi_{Bp0} - \phi_0 \ - \phi_F$
          - ϕ_F: The Fermi potential $\frac{kT}{e}\ln\left(\frac{N_V}{N_A}\right)$
          - N_A deduced from CV (and compared with SIMS)

Introduction

- Take the thin interface oxide layer into consideration
  - Calculate the $D_{is}(V)$ and CNL for δ of native oxide layer
    - The D_{is} used in TCAD simulation is the average
      - Seem not possible to include D_{is} energy dependence in TCAD
    - We assume three δ values for the native oxide layer
      - 1.0nm, 1.5nm, 2.0nm



	δ=1 nm	δ=1.5 nm	δ=2 nm
$< D_{is}(V) >$	**1.95E+14**	**1.3E+14**	**9.77e13**
CNL	**4.5**	**4.59**	**4.67**

Procedure of Simulation

- Simulation of the device manufactory process using SPROCESS
  - Substrate definition and initialization
    - Substrate structure
    - 100µm thickness
    - 5×10^{18} cm^{-3} Boron doping

  - Thermal P-type epitaxial layer growth
    - 50µm thickness
    - 3.3×10^{12} cm^{-3} Boron doping
    - Temperature ramping from 550℃ to 1000℃ in 1 minute
    - Annealing
      - 1000℃ for 20 hours

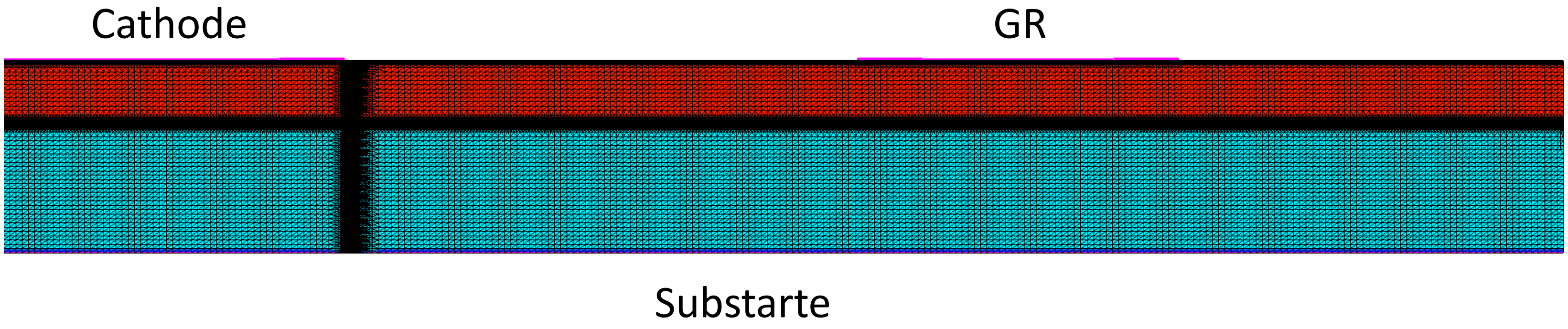
Procedure of Simulation

- Simulation of the device manufactory process using SPROCESS
  - SiO2 anisotropic deposit
    - 500nm thickness
  - Mask of cathode and GR
    - 1000nm thickness
  - Anisotropic etching of SiO2
    - Plasma etching in reality but very anisotropic
  - Aluminum isotropic deposit
    - 1000nm thickness
  - Mask of cathode and GR
    - 2500nm thickness
  - Anisotropic etching of aluminum
    - 1100nm thickness

Procedure of Simulation

- Simulation of the device manufactory process using SPROCESS
  - Highly doping at the bottom
    - 10^{20} cm^{-3}
    - Ohmic contact

  - Re-meshing
    - More meshes in the area of interest



Procedure of Simulation

- Simulation using SDEVICE
  - Physics models
    - SDEVICE parameters for optical generation
      - OpticalGeneration (QuantumYield (StepFunction (EffectiveBandgap))
      - ComplexRefractiveIndex (CarrierDep(Imag) WavelengthDep(Imag))
        - Extinction coeff. only
      - OpticalSolver (OptBeam (LayerStackExtraction (WindowName = "LaserW“ Position = (0, Y_hit, Z_hit) Mode = ElementWise
        - Laser window of 5 x 5 um2, centre position retrieved from .gds, default NumberOfCellsPerLayer
      - Wavelength= 1.064
        - Incident light wavelength [um]
      - Intensity= @<????*exp(-0.036*@Silicide_Thick@)*0.966>@
        - Depends on the simulation run, i.e. effective value of Laser power density
      - PolarizationAngle= 0 Theta= 90 Phi = 0

Procedure of Simulation

- Simulation using SDEVICE
  - Physics models
    - SDEVICE parameters for mobility and recombination
      - Temperature = 21°C
      - Fermi
      - SRH (DopingDependence TempDependence ElectricField (Lifetime = Hurkx))
      - Mobility(PhuMob Enormal (Lombardi PosInterfaceCharge), HighFieldSaturation(GradQuasiFermi)
      - UniBo for impact ionization (incl. Auger, GradQuasiFermi)
      - Excluded flat elements by using FlatElementExclusion

Procedure of Simulation

- Simulation using SDEVICE
  - Math models
    - Cylindrical
      - To make effectively a 3D simulation from the 2D mesh
    - Pardiso(iterativeRefinement)
    - ParallelToInterfaceInBoundaryLayer(FullLayer -ExternalBoundary)
    - Geometricdistances
      - At interfaces
    - e/hMobilityAveraging=ElementEdge
      - For interface mobility degradation
    - NonLocal meshes at contacts (Length = 40 nm)
    - RefDens_eGradQuasiFermi_ElectricField=1e10
    - TrapsDLN=30
    - Traps(Damping=100)
    - At high fluences (1e15) explicit traps filling at the beginning of transient simulation, then ‘unfreezing’ before charge injection (longer initial transients)

Procedure of Simulation

- Simulation using SDEVICE
  - Pinning parameters used in Sentaurus TCAD
    - In Sentaurus TCAD, the pinning effect at the Schottky contacts is enabled by specifying pinning in the electrode section and model used

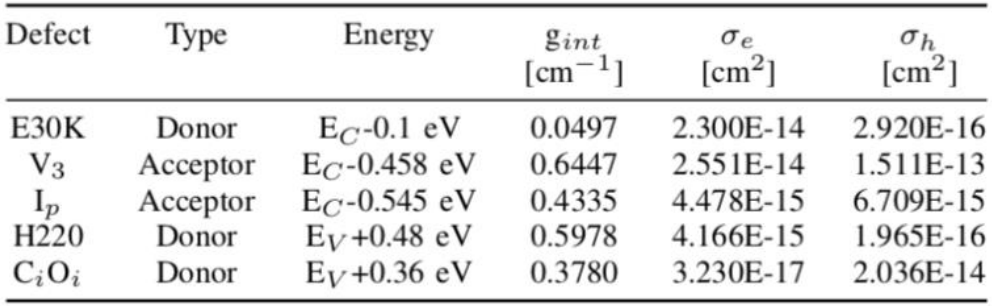
      -
        ```
        { Name = "CathodeR" Voltage = 0.0 Material=Aluminum
        Schottky(Pinning(Model="Sze"))   Resistance=1E2 }
        ```
    - The pinning parameters are added in the Schottky subsection of the electrode section of the sdevice parameter file

      -
        ```
        Electrode = "CathodeR"  {
        Schottky {
        ###Fermi pinnning params
        Pinning_d =@dint_thick@
        Pinning_CNL =@CNL@
        Pinning_Nint =@Nint@
                  }
                                        }
        ```

	δ=1 nm	δ=1.5 nm	δ=2 nm
$< D_{is}\ (V) >$	**1.95E+14**	**1.3E+14**	**9.77e13**
CNL	**4.5**	**4.59**	**4.67**

Procedure of Simulation

- Simulation using SDEVICE
  - Radiation model
    - Hamburg Penta Trap Model (HPTM)

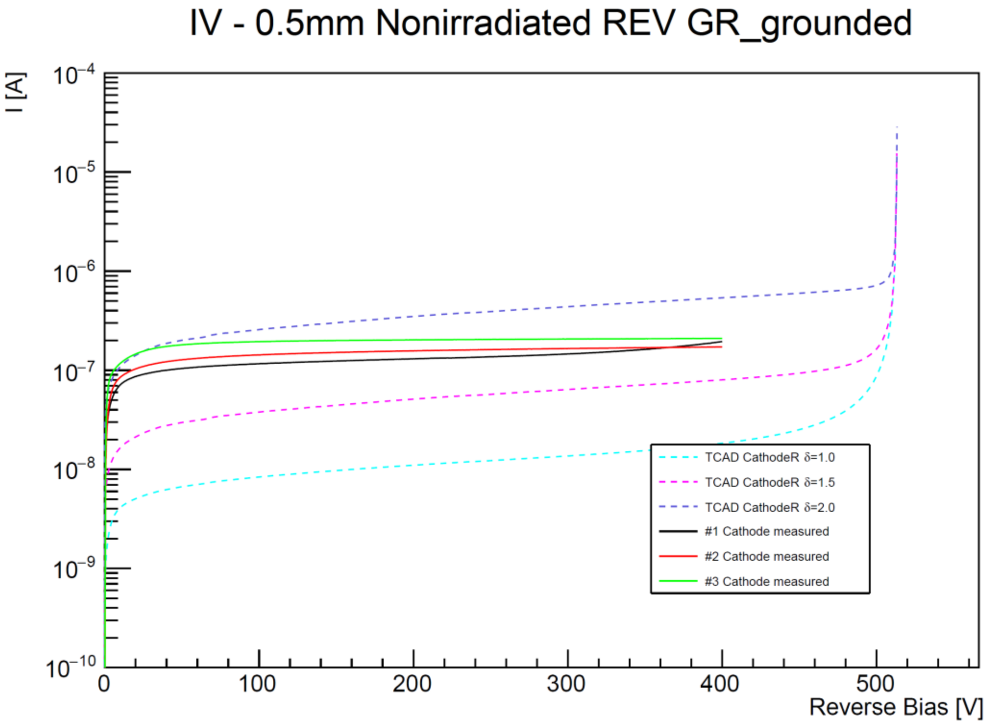


Defect	Type	Energy	g_{int} [cm^{-1}]	σ_e [cm^2]	σ_h [cm^2]
E30K	Donor	E_C-0.1 eV	0.0497	2.300E-14	2.920E-16
V_3	Acceptor	E_C-0.458 eV	0.6447	2.551E-14	1.511E-13
I_p	Acceptor	E_C-0.545 eV	0.4335	4.478E-15	6.709E-15
H220	Donor	E_V+0.48 eV	0.5978	4.166E-15	1.965E-16
C_iO_i	Donor	E_V+0.36 eV	0.3780	3.230E-17	2.036E-14

- Trap concentration of defects
  - $N = g_{int} \cdot \Phi_{neq}$
  - A factor 1.66 has been applied to g_{int} to account for Neutron irradiation

Comparison between Measurement and Simulation

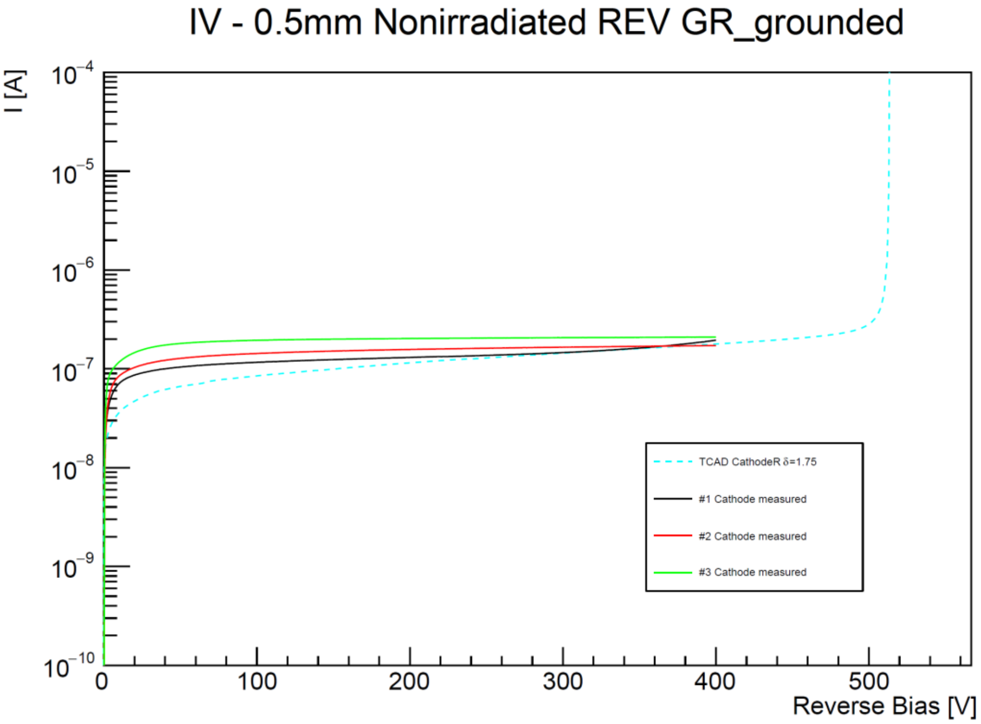
- IV simulation
  - Non-irradiated
    - δ = 1.0nm, 1.5nm, 2.0nm



- No breakdown below -400V
- δ should be between 1.5 and 2.0 nm

Comparison between Measurement and Simulation

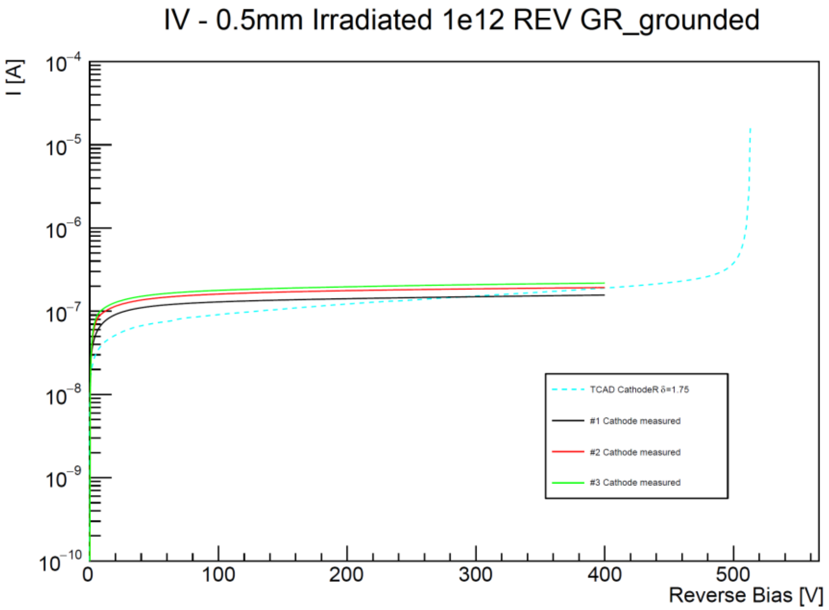
- IV simulation
  - Non-irradiated
    - $\delta = 1.75\text{nm}$

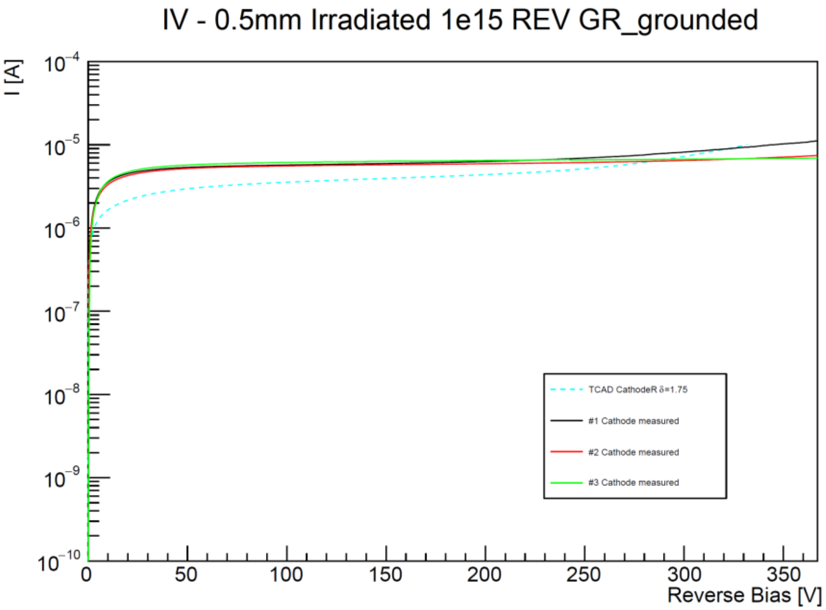


- More consistent with the measurements
  - Use this value to do more simulations

Comparison between Measurement and Simulation

- IV simulation
  - Neutron irradiated - 10^{12} and 10^{15} [1MeV n_{eq}/cm^2]
    - δ = 1.75nm





- Current compliance in simulation
  - 1×10^{-5}A
- Relatively consistent with the measurements

Summary

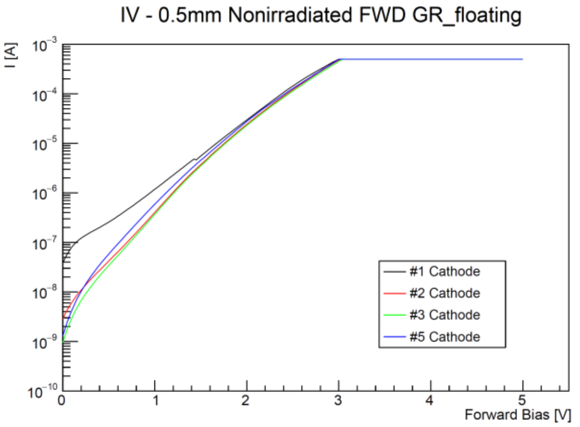
- Summary
  - P-type epitaxial Schottky diodes simulated with TCAD
  - The thickness of the native interface oxide layer is around 1.75nm
  - Simulations of IV relatively consistent with the measurements

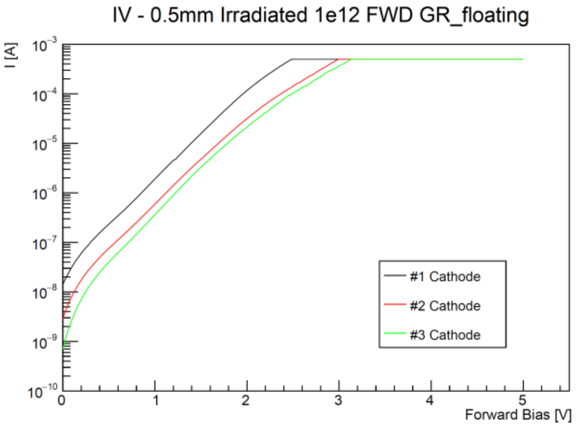
- Next
  - Simulation optimization
  - More simulations should be done
    - Other Neutron fluence
    - CV and CCE

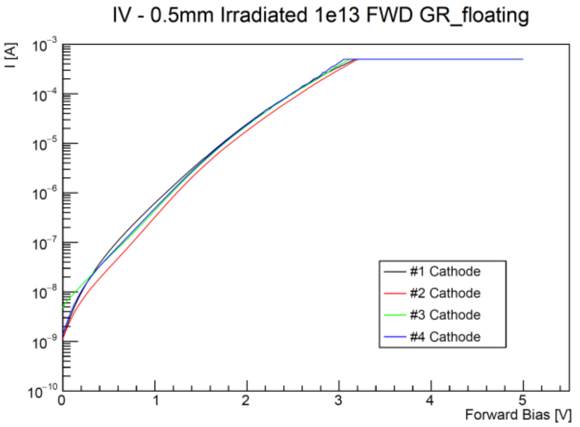
Thanks!

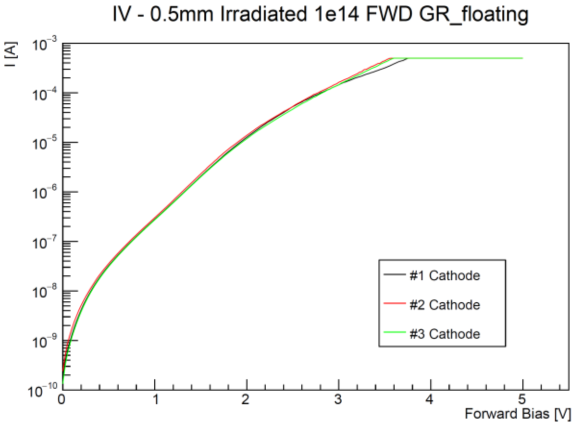
BACKUP

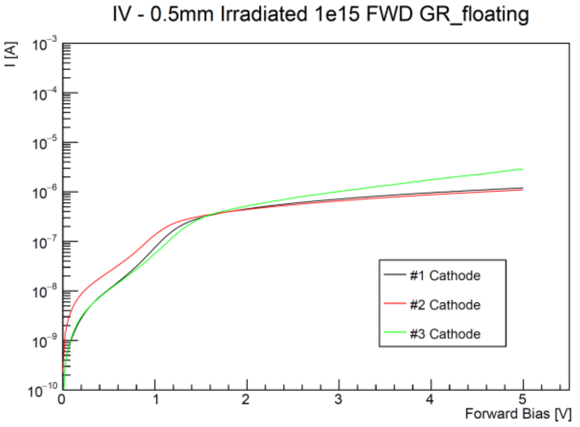
FWD IV – GR Floating

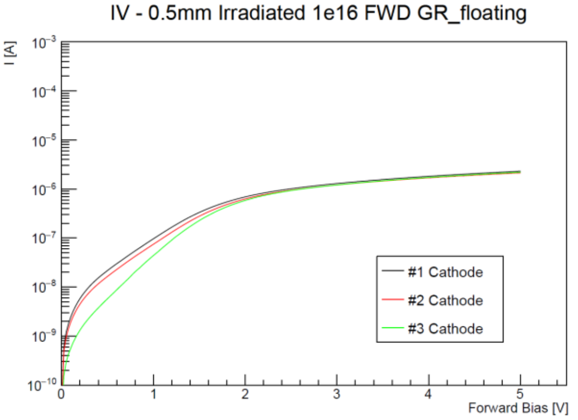




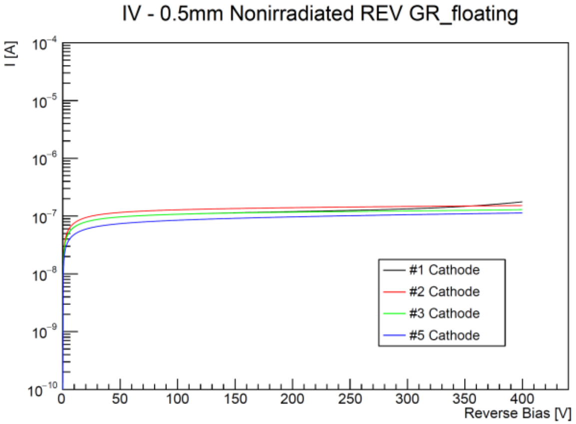


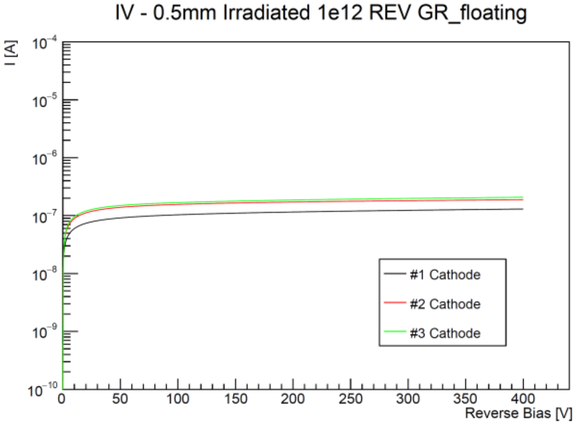


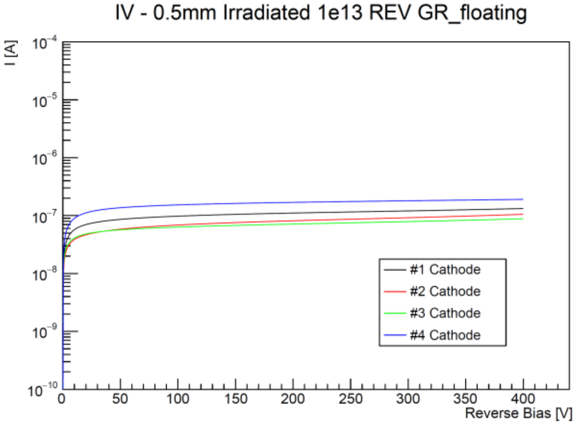


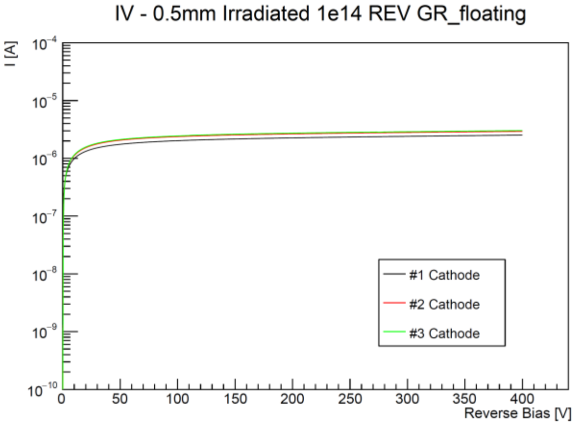


REV IV – GR Floating


IV - 0.5mm Nonirradiated REV GR_floating


IV - 0.5mm Irradiated 1e12 REV GR_floating


IV - 0.5mm Irradiated 1e13 REV GR_floating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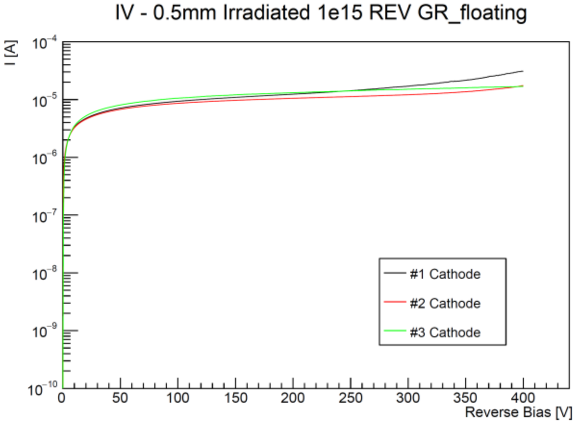
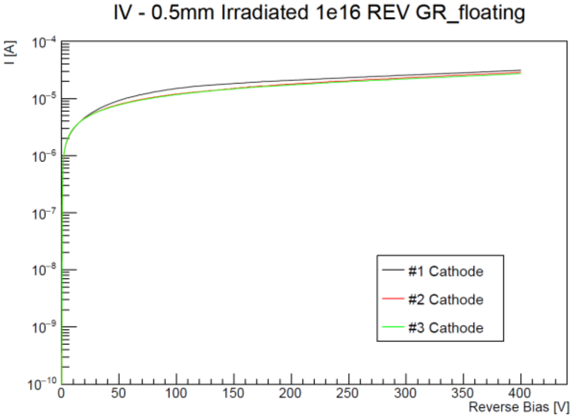
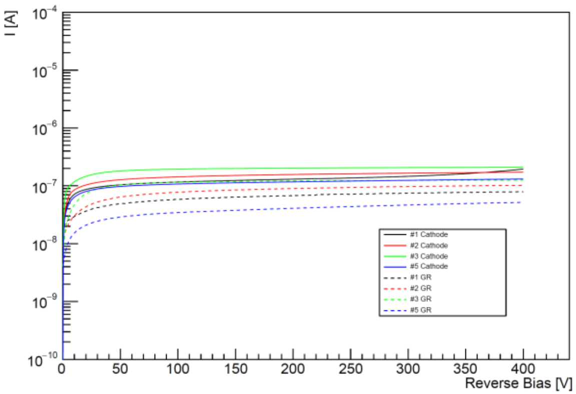
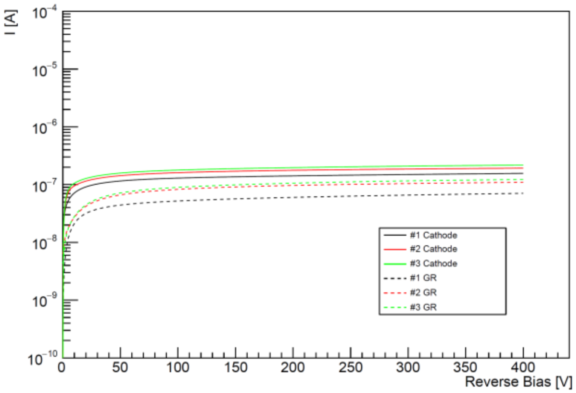

IV - 0.5mm Irradiated 1e15 REV GR_floating


IV - 0.5mm Irradiated 1e16 REV GR_floating

REV IV – GR Grounded


IV - 0.5mm Nonirradiated REV GR_grounded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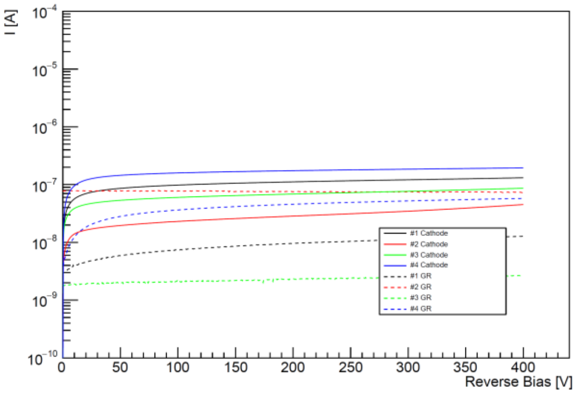
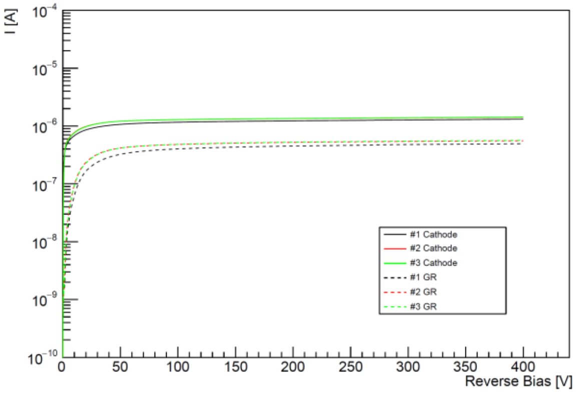
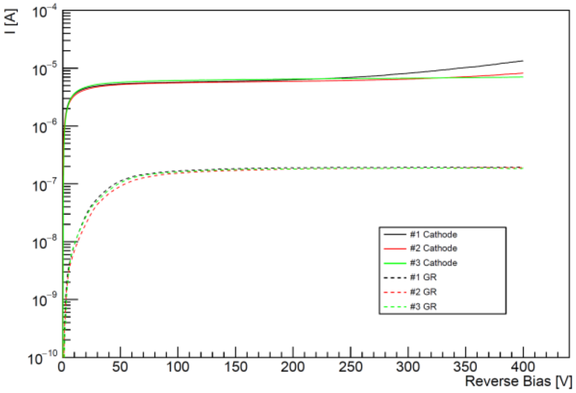
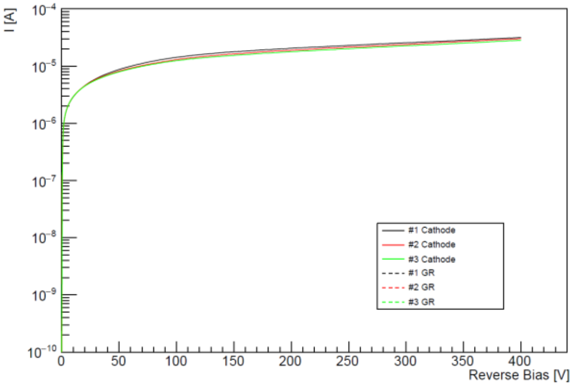

IV - 0.5mm Irradiated 1e13 REV GR_grounded

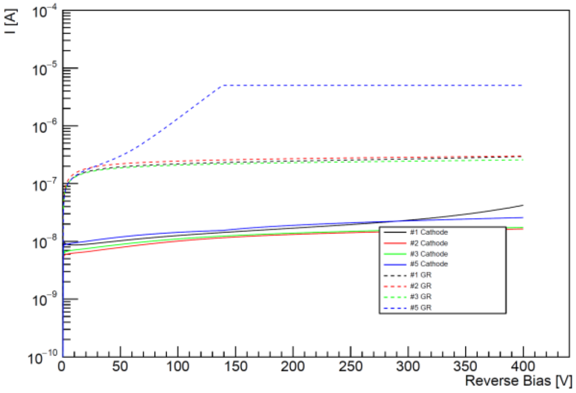

IV - 0.5mm Irradiated 1e14 REV GR_grounded


IV - 0.5mm Irradiated 1e15 REV GR_grounded

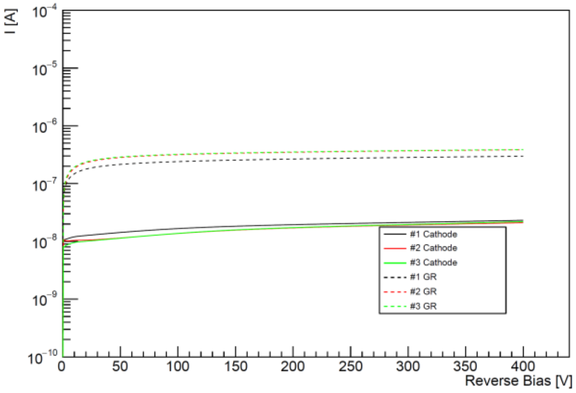

IV - 0.5mm Irradiated 1e16 REV GR_grounded

REV IV – GR at the Same Potential as Cathode

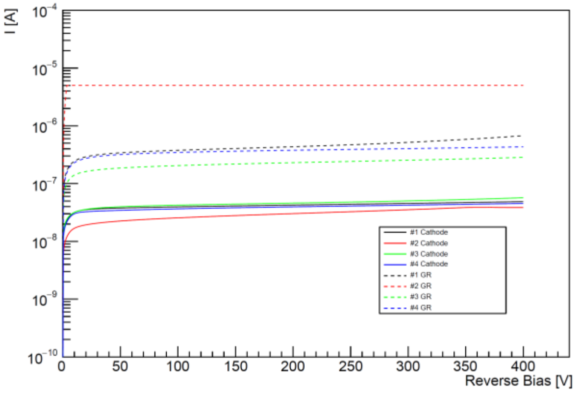
IV - 0.5mm Nonirradiated REV GR_at_the_same_potential_as_cathode



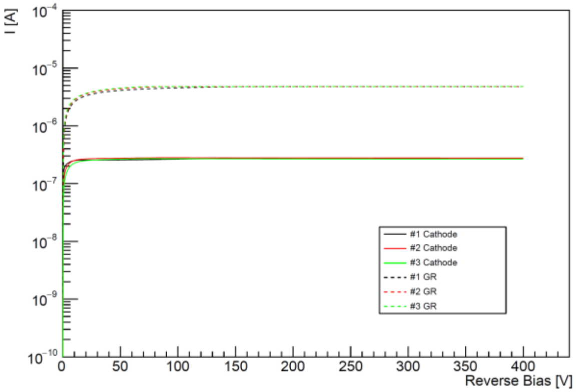
IV - 0.5mm Irradiated 1e12 REV GR_at_the_same_potential_as_cathode



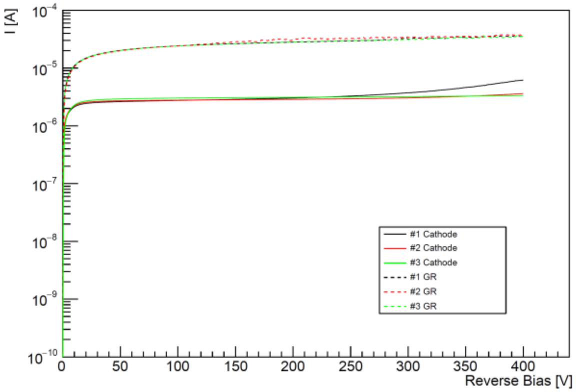
IV - 0.5mm Irradiated 1e13 REV GR_at_the_same_potential_as_cathode



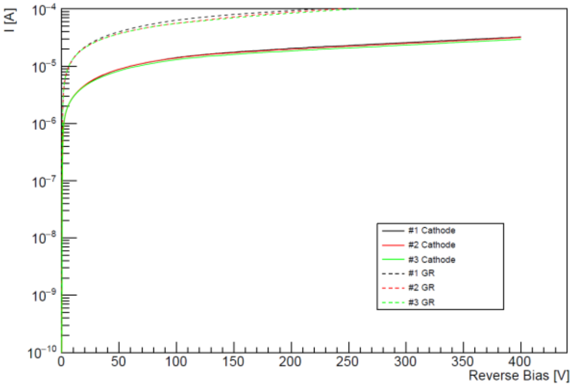
IV - 0.5mm Irradiated 1e14 REV GR_at_the_same_potential_as_cathode



IV - 0.5mm Irradiated 1e15 REV GR_at_the_same_potential_as_cathode



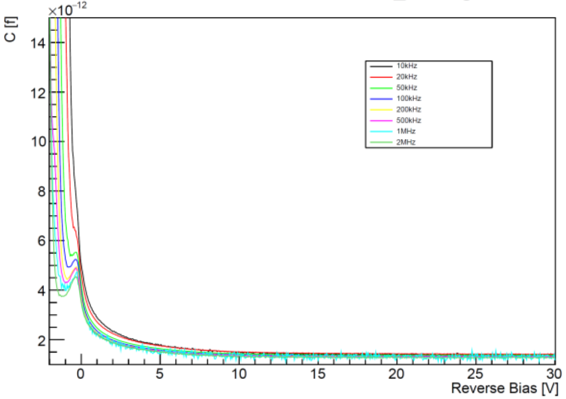
IV - 0.5mm Irradiated 1e16 REV GR_at_the_same_potential_as_cathode



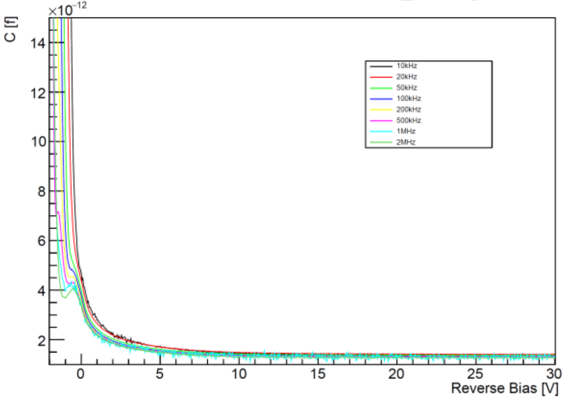
CV – GR Floating

Plot of each diode looks similar
Just diodes #1 shown here

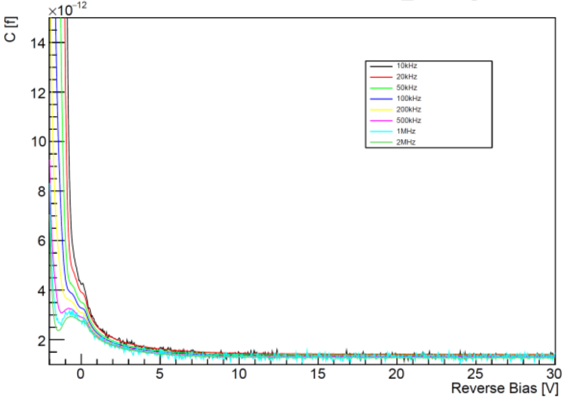
CV - 0.5mm Nonirradiated GR_floating #1



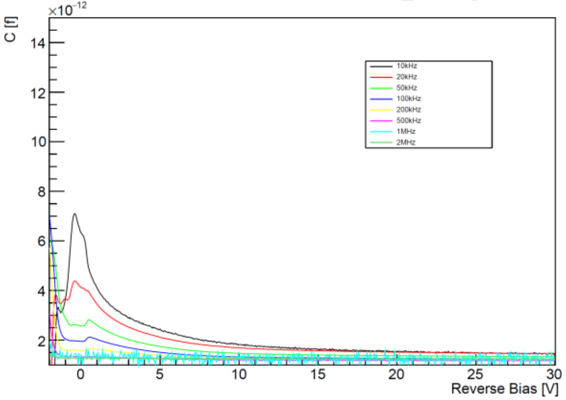
CV - 0.5mm Irradiated 1e12 GR_floating #1



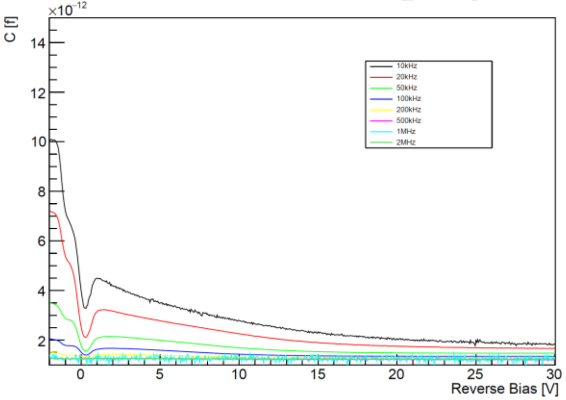
CV - 0.5mm Irradiated 1e13 GR_floating #1



CV - 0.5mm Irradiated 1e14 GR_floating #1



CV - 0.5mm Irradiated 1e15 GR_floating #1



CV - 0.5mm Irradiated 1e16 GR_floating #1