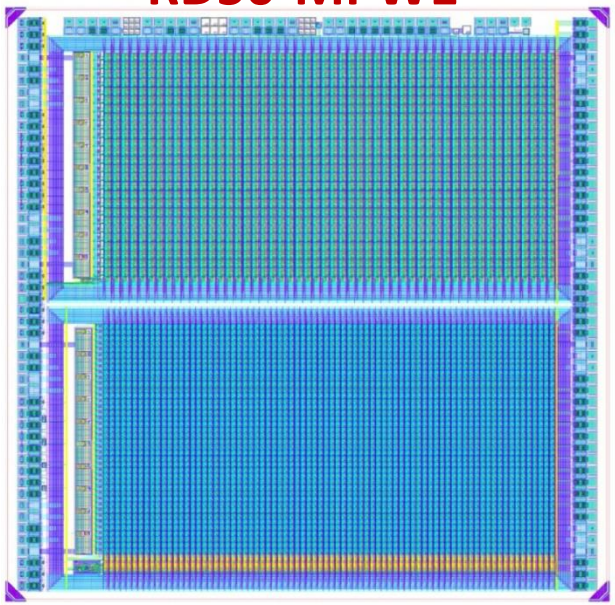
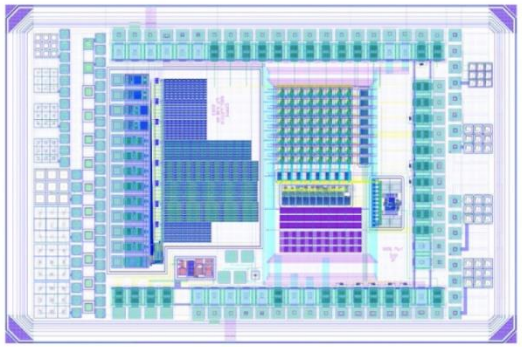
CERN-RD50 – Monolithic CMOS

- R&D programme to study and develop radiation hard High Voltage CMOS devices for very high luminosity colliders (HL-LHC, FCC)

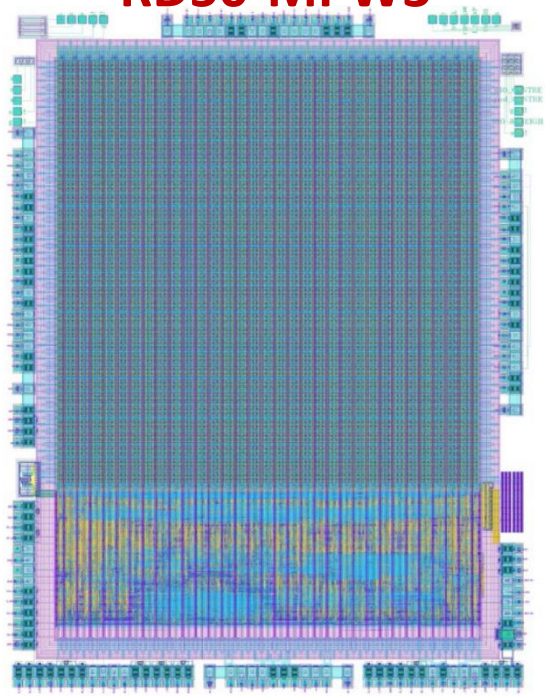
RD50-MPW1



RD50-MPW2



RD50-MPW3

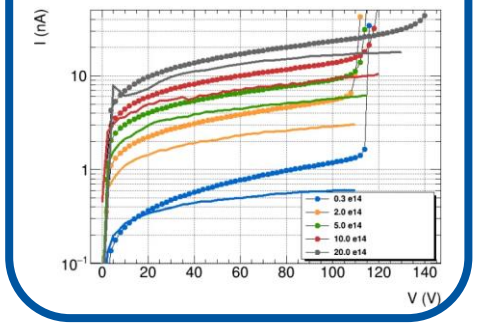


2017 2018 2019 2020 2021 2022 2023 +

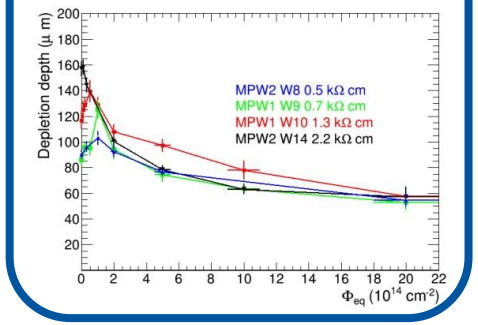
RD50-MPW2

- Prototype HV-CMOS sensor with test structures and a small active pixel matrix, fabricated in high resistivity substrates in a Multi-Project Wafer submission with LFoundry.
  - Aim to study and improve time resolution and radiation tolerance with 60 µm x 60 µm pixels
  - Evaluated in the lab before and after neutron irradiation up to 2e15 n_{eq}/cm^2

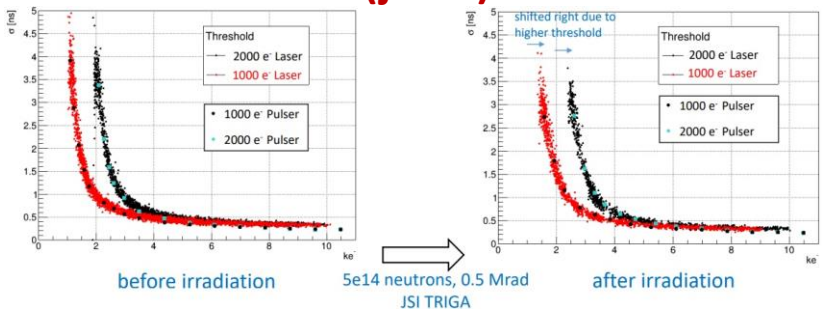
I-V (after 80 mins annealing)



eTCT @ V_HV = 100 V, 2 kΩcm

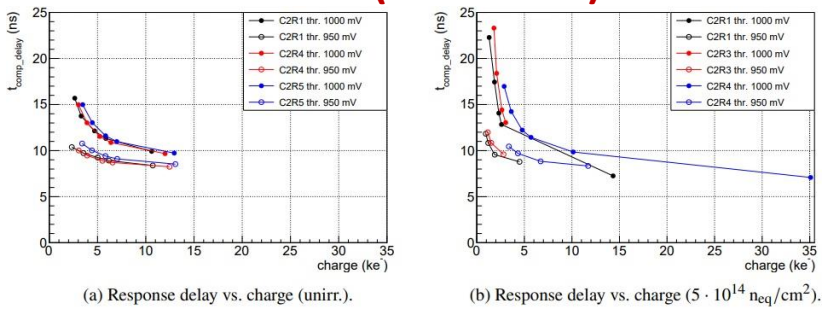


Time resolution (jitter)



Jitter < 160 ps before and after irradiation to 5e14

Time resolution (time-walk)



(a) Response delay vs. charge (unirr.). (b) Response delay vs. charge ($5 \cdot 10^{14}$ n_{eq}/cm^2).

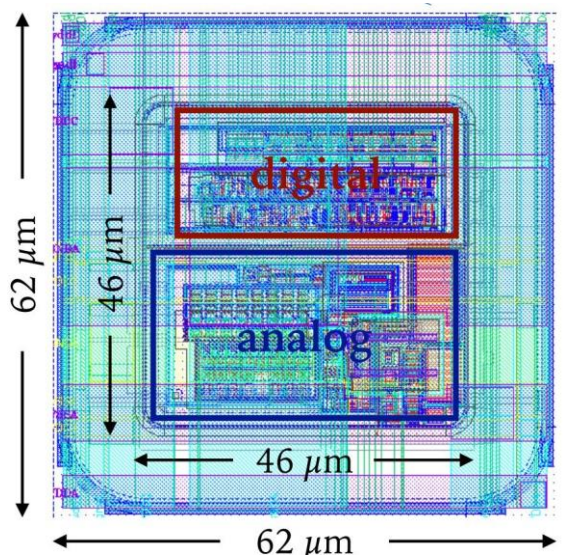
Time-walk < 10 ns before and after irradiation to 5e14 @ > 2ke⁻ collected

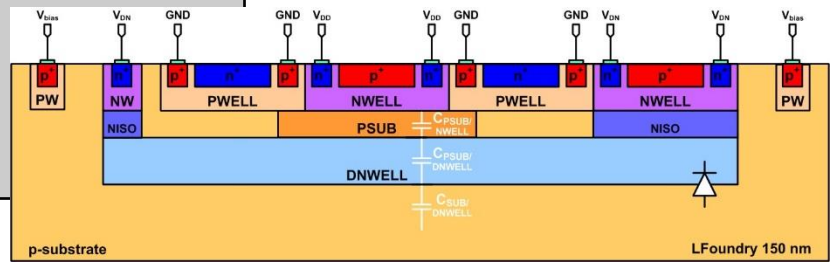
RD50-MPW3

Chip	RD50-MPW3
Technology	150 nm HV-CMOS LFoundry
Pixel size	62 µm x 62 µm (has analogue and digital readout)
Pixel matrix	64 rows x 64 columns
Chip size	5.1 mm x 7.6 mm (prototype size)

Third prototype iteration

- FE-I3 style readout (pixel coordinates + time-stamp)
- Pixels organised in double columns
- Minimises crosstalk noise
- Test structures with advanced guard rings to improve V_BD and radiation tolerance (V_BD > 400 V)





RD50-MPW3

- **Readout boards**
  - New chip board production (January 2023)
  - Piggy board production (early 2023)
    - To make an RD50-MPW3 telescope and evaluate it at test beams
- **Irradiation campaign (early 2023)**
  - Neutrons
  - Protons
- **Test beams**
  - DESY (spring 2023)
  - CERN (autumn 2023)
- **Defect evaluation (2023)**

RD50-MPW4?

- **New RD50 project, currently baking in the oven...**
- **Goal**
  - Provide a fully functional HV-CMOS pixel chip
  - Evaluate HV-CMOS sensors to very high fluence

RD50-MPW4?

- **To fix issues observed in RD50-MPW3**
  - Interface between matrix and periphery
    - We know the solution already (longer pull-down)
  - Easy generation of global time-stamp
    - We know the solution already (64-bit counter in the chip)
  - High noise in lower half of matrix
    - Currently studying this both in simulations and lab measurements

- **To further improve V_BD and therefore radiation tolerance too (V_BD > 400 V is possible)**
  - Improve rings around the chip as in test structures in RD50-MPW3
  - Improve HV distribution to the pixels (V_BD should not depend on the p/n pixel electrodes spacing any more)

- **To do backside biasing (thin beyond the 280 µm?)**
  - It is possible with MPW submissions (Liverpool experience with UKRI-MPW0 HV-CMOS chip)

LF15A MPW shuttle run – 2023 Schedule

LF15A		
Run ID	Tape In	Est. Ship date
C15E23	08-05-23	02-11-23
C15J23	23-10-23	18-04-24

→ **delivery in 1 year from now**

→ **delivery in 1.5 years from now**

- **Put in new RD50 funding request (~75 kEUR)**
  - If institutes are interested, please get in touch with me [Eva]
- **New Cadence Design Share Agreement?**
  - Inquire Europractice asap [Eva]

FPGAs for monolithic CMOS control

- **New RD50 project, currently baking in the oven...**
  - Repository for common code
  - Explore low-cost FPGA (e.g. Intel)
  - ~15 kEUR
  - If institutes are interested, please get in touch with Rogelio